

Compal Confidential

DCL55 Schematics Document

Banias ICP uFCBGA/uFCPGA Package with Montara-GM Core Logic

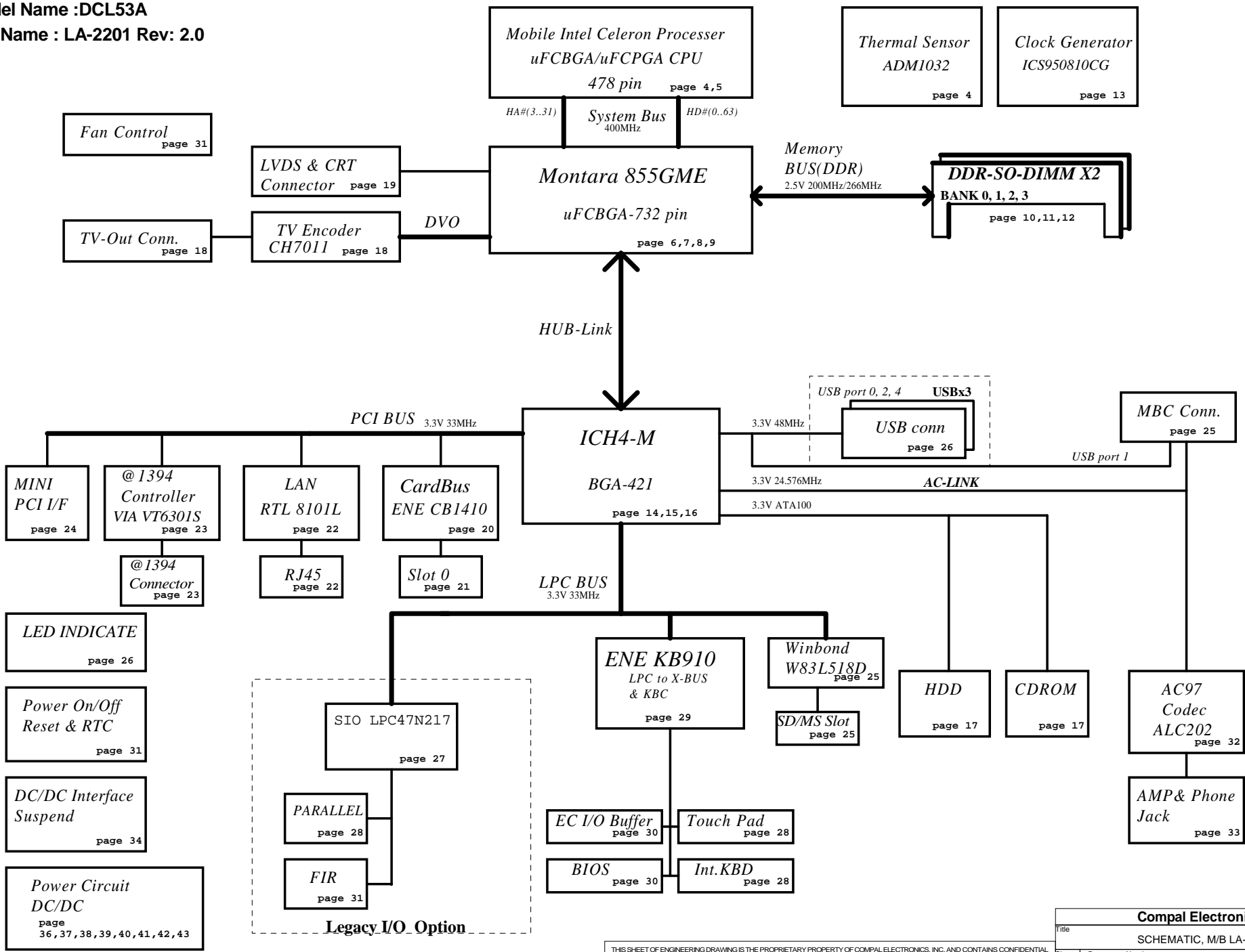
2005-05-23

REV: 3.0

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SCHEMATIC, M/B LA-2201			
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Model Name :DCL53A
File Name : LA-2201 Rev: 2.0



Voltage Rails

Power Plane	Description	S0-S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+CPU_CORE	Core voltage for CPU	ON	OFF	OFF
+VCCP	1.05V rail for Processor I/O	ON	OFF	OFF
+1.2VS	1.2VS switched power rail for GMCH	ON	OFF	OFF
+1.25VS	1.25V switched power rail	ON	OFF	OFF
+1.5VALW	1.5V power rail	ON	ON	ON
+1.5V	1.5V power rail	ON	ON	OFF
+1.5VS	1.5V power rail for GMCH	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+2.5V	2.5V power rail	ON	ON	OFF
+2.5VS	2.5V switched power rail	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+3V	3.3V power rail	ON	ON	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5V	5V power rail	ON	ON	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+12VALW	12V always on power rail	ON	ON	ON*
RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

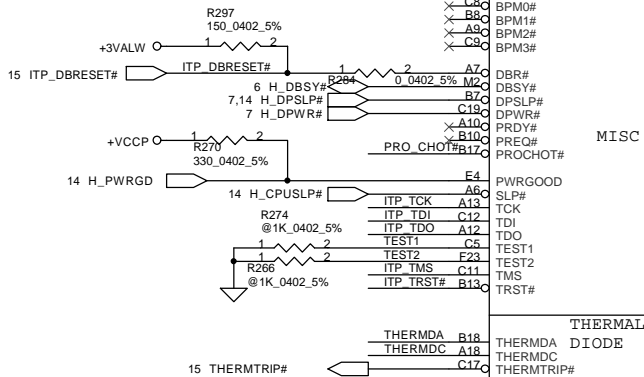
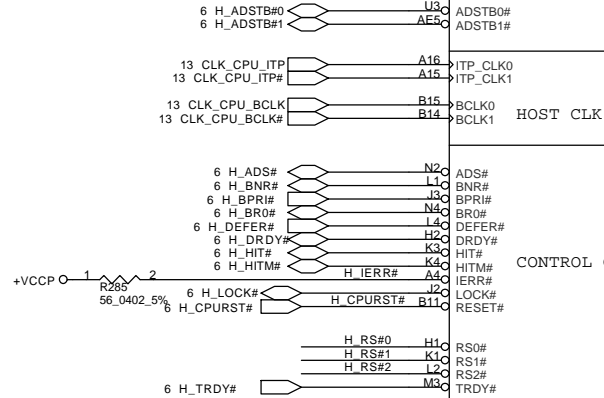
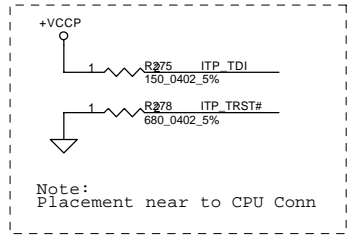
Board ID Table for AD channel

Vcc	3.3V +/- 5%			
R368	100K +/- 5%			
Board ID	R361	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

Board ID	PCB Revision
0	
1	0.1
2	0.2
3	1.0
4	
5	
6	
7	

External PCI Devices

Device	IDSEL#	REQ#/GNT#	Interrupts
CardBus	AD20	2	PIRQA
LAN	AD17	3	PIRQF
Mini-PCI	AD18/AD20	1/4	PIRQG/PIRQH
1394	AD16	0	PIRQE



AMP_1473129-1

Banias

ADDR GROUP

DATA GROUP

HOST CLK

CONTROL GROUP

MISC

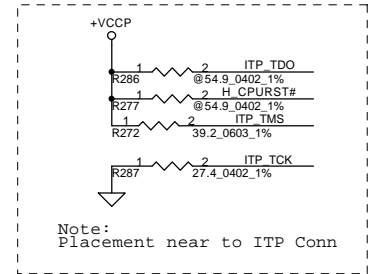
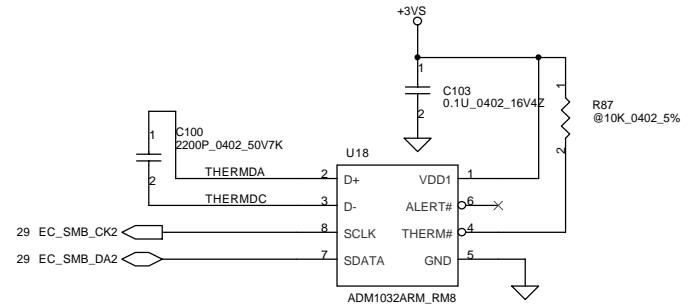
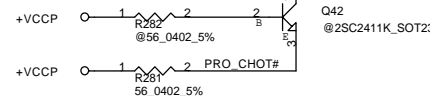
THERMAL DIODE

LEGACY CPU

D0#	A19	HD#0
D1#	A25	HD#1
D2#	A22	HD#2
D3#	B21	HD#3
D4#	A24	HD#4
D5#	B26	HD#5
D6#	A21	HD#6
D7#	B20	HD#7
D8#	C20	HD#8
D9#	B24	HD#9
D10#	D24	HD#10
D11#	E24	HD#11
D12#	C26	HD#12
D13#	B23	HD#13
D14#	E23	HD#14
D15#	C25	HD#15
D16#	H23	HD#16
D17#	G25	HD#17
D18#	L23	HD#18
D19#	M26	HD#19
D20#	H24	HD#20
D21#	E25	HD#21
D22#	G24	HD#22
D23#	J23	HD#23
D24#	M23	HD#24
D25#	J25	HD#25
D26#	L26	HD#26
D27#	N24	HD#27
D28#	M25	HD#28
D29#	H26	HD#29
D30#	N25	HD#30
D31#	K25	HD#31
D32#	Y26	HD#32
D33#	AA24	HD#33
D34#	T25	HD#34
D35#	U23	HD#35
D36#	V23	HD#36
D37#	B24	HD#37
D38#	B26	HD#38
D39#	C23	HD#39
D40#	U26	HD#40
D41#	V24	HD#41
D42#	U25	HD#42
D43#	V25	HD#43
D44#	V26	HD#44
D45#	AA26	HD#45
D46#	J25	HD#46
D47#	AB25	HD#47
D48#	AC23	HD#48
D49#	AB24	HD#49
D50#	AC20	HD#50
D51#	AC22	HD#51
D52#	AC25	HD#52
D53#	AD23	HD#53
D54#	AD22	HD#54
D55#	AE22	HD#55
D56#	AE23	HD#56
D57#	AD24	HD#57
D58#	AE20	HD#58
D59#	AE21	HD#59
D60#	AD21	HD#60
D61#	AE25	HD#61
D62#	AE22	HD#62
D63#	AE26	HD#63

DIN0#	D25	H_DIN#0 6
DIN1#	J26	H_DIN#1 6
DIN2#	T24	H_DIN#2 6
DIN3#	AD20	H_DIN#3 6
DSTBN0#	C23	H_DSTBN#0 6
DSTBN1#	K24	H_DSTBN#1 6
DSTBN2#	W25	H_DSTBN#2 6
DSTBN3#	AE24	H_DSTBN#3 6
DSTBP0#	C22	H_DSTBP#0 6
DSTBP1#	L24	H_DSTBP#1 6
DSTBP2#	W24	H_DSTBP#2 6
DSTBP3#	AE25	H_DSTBP#3 6

A20M#	C2	H_A20M# 14
FERR#	D3	H_FERR# 14
IGNNE#	A3	H_IGNNE# 14
INIT#	B5	H_INIT# 14
LINT0	D1	H_INTR# 14
LINT1	D4	H_NMI# 14
STPCLK#	C6	H_STPCLK# 14
SMI#	B4	H_SMI# 14

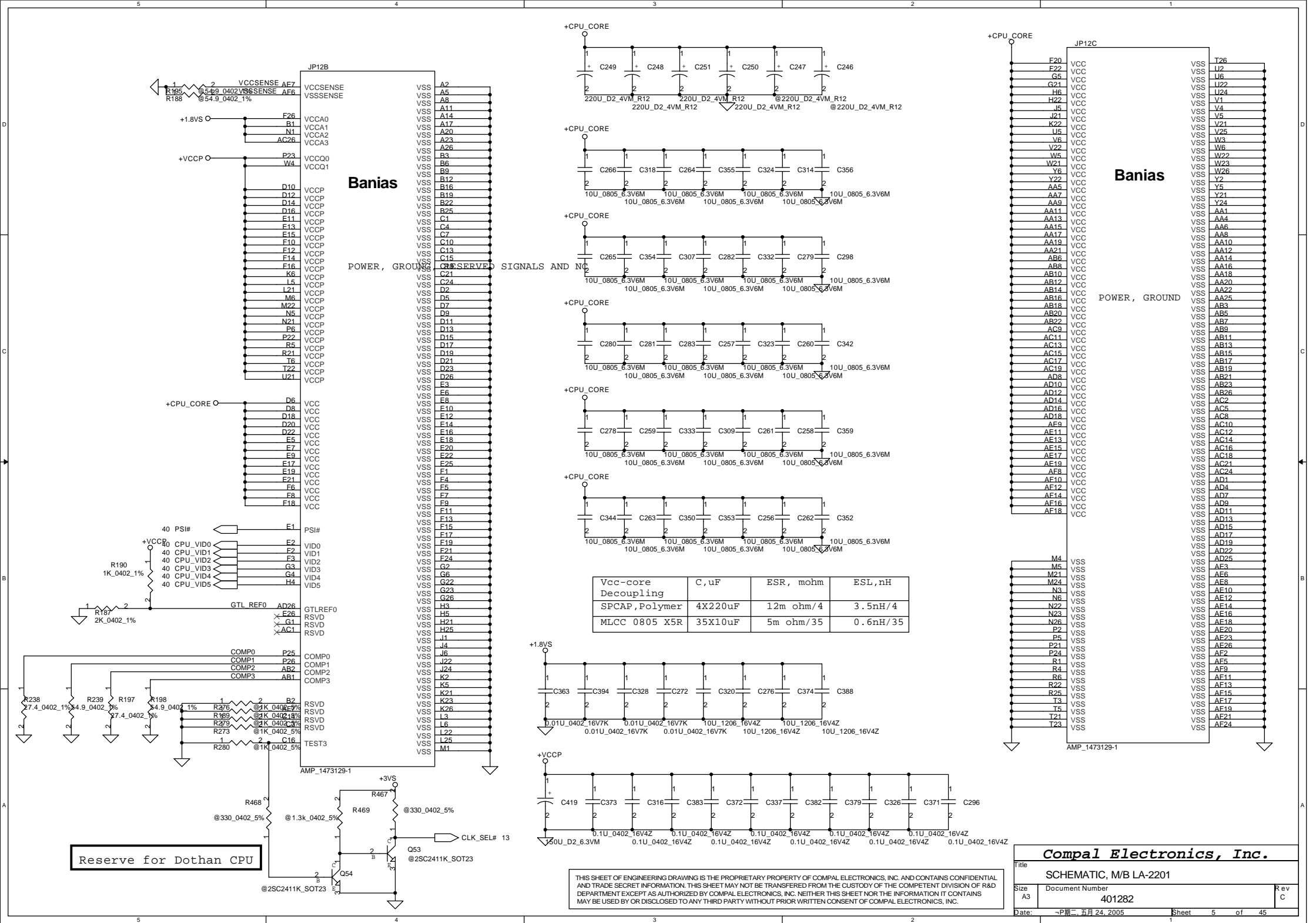


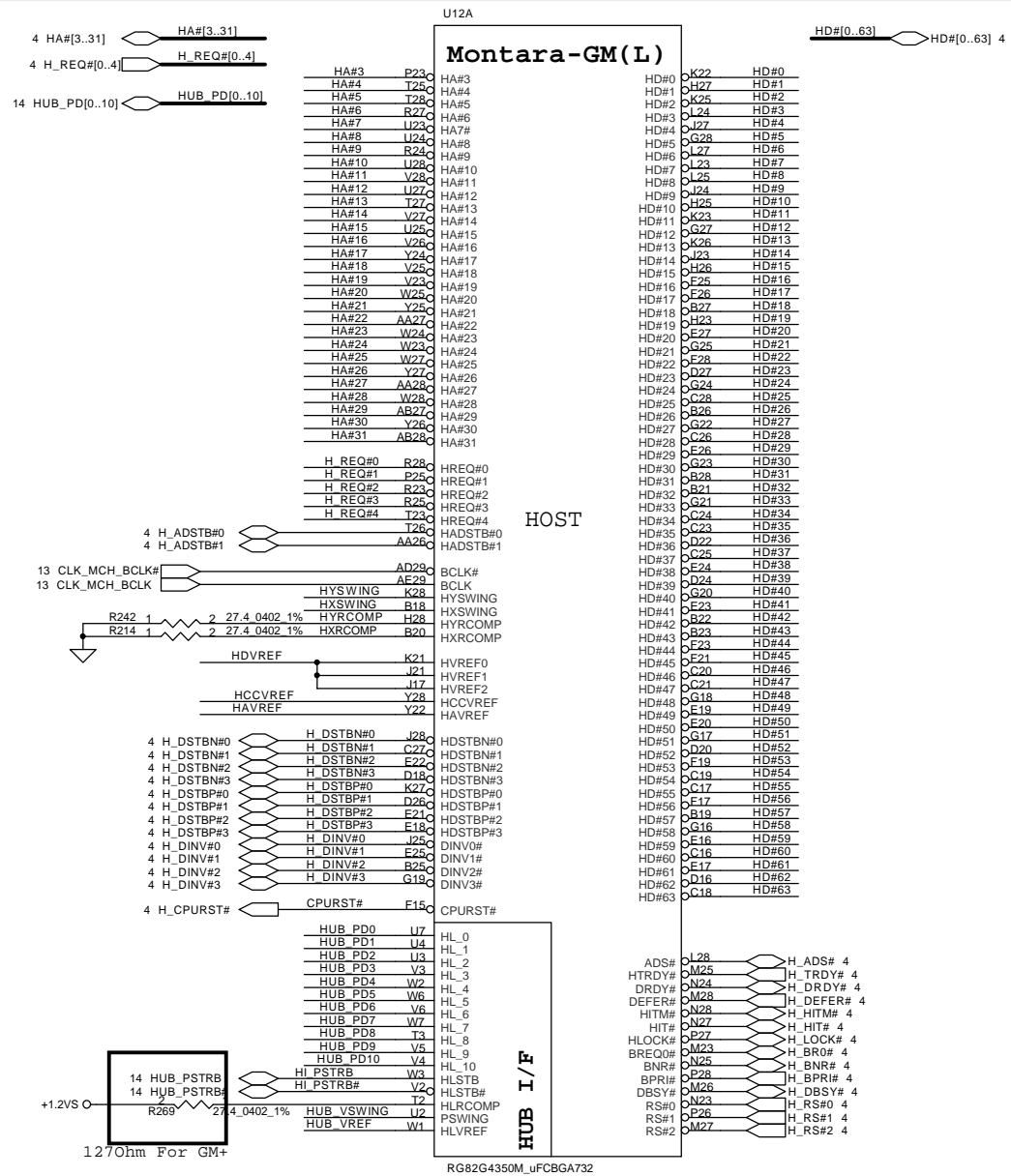
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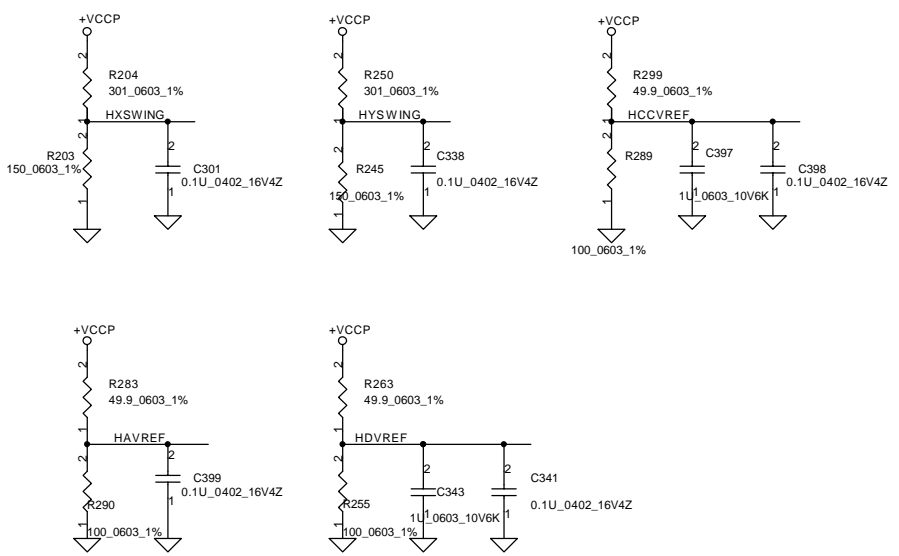
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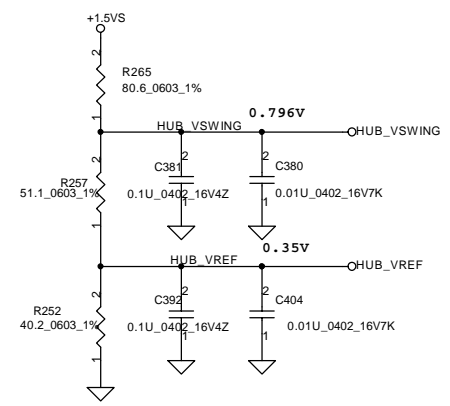


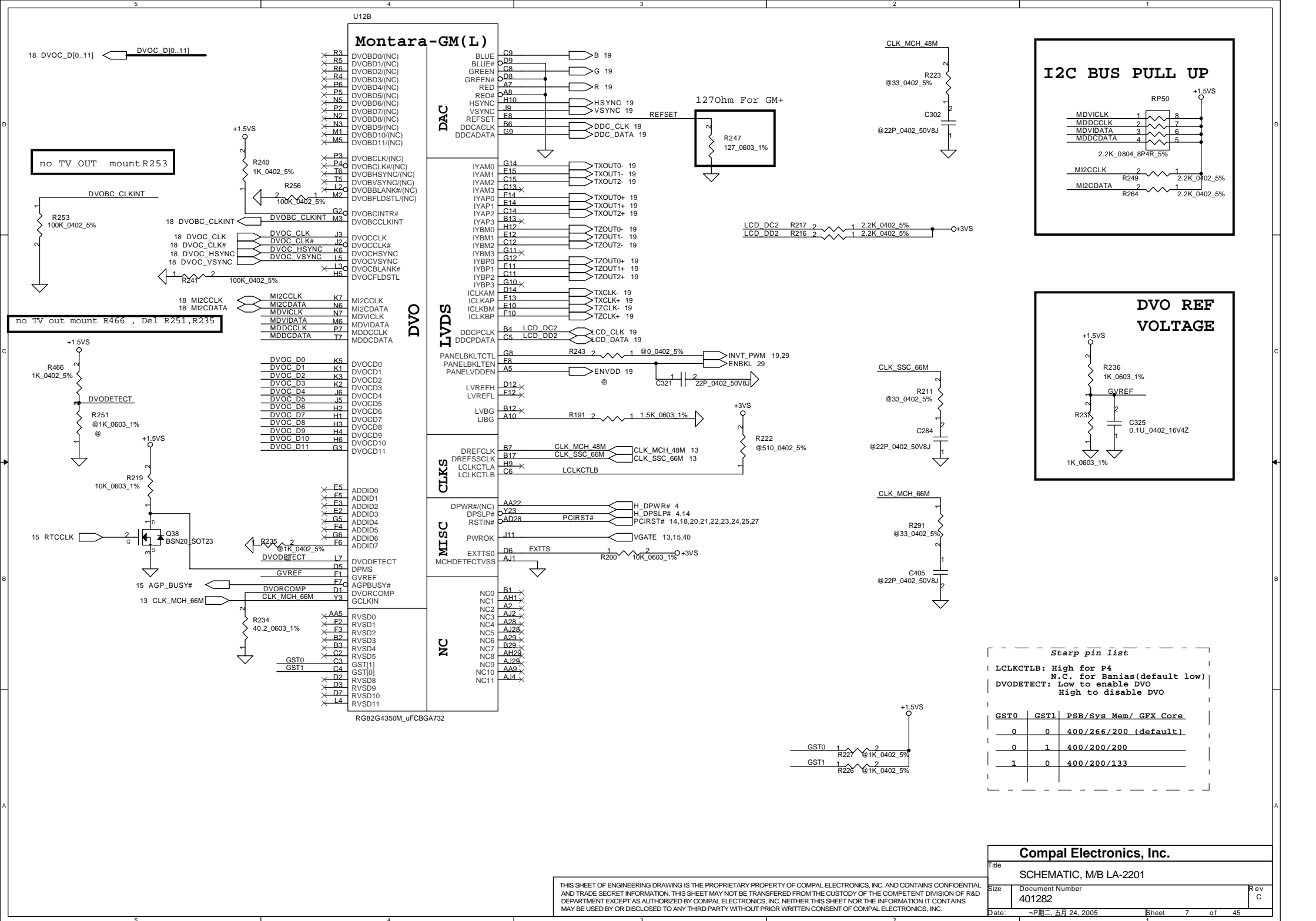


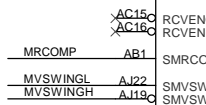
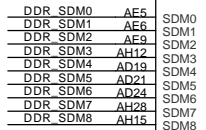
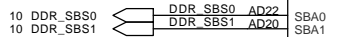
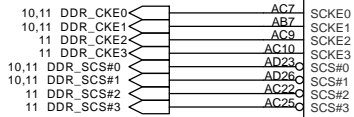
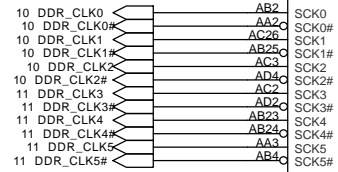
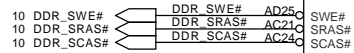
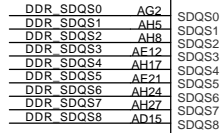
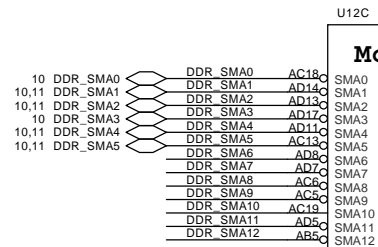
HOST REF VOLTAGE



HUB I/F REF VOLTAGE

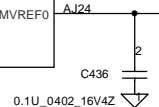
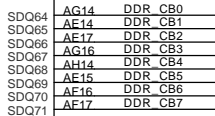
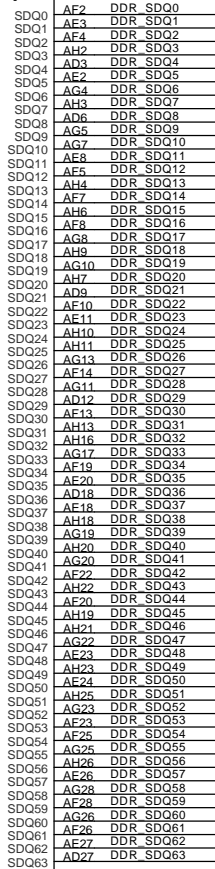




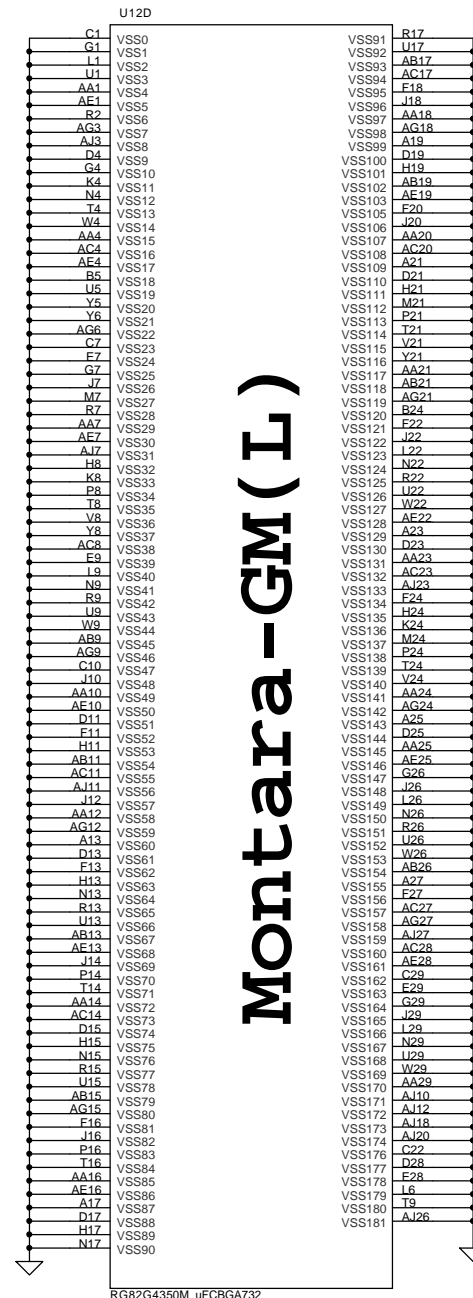
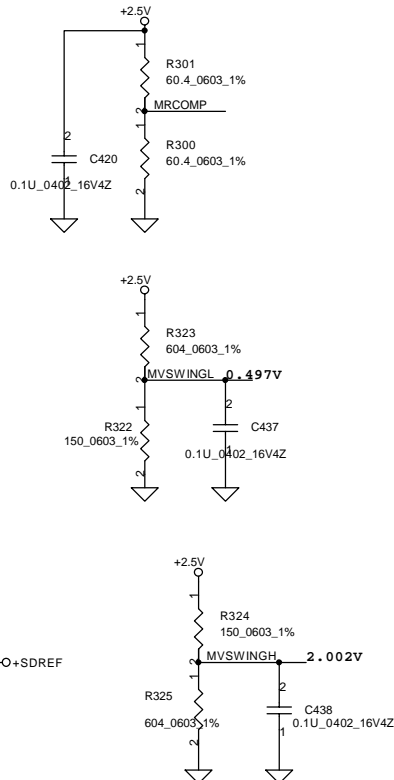


RG82G4350M_uFCBGA732

MEMORY



DDR REF & SWING VOLTAGE



RG82G4350M_uFCBGA732

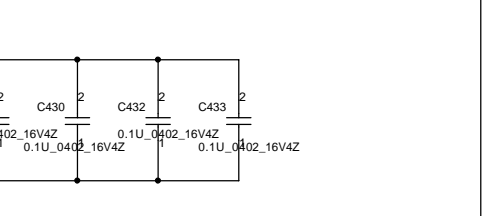
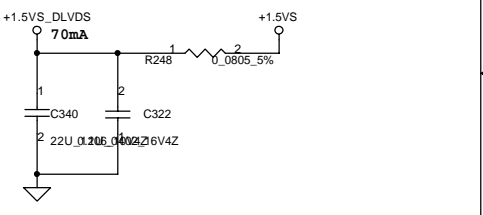
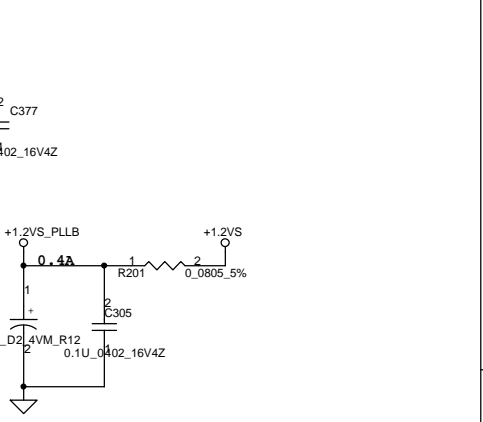
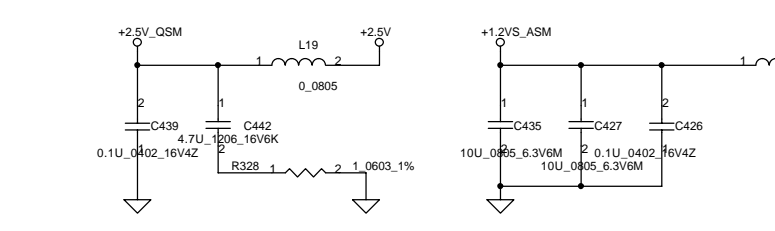
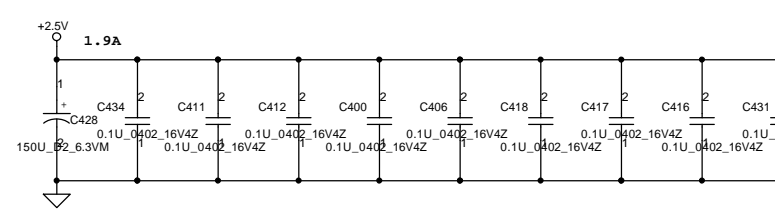
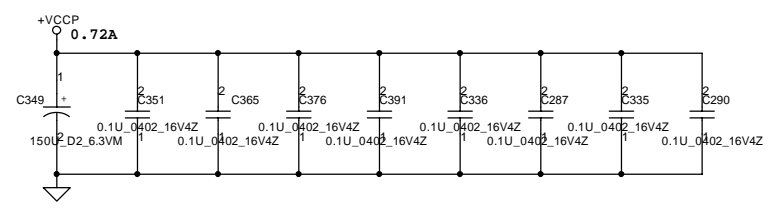
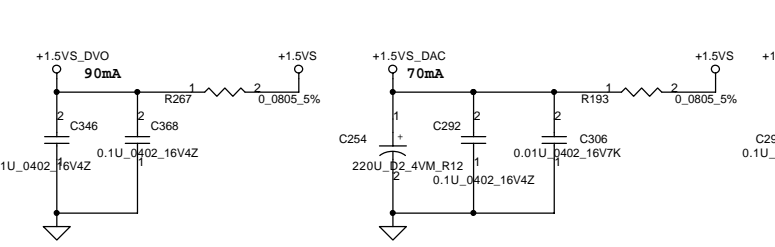
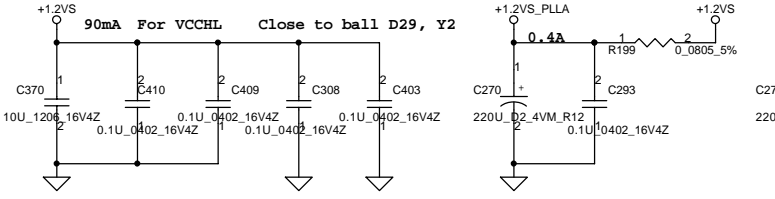
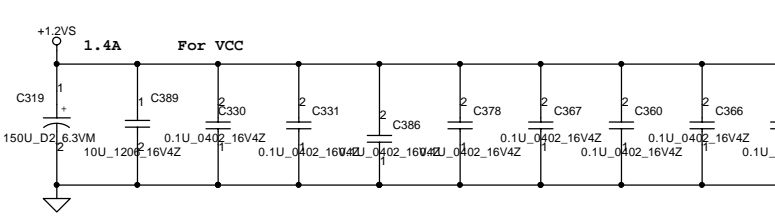
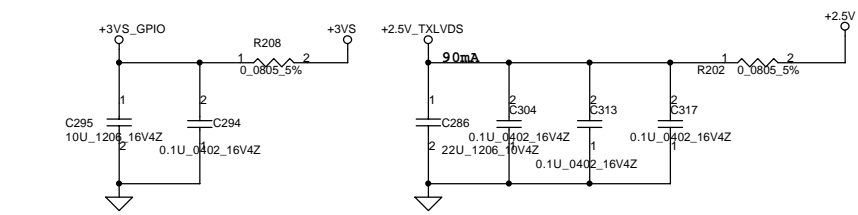
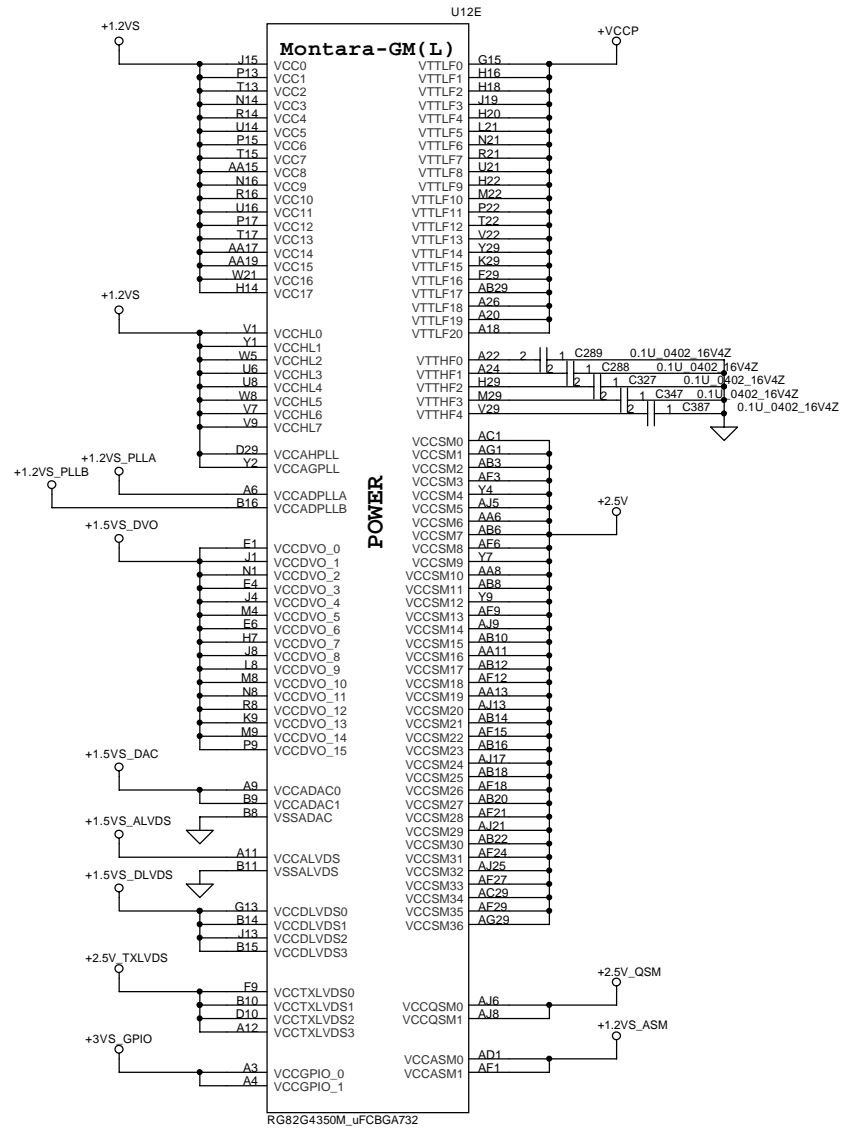
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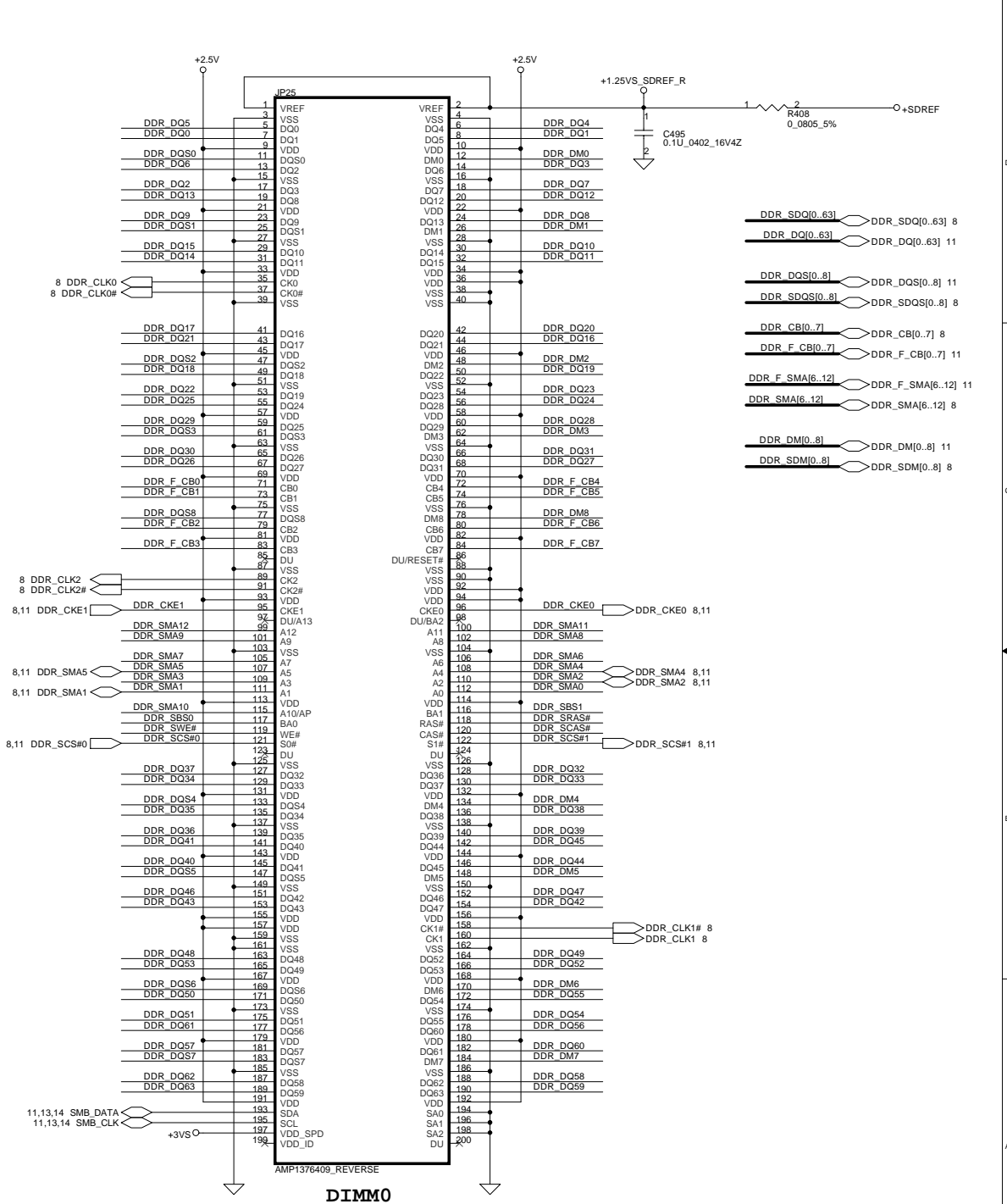
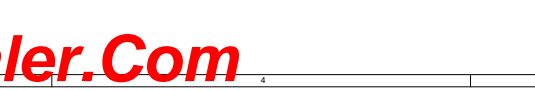
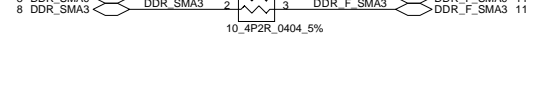
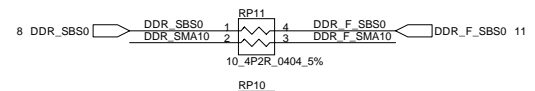
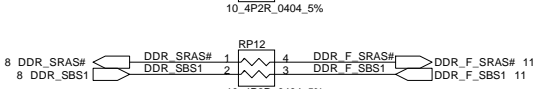
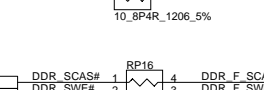
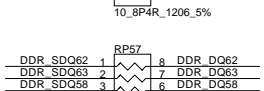
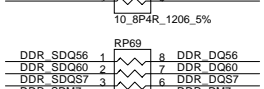
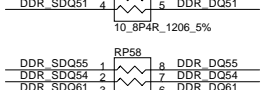
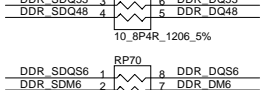
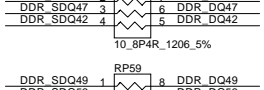
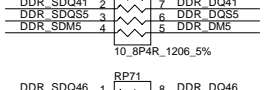
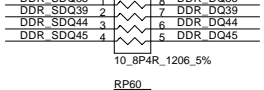
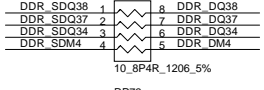
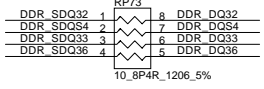
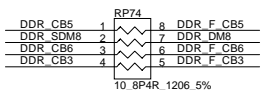
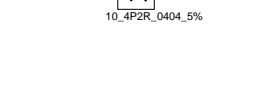
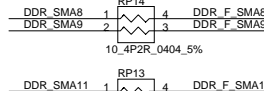
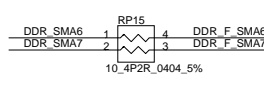
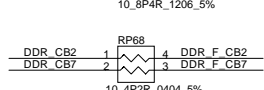
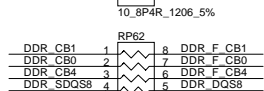
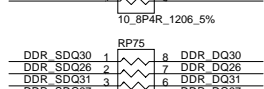
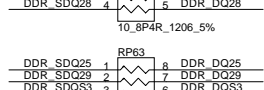
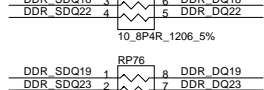
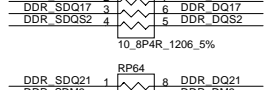
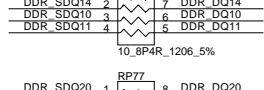
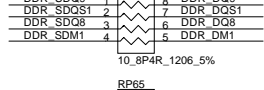
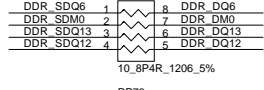
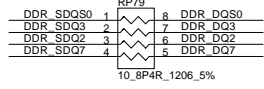
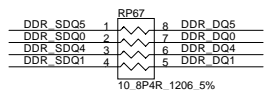
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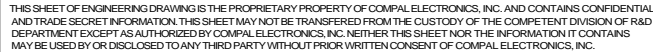
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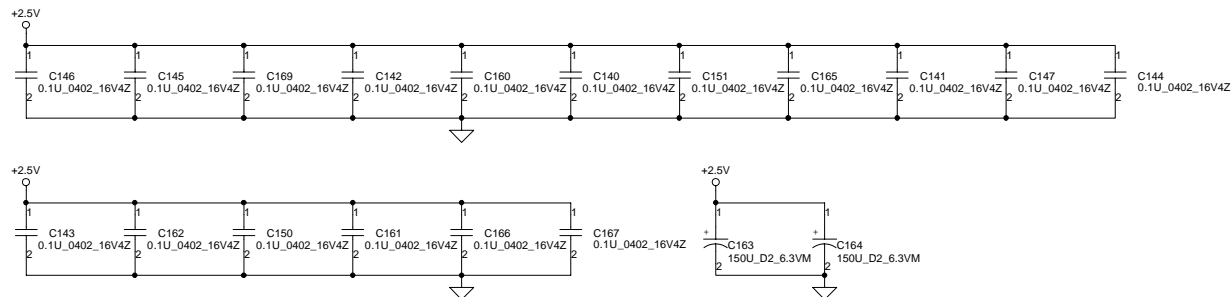


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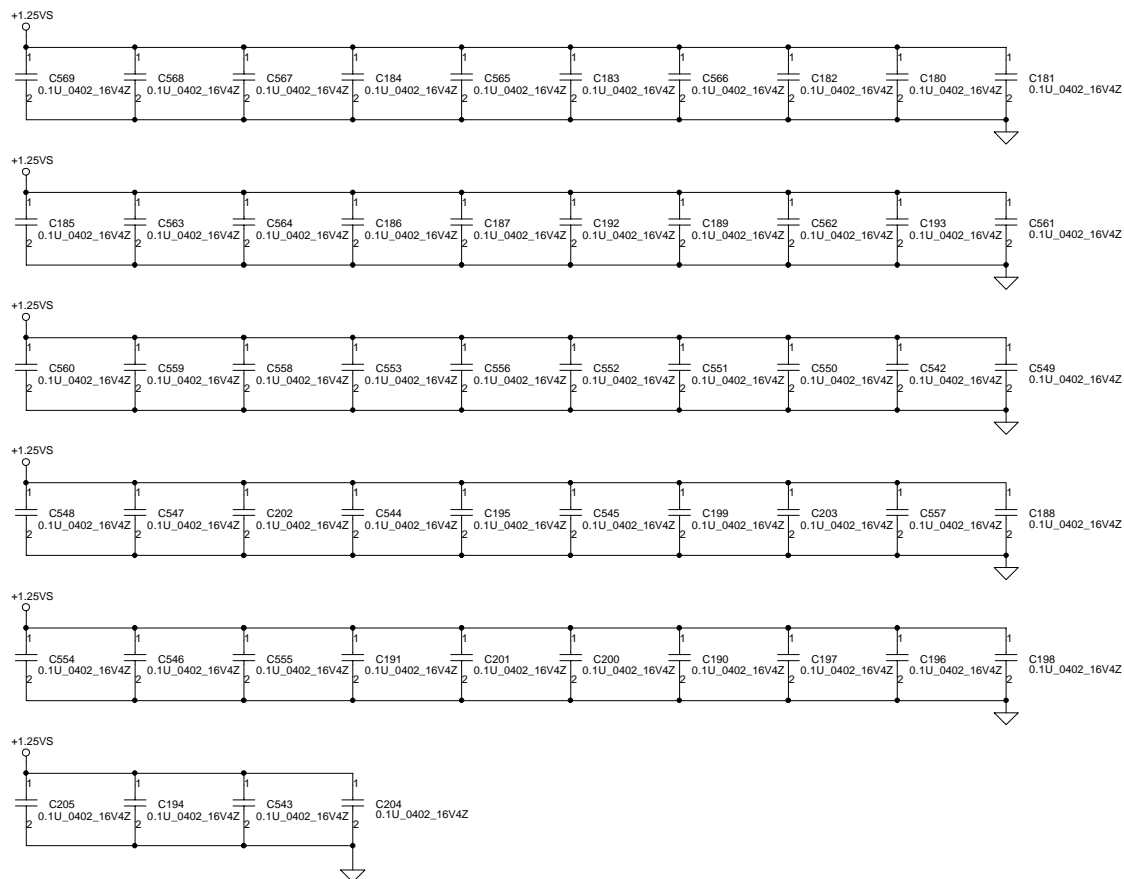
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Layout note :
Distribute as close as possible
to DDR-SODIMM.



Layout note :
Place one cap close to every 2 pull up resistors termination to
+1.25V



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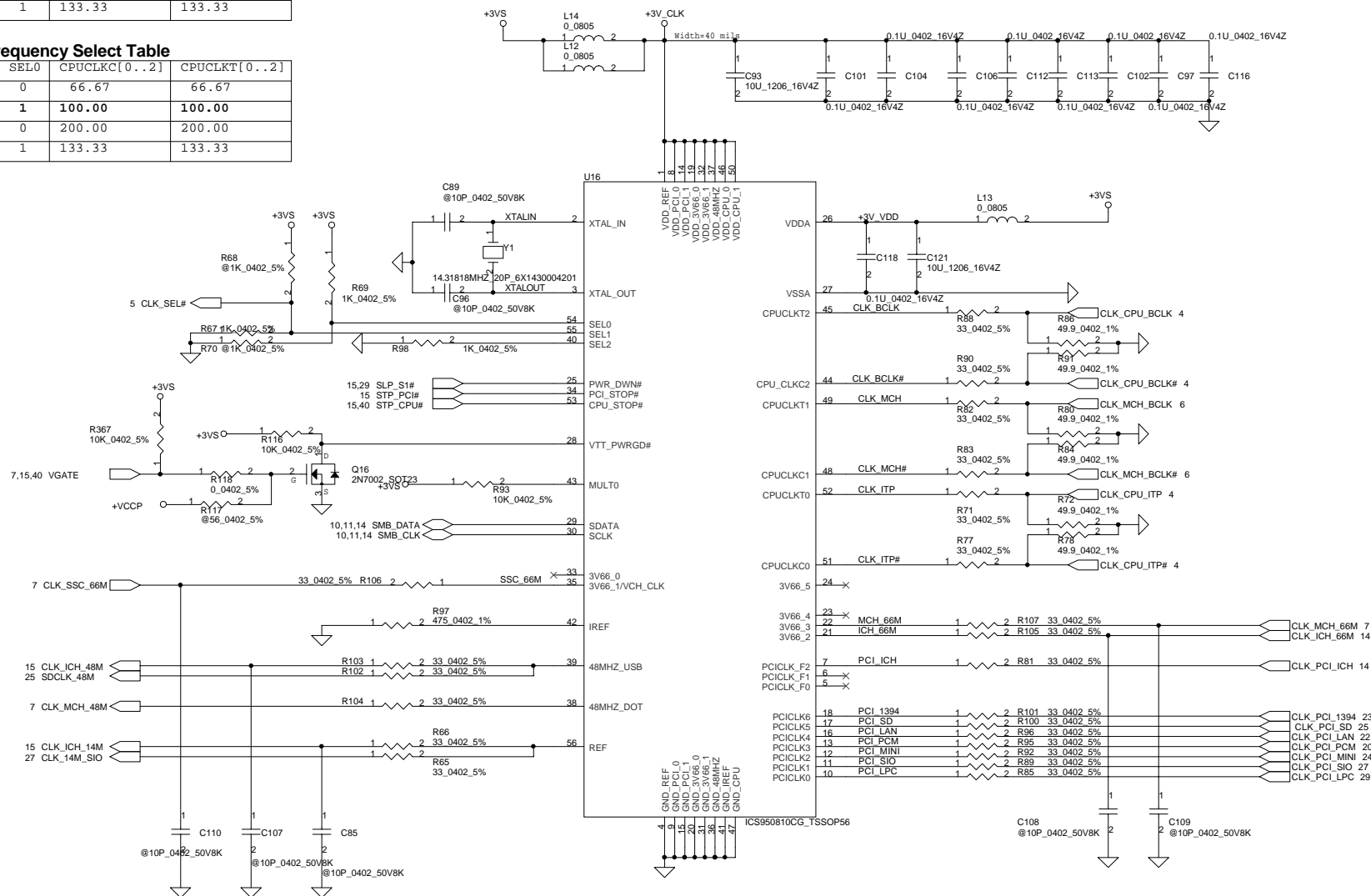
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Clock Generator

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	166.67	166.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

Clock Generator

SEL2	SEL1	SEL0	CPUCLKC[0..2]	CPUCLKT[0..2]
0	0	0	66.67	66.67
0	0	1	100.00	100.00
0	1	0	200.00	200.00
0	1	1	133.33	133.33

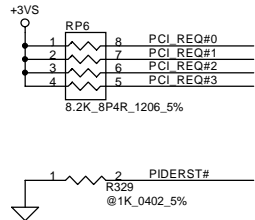
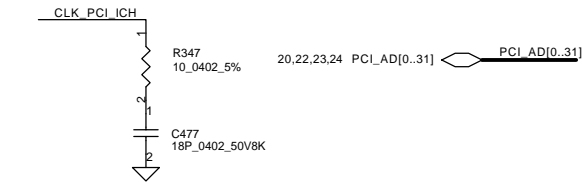


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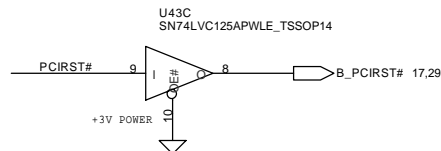
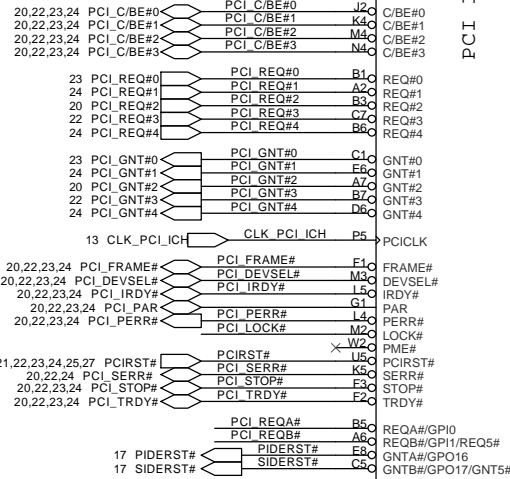
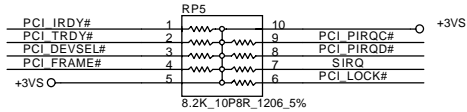
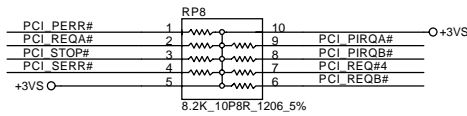
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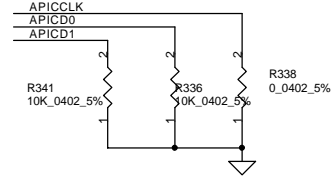
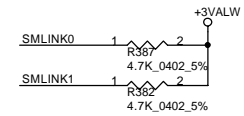
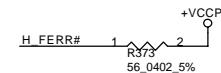
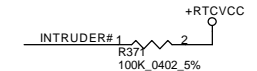
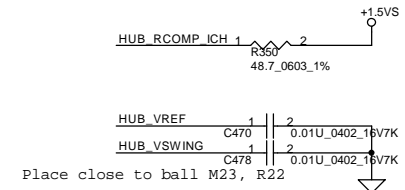
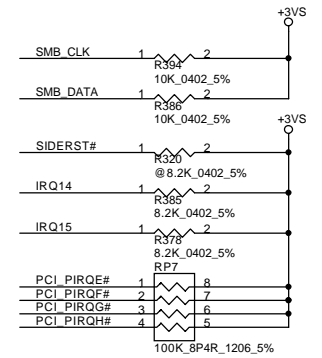
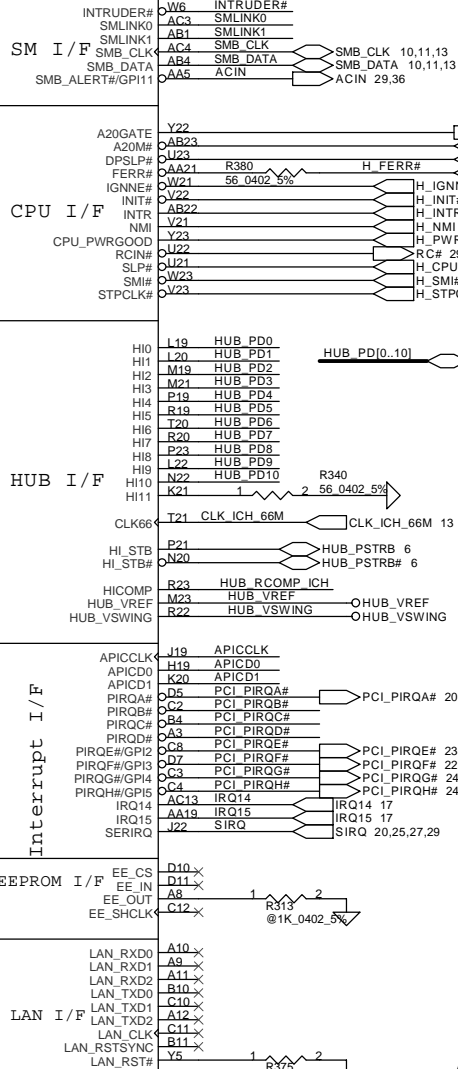
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PCI Pullups



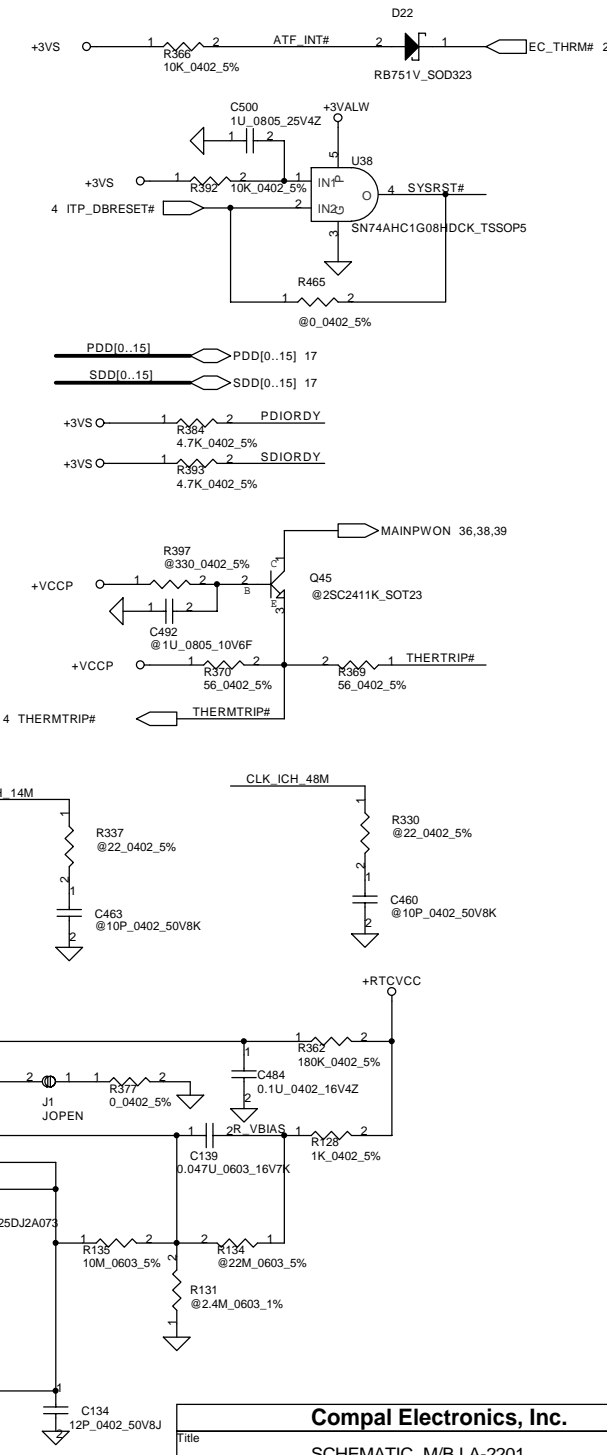
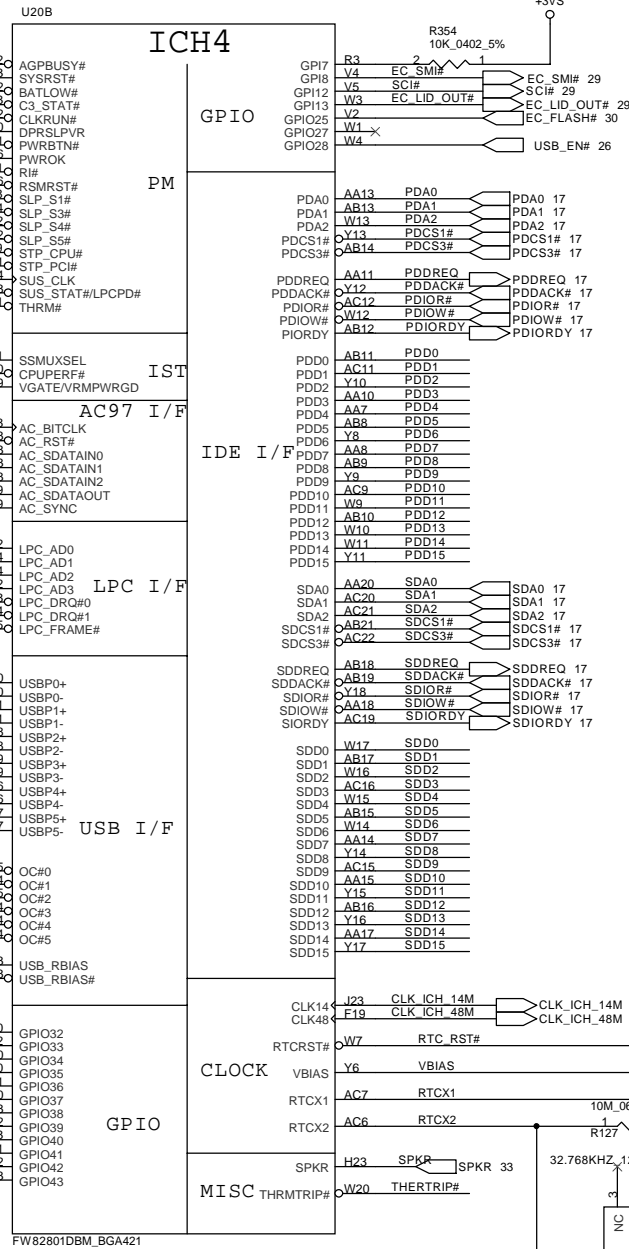
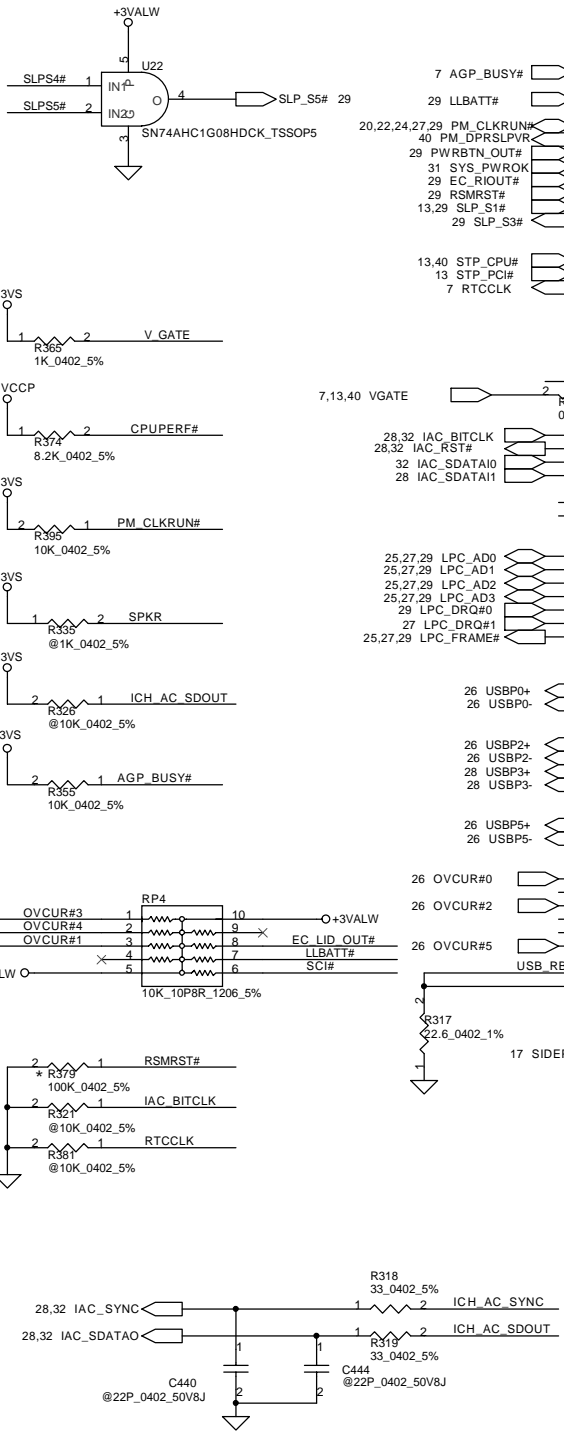
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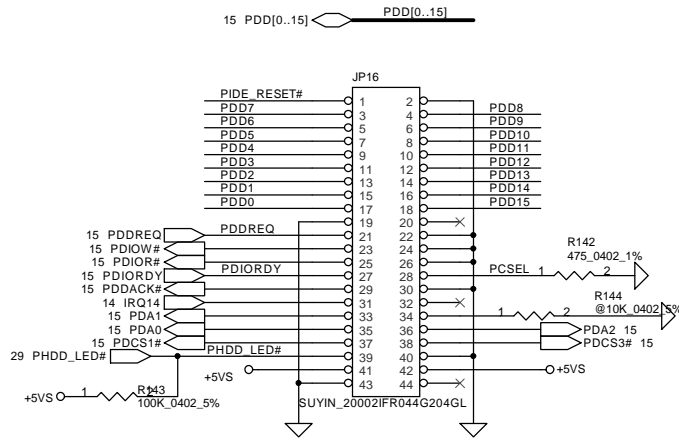
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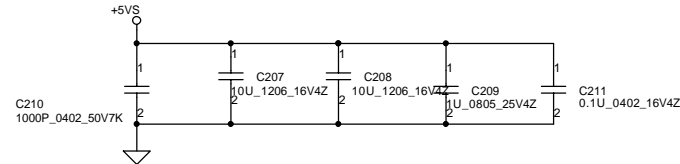
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HDD Connector

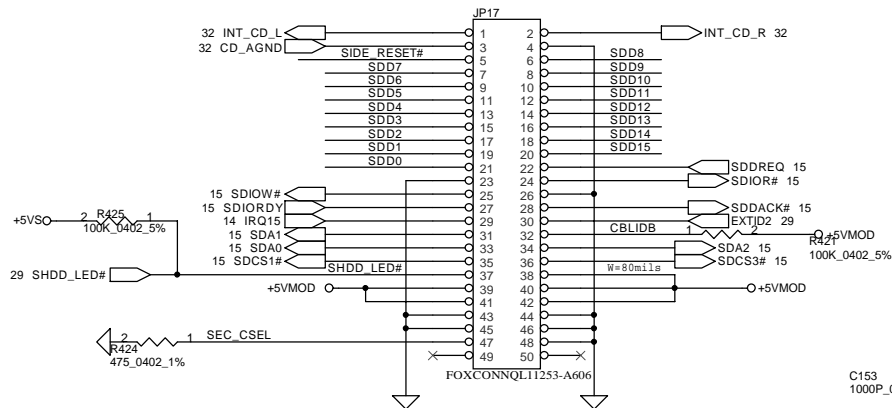


Placea caps. near HDD
CONN.

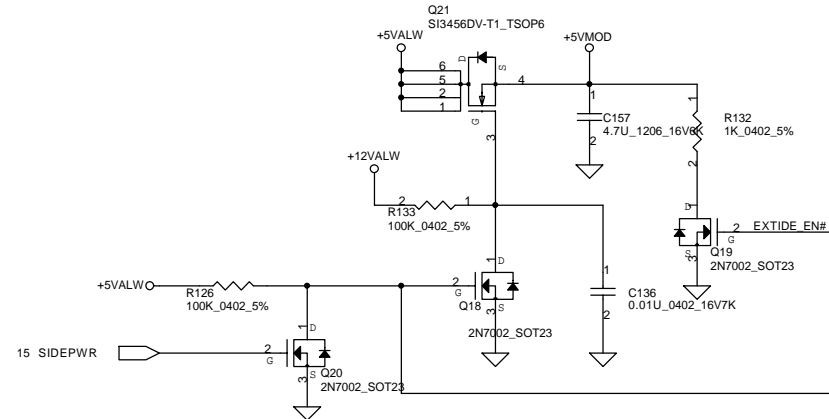
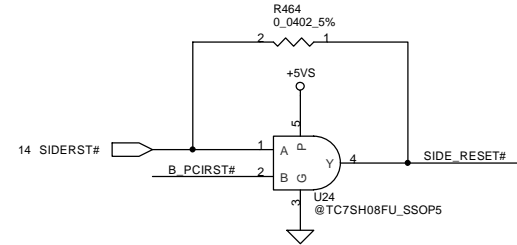
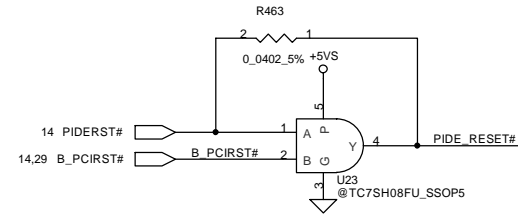
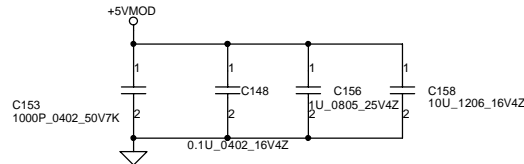


CD-ROM Connector

SDD[0..15]



Placea caps. near CDROM
CONN.



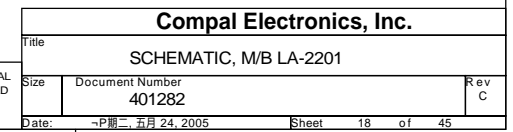
SI3456DV: N CHANNEL
VGS: 4.5V, RDS: 65 mOHM
Id(MAX): 5.1A
VGS,+20V

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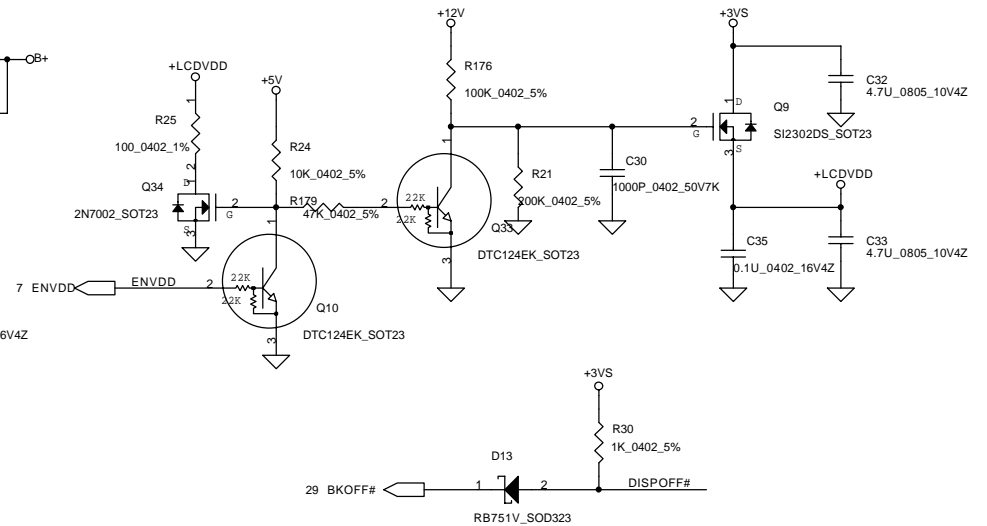
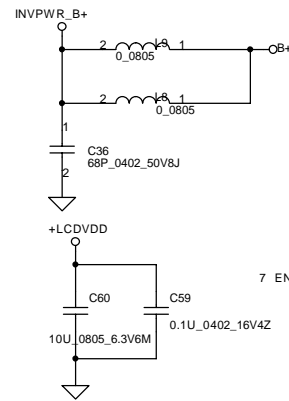
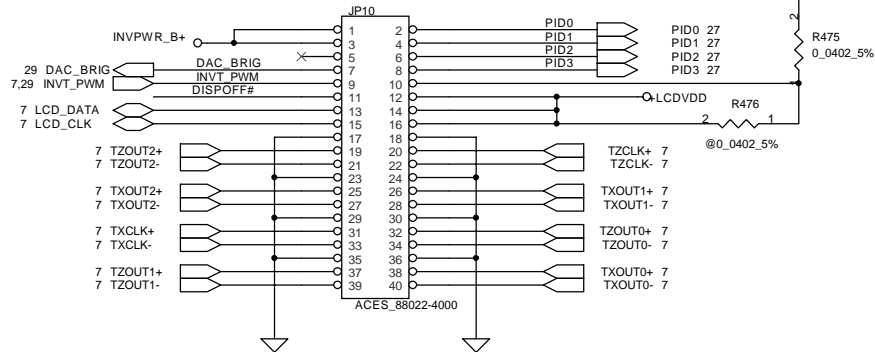
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TV Encoder

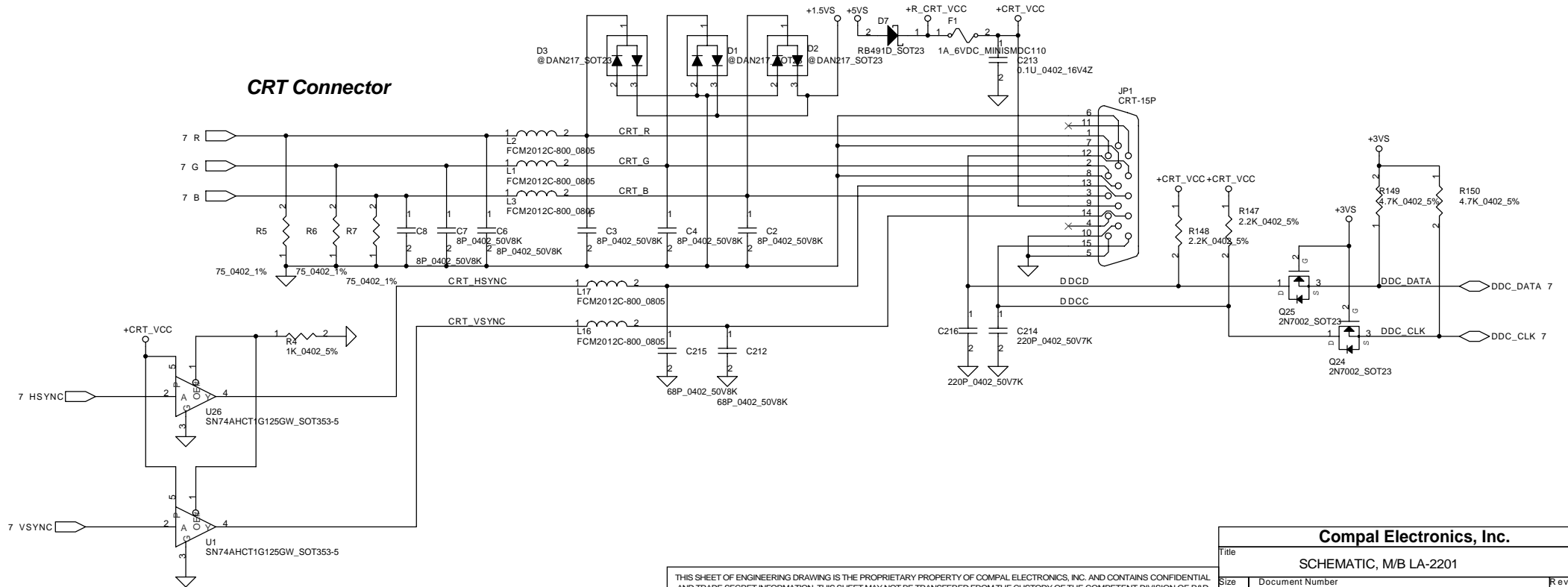


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LVDS Connector



CRT Connector



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14,22,23,24 PCI_AD[0..31] PCI_AD[0..31]

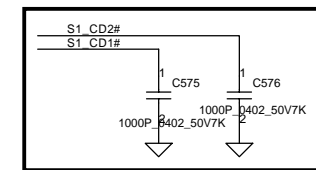
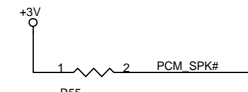
PCI_AD31	3	AD31	144	S1_D10
PCI_AD30	4	AD30	142	S1_D9
PCI_AD29	5	AD29	141	S1_D1
PCI_AD28	7	AD28	140	S1_D8
PCI_AD27	8	AD27	139	S1_D0
PCI_AD26	9	AD26	129	S1_A0
PCI_AD25	10	AD25	128	S1_A1
PCI_AD24	11	AD24	127	S1_A2
PCI_AD23	15	AD23	124	S1_A3
PCI_AD22	16	AD22	121	S1_A4
PCI_AD21	17	AD21	120	S1_A5
PCI_AD20	19	AD20	118	S1_A6
PCI_AD19	23	AD19	116	S1_A25
PCI_AD18	24	AD18	115	S1_A7
PCI_AD17	25	AD17	113	S1_A24
PCI_AD16	26	AD16	98	S1_A17
PCI_AD15	38	AD15	96	S1_IOWR#
PCI_AD14	39	AD14	97	S1_A9
PCI_AD13	40	AD13	93	S1_IORD#
PCI_AD12	41	AD12	95	S1_A11
PCI_AD11	42	AD11	92	S1_OE#
PCI_AD10	45	AD10	91	S1_OE# 21
PCI_AD9	46	AD9	89	S1_A10
PCI_AD8	47	AD8	87	S1_D15
PCI_AD7	49	AD7	85	S1_D7
PCI_AD6	51	AD6	82	S1_D13
PCI_AD5	53	AD5	83	S1_D6
PCI_AD4	53	AD4	80	S1_D12
PCI_AD3	54	AD3	81	S1_D5
PCI_AD2	55	AD2	77	S1_D11
PCI_AD1	56	AD1	79	S1_D4
PCI_AD0	57	AD0	76	S1_D3

PQFP 144
22.2 X 22.2 X 1.60

14,22,23,24 PCI_C/BE#3	12	C/BE#3
14,22,23,24 PCI_C/BE#2	27	C/BE#2
14,22,23,24 PCI_C/BE#1	37	C/BE#1
14,22,23,24 PCI_C/BE#0	48	C/BE#0
7,14,18,21,22,23,24,25,27 PCIRST#	20	RST#
14,22,23,24 PCI_FRAME#	28	FRAME#
14,22,23,24 PCI_IRDY#	29	IRDY#
14,22,23,24 PCI_TRDY#	31	TRDY#
14,22,23,24 PCI_DEVSEL#	32	DEVSEL#
14,22,23,24 PCI_STOP#	33	STOP#
14,22,23,24 PCI_PERR#	34	PERR#
14,22,24 PCI_SERR#	35	SERR#
14,22,23,24 PCI_PAR#	36	PAR#
14 PCI_REQ#2	1	REQ#
14 PCI_GNT#2	2	GNT#
13 CLK_PCI_PCM	21	CLK

CC/BE3#/REG#	125	S1_REG#
CC/BE2#/A12	112	S1_A12
CC/BE1#/A8	99	S1_A8
CC/BE0#/CE1#	88	S1_CE1#
CRST#/RESET	119	S1_RST
CFRAME#/A23	111	S1_A23
CIRDY#/A15	110	S1_A15
CTRDY#/A22	109	S1_A22
CDEVSEL#/A21	107	S1_A21
CSTOP#/A20	105	S1_A20
CPERR#/A14	104	S1_A14
CSERR#/WAIT#	133	S1_WAIT#
CPAR#/A13	101	S1_A13
CREQ#/INPACK#	106	S1_INPACK#
CGNT#/WE#	108	S1_WE#
CLK/A16	108	A16 CLK
CSTSCHG/BVD1	135	S1_BVD1
CLKRUN#/WP	136	S1_WP
CBLOCK#/A19	103	S1_A19
CINT#/READY	132	S1_RDY#
SPKOUT	62	PCM_SPK#
CAUDIO/BVD2	134	S1_BVD2
CCD2#/CD2#	137	S1_CD2#
CCD1#/CD1#	125	S1_CD1#
CVS2/VS2#	117	S1_VS2
CVS1/VS1#	131	S1_VS1

S1_A[0..25] S1_A[0..25] 21
S1_D[0..15] S1_D[0..15] 21



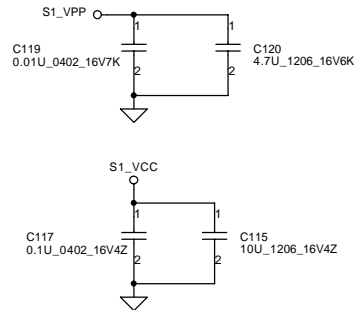
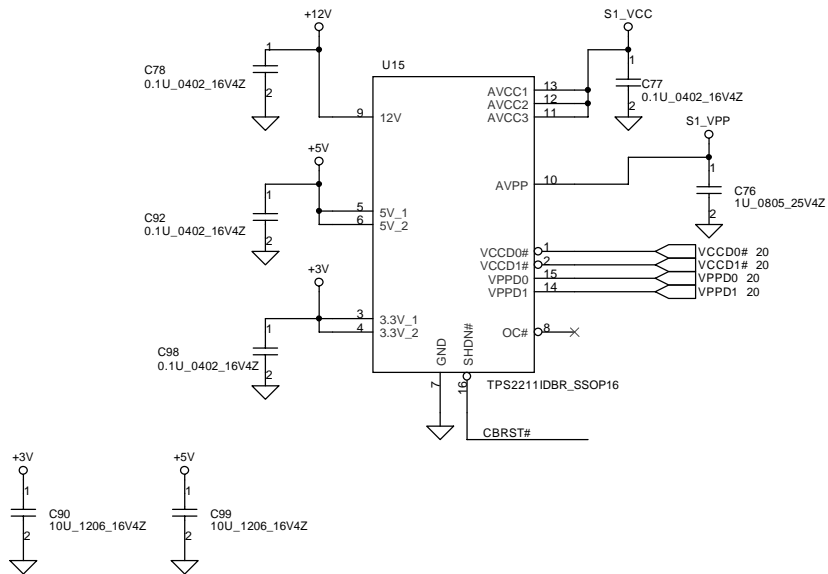
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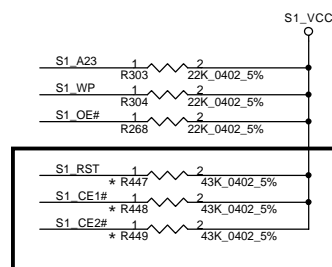
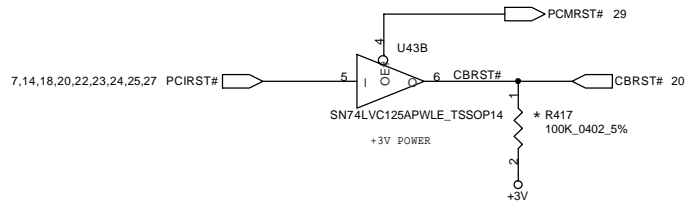
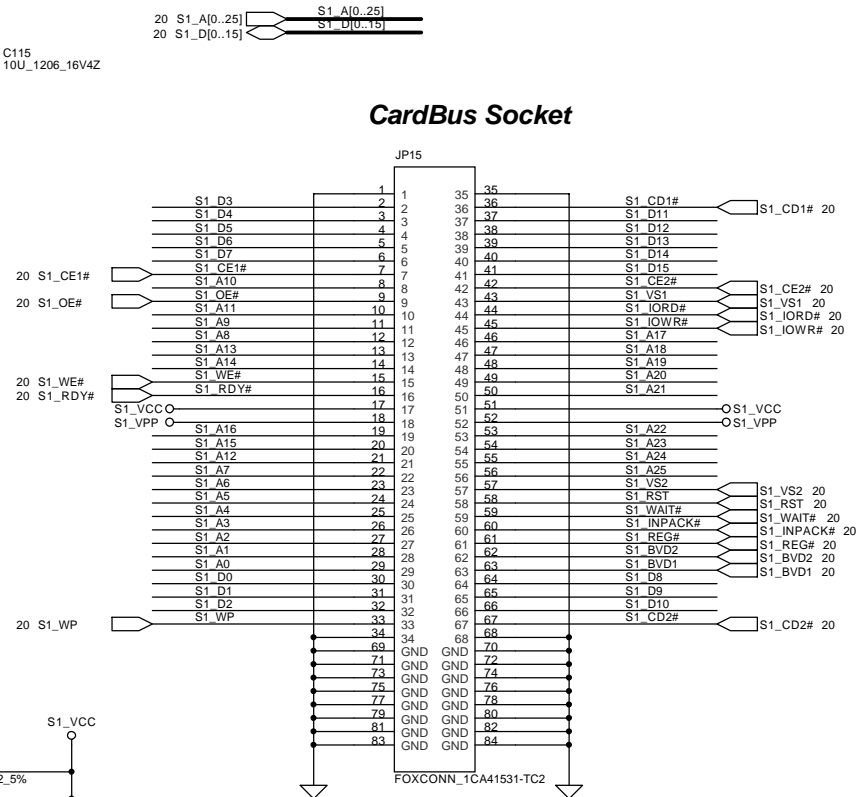
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PCMCIA Power Controller



CardBus Socket

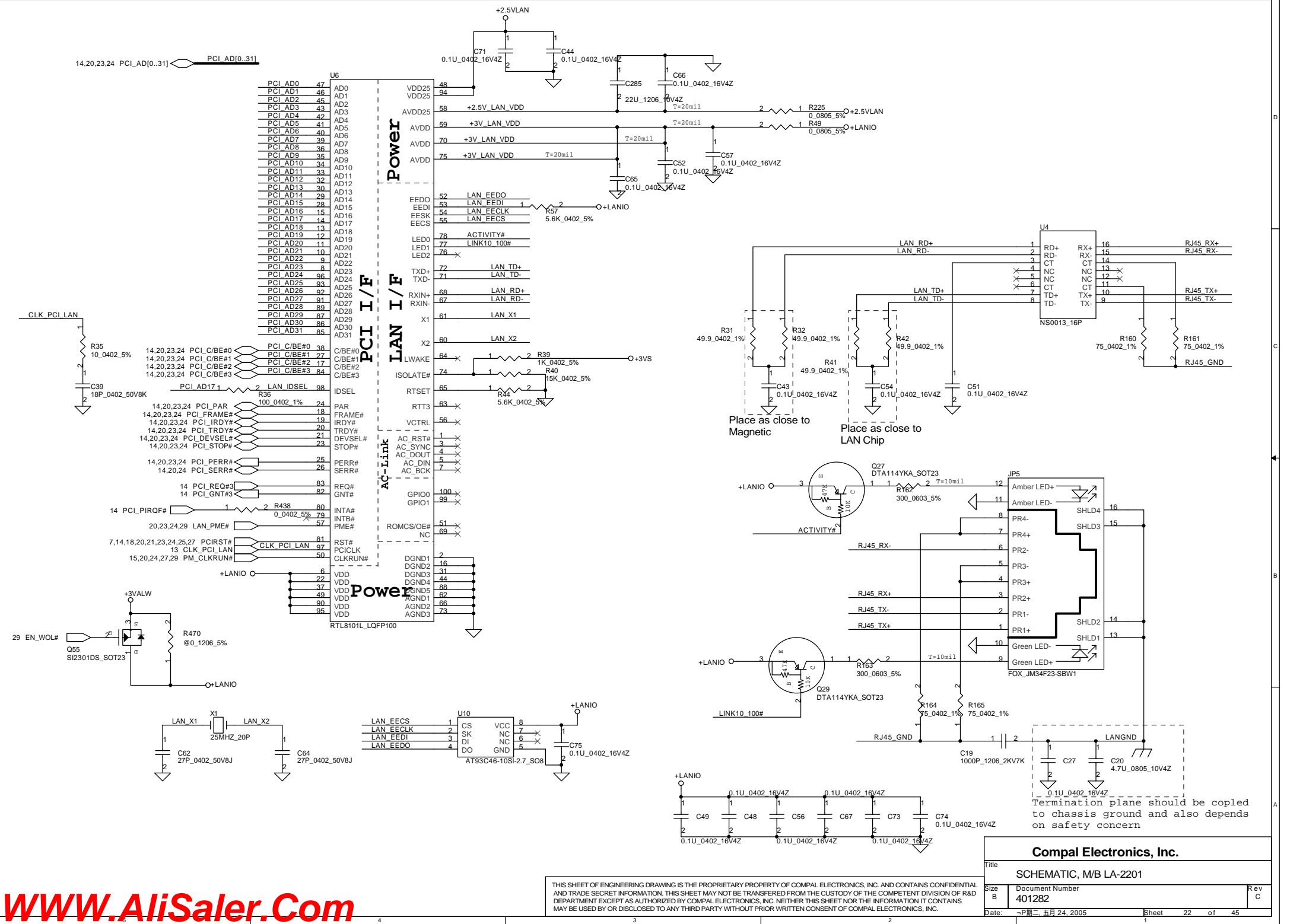


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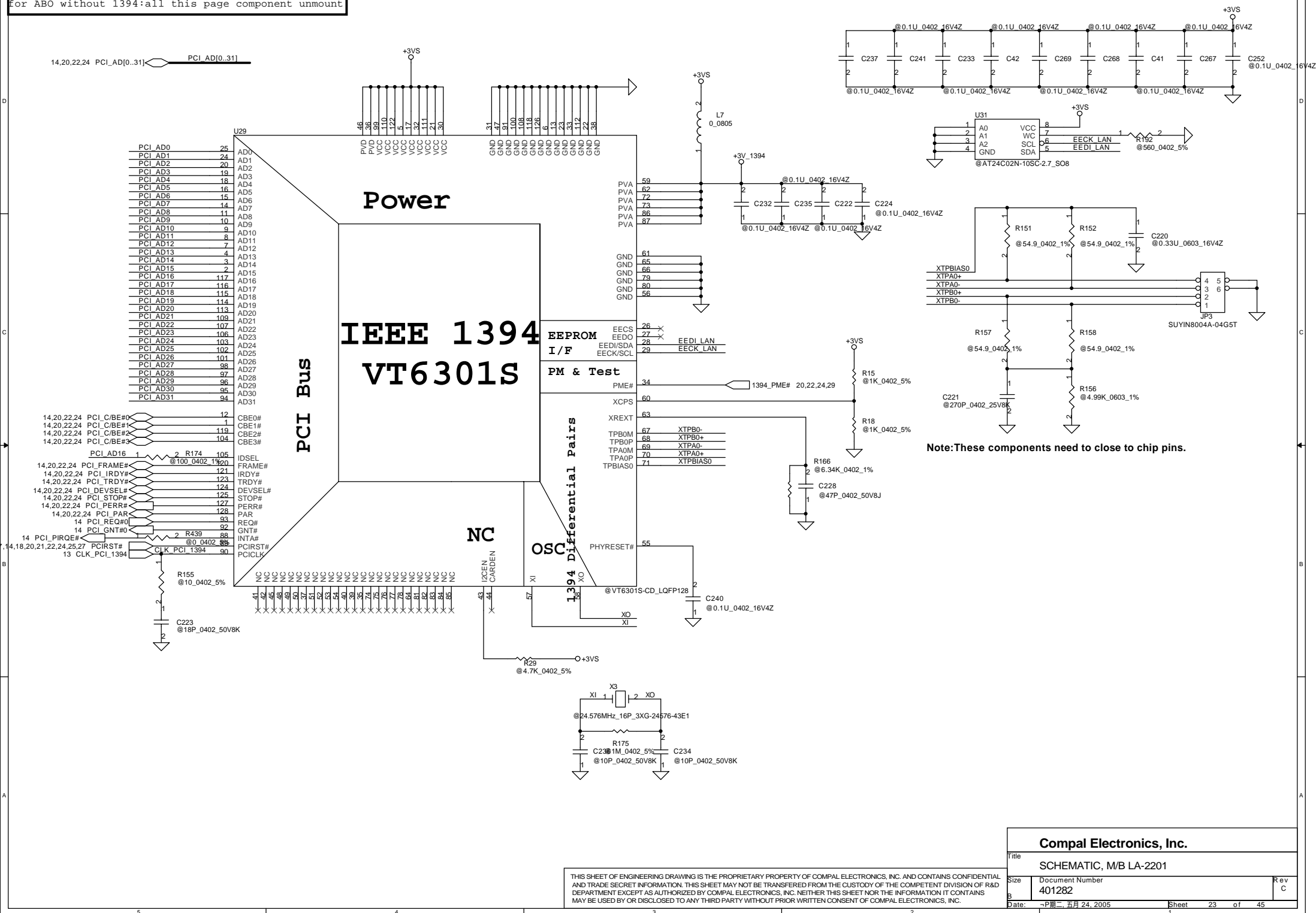
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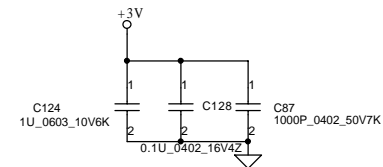
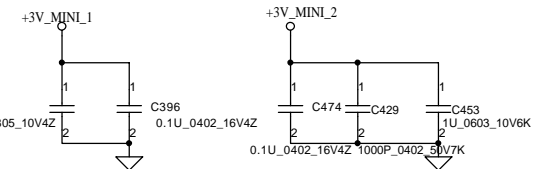
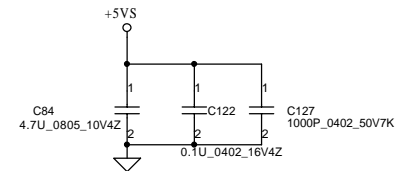
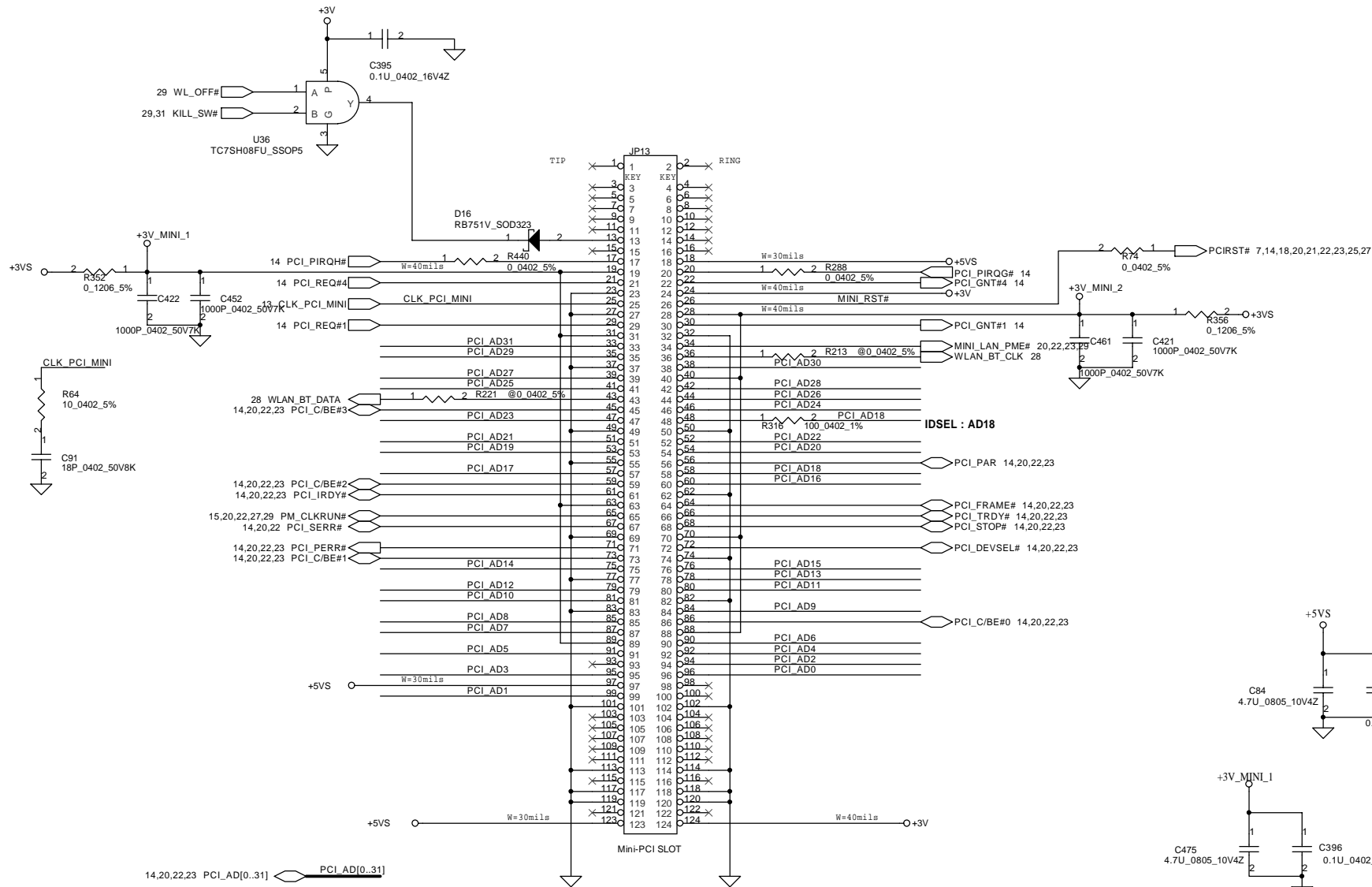
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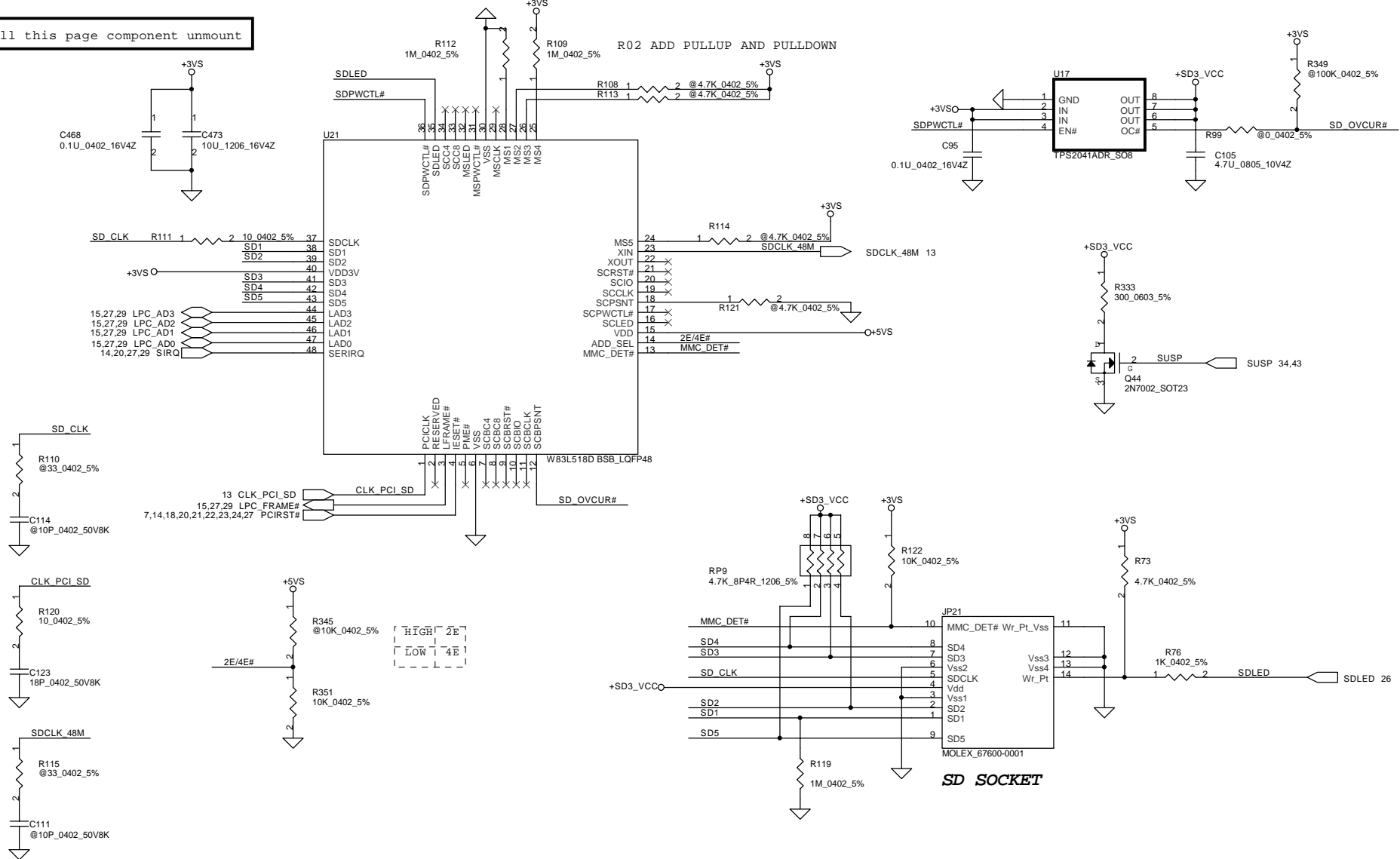
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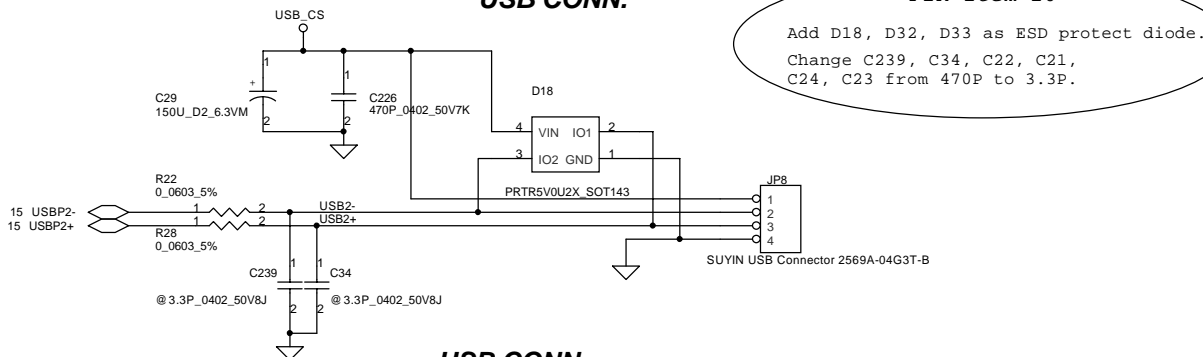
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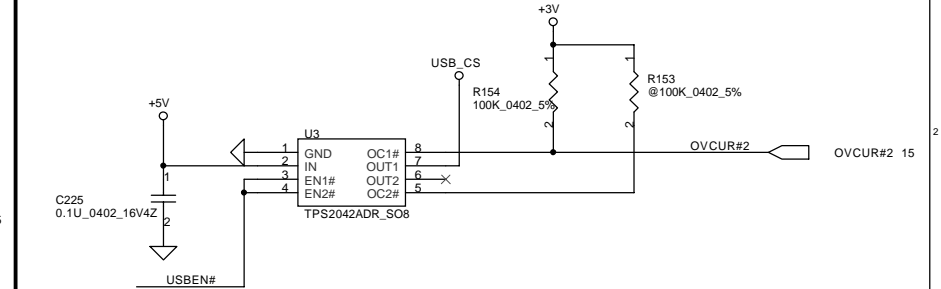
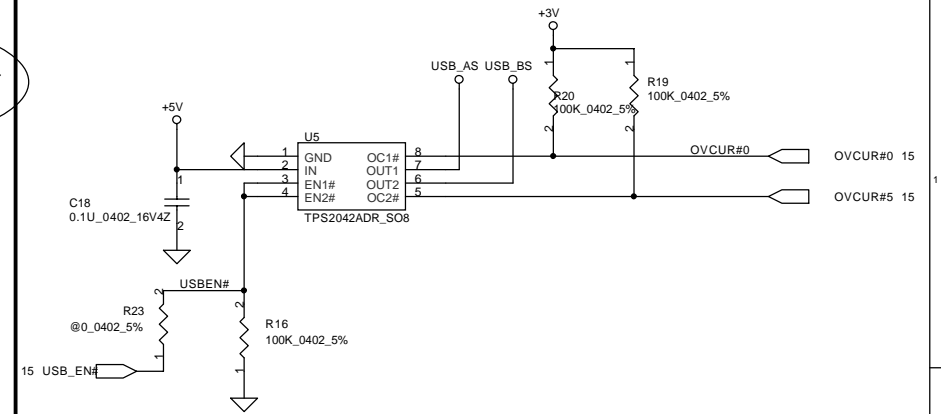
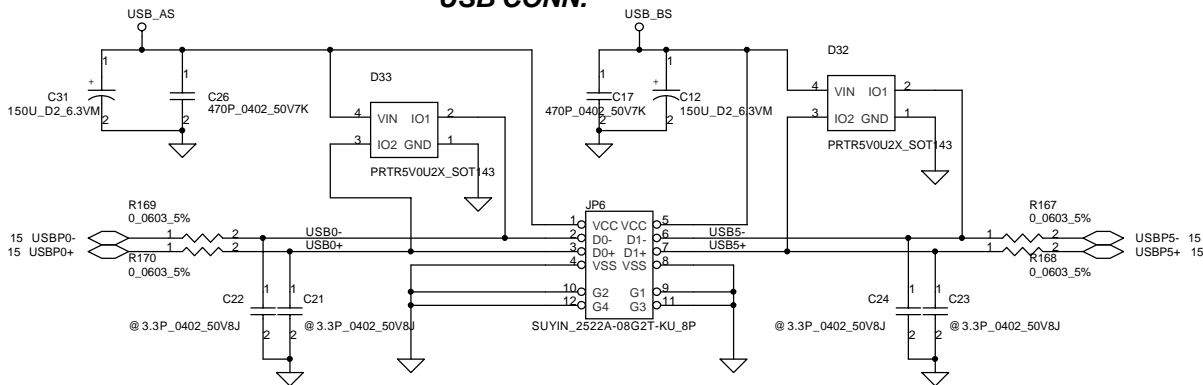
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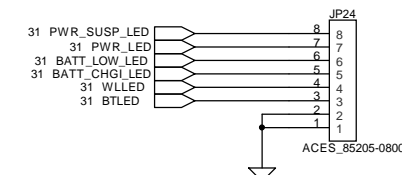
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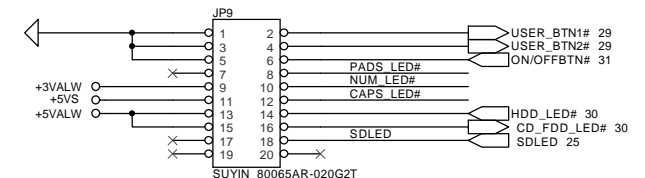
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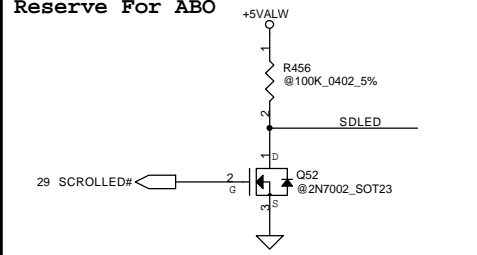
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POWER/B CONN.



Reserve For ABO

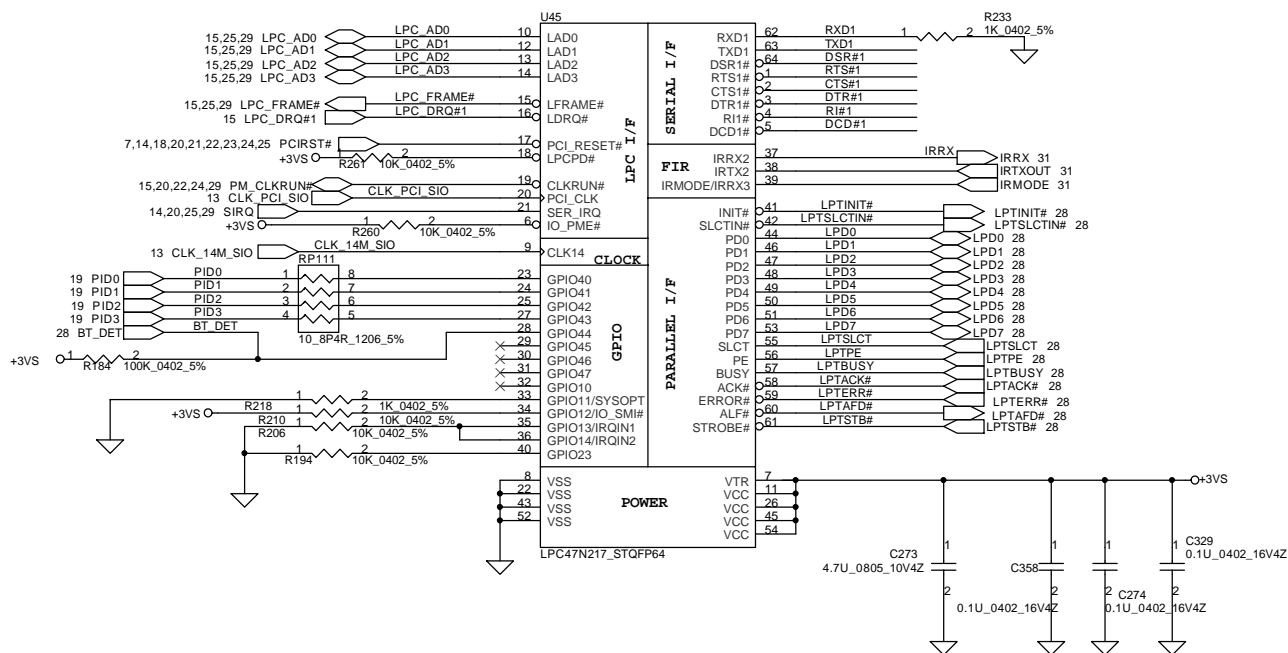


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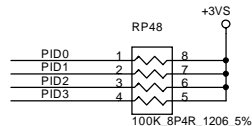
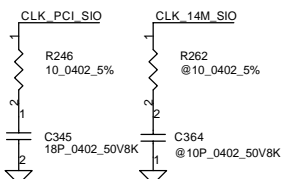
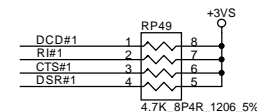
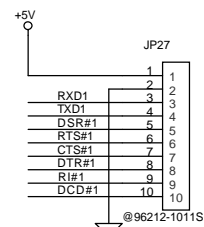
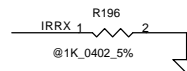
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SUPER I/O SMsC FDC47N227



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Base I/O Address
* 0 = 02Eh
  1 = 04Eh
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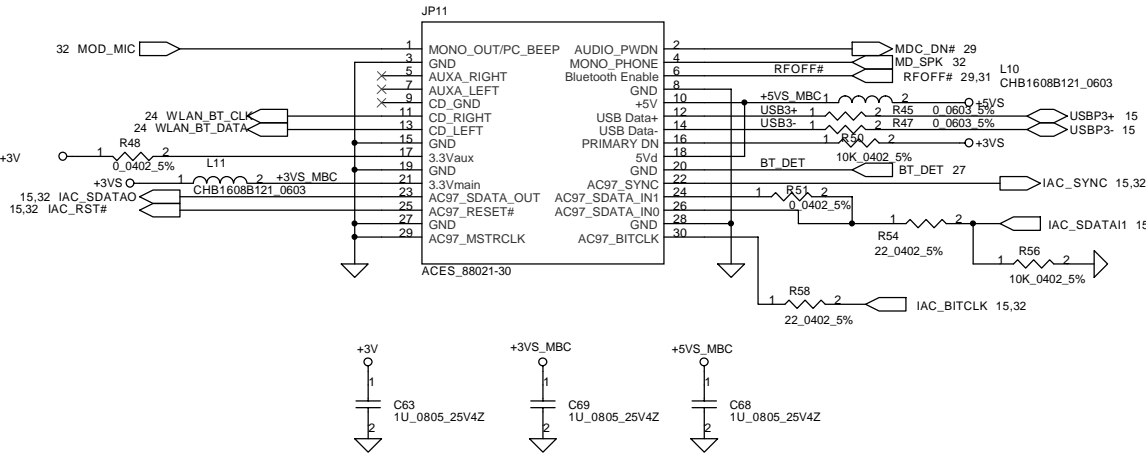
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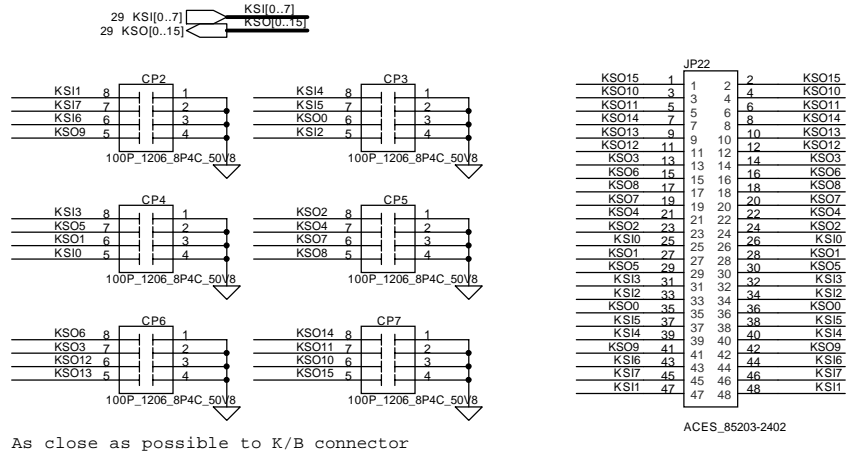
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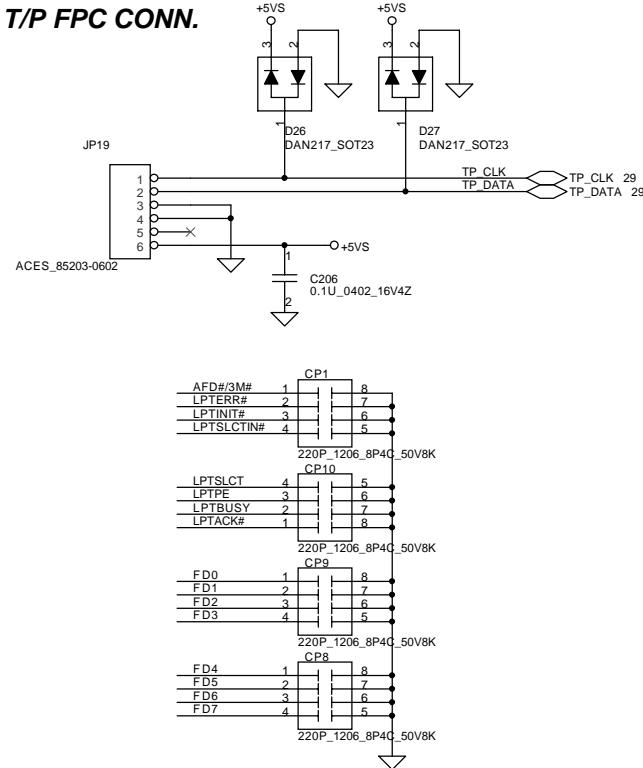
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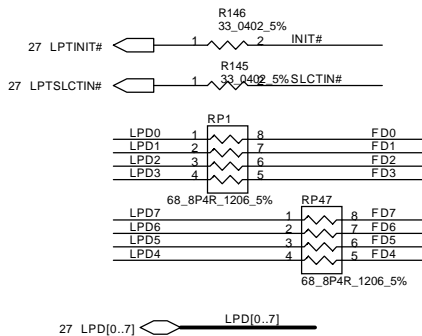
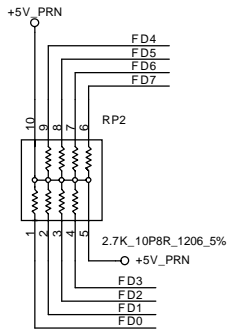
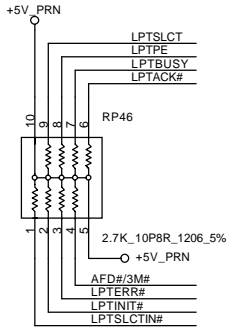
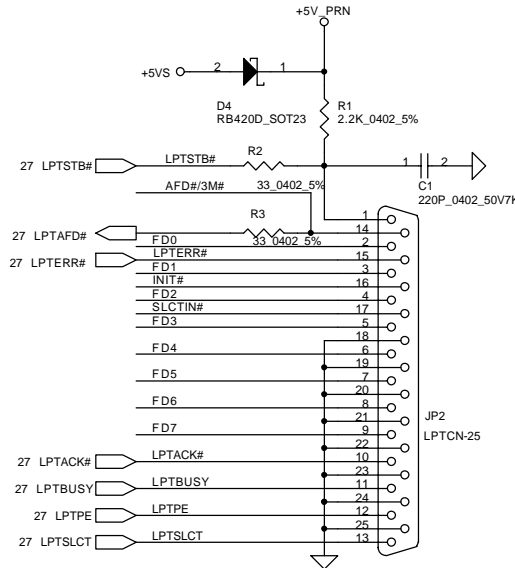
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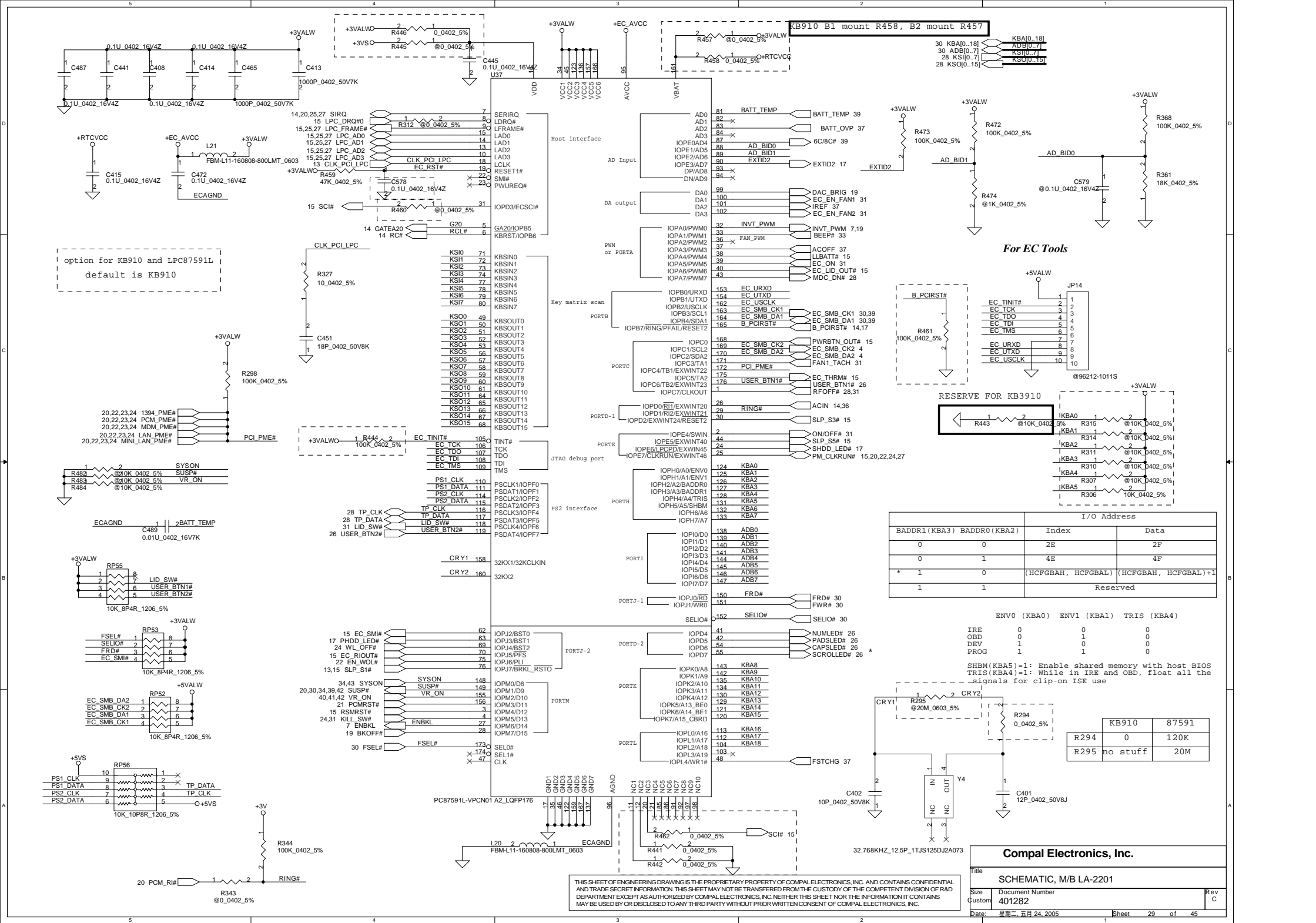


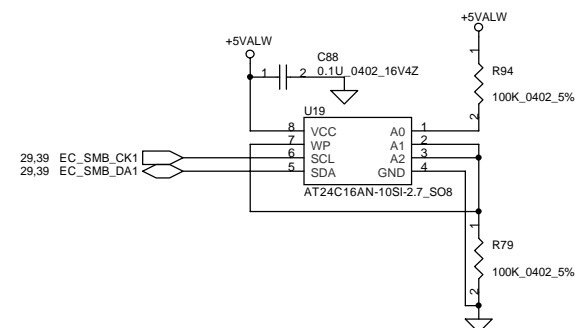
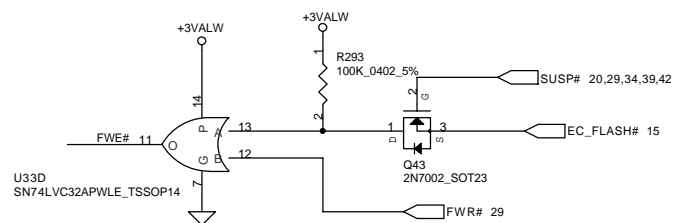
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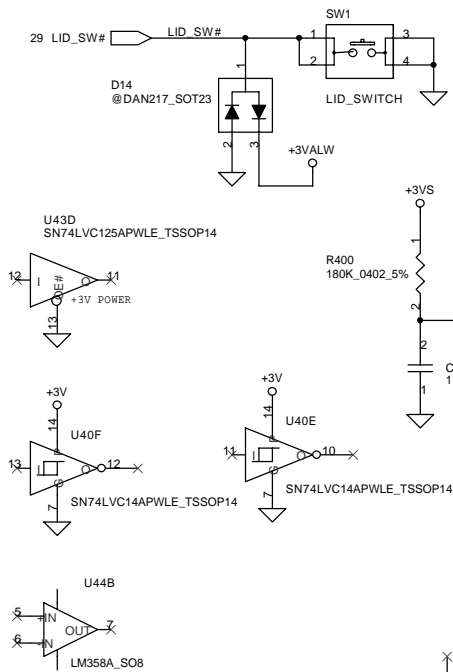
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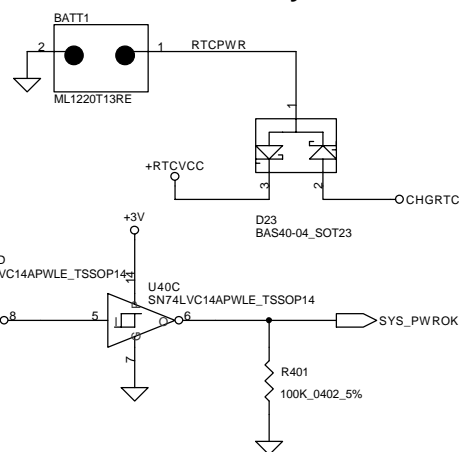




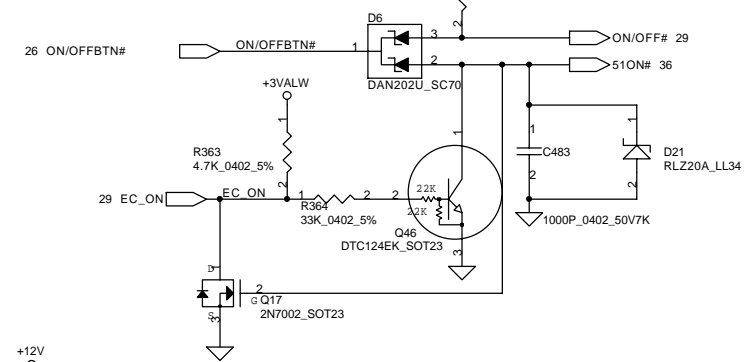
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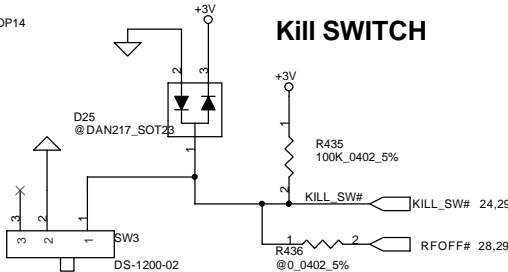
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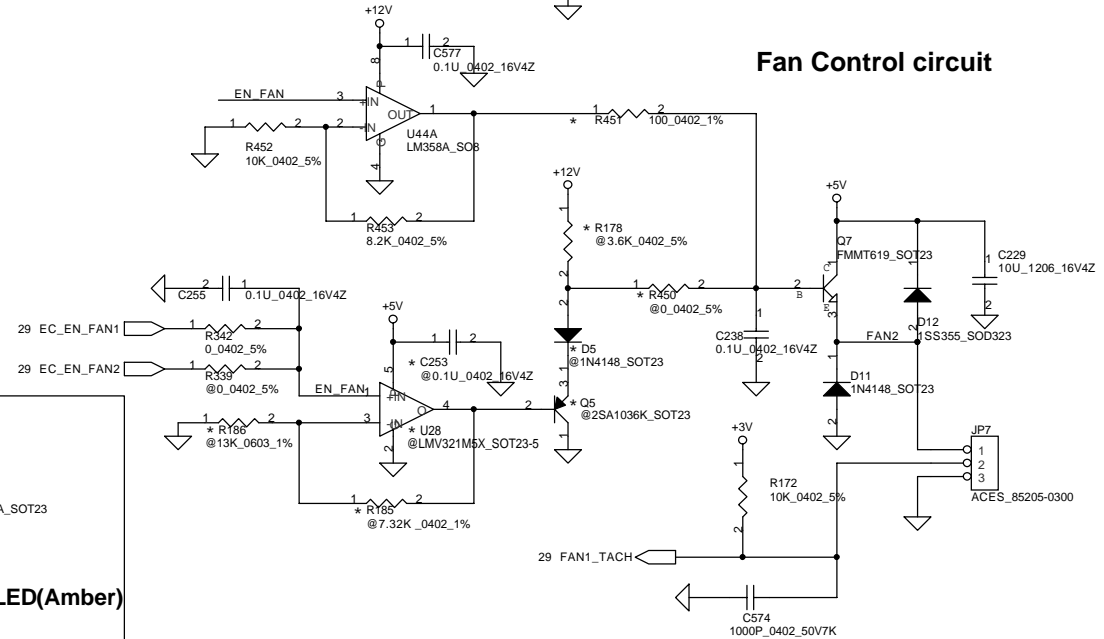
Power BTN



Kill SWITCH



Fan Control circuit

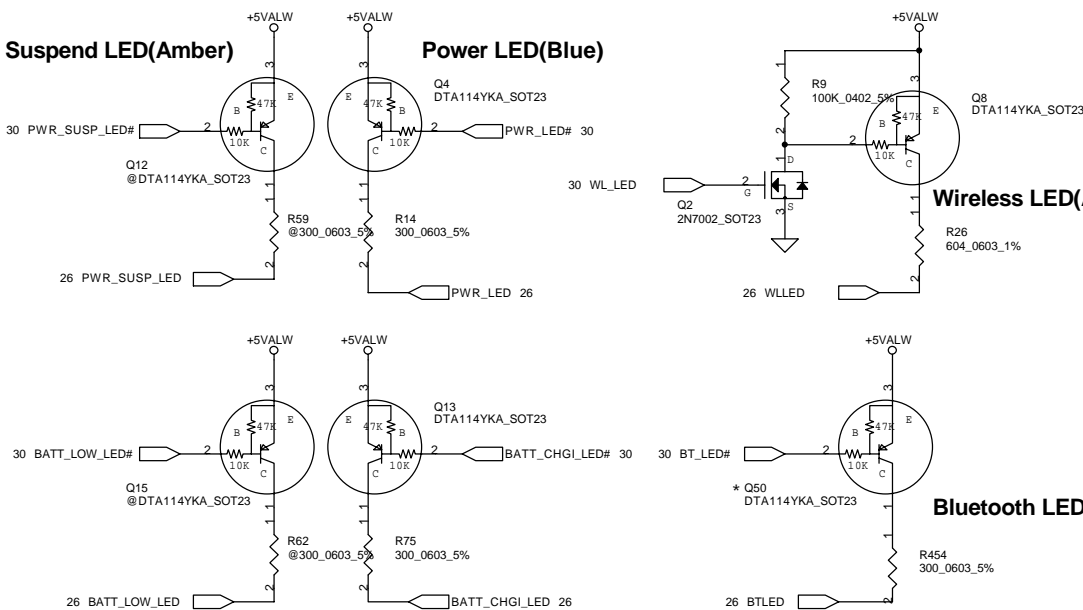


Suspend LED(Amber)

Power LED(Blue)

Wireless LED(Amber)

Bluetooth LED(Blue)

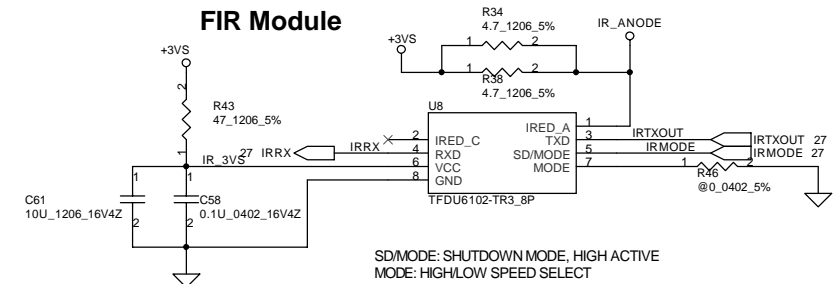


BATT Low LED(Amber)

BATT Charge LED(Blue)

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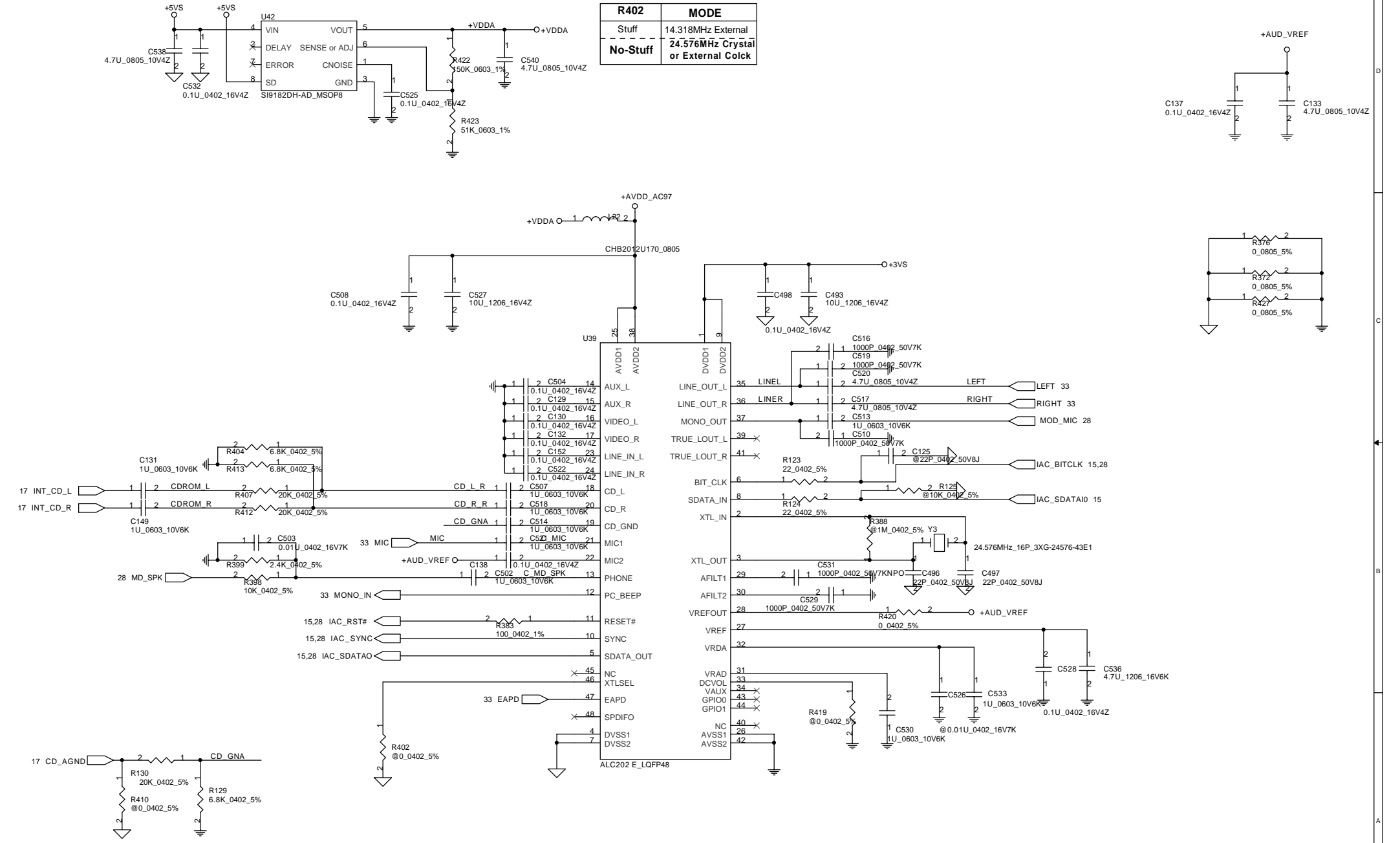
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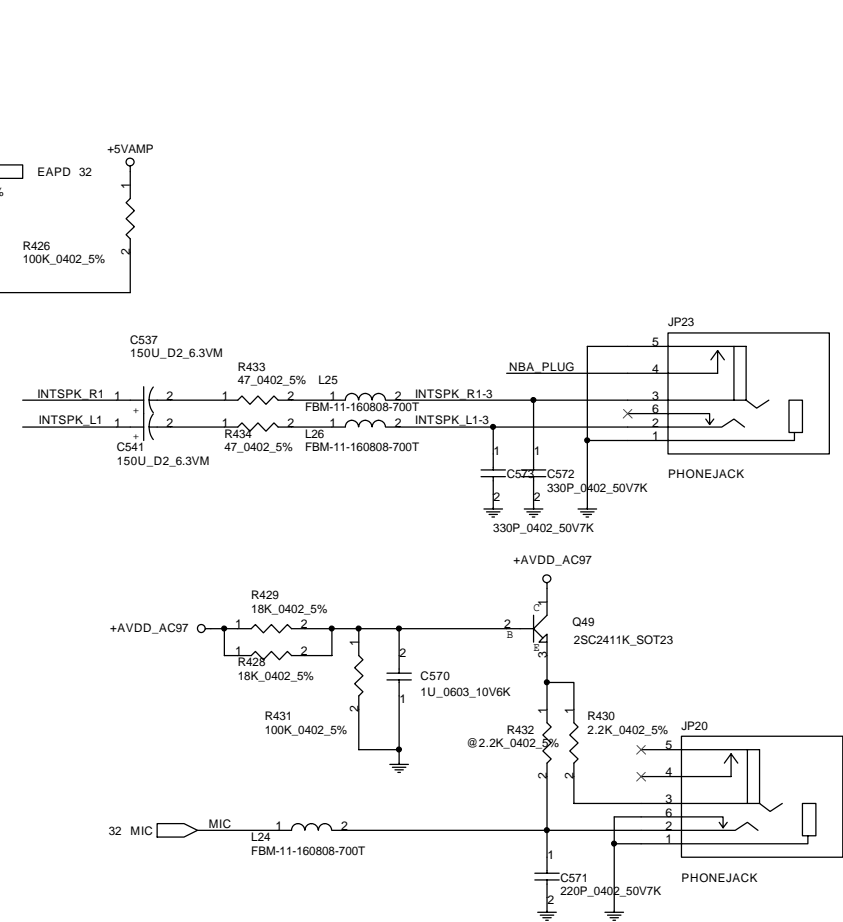
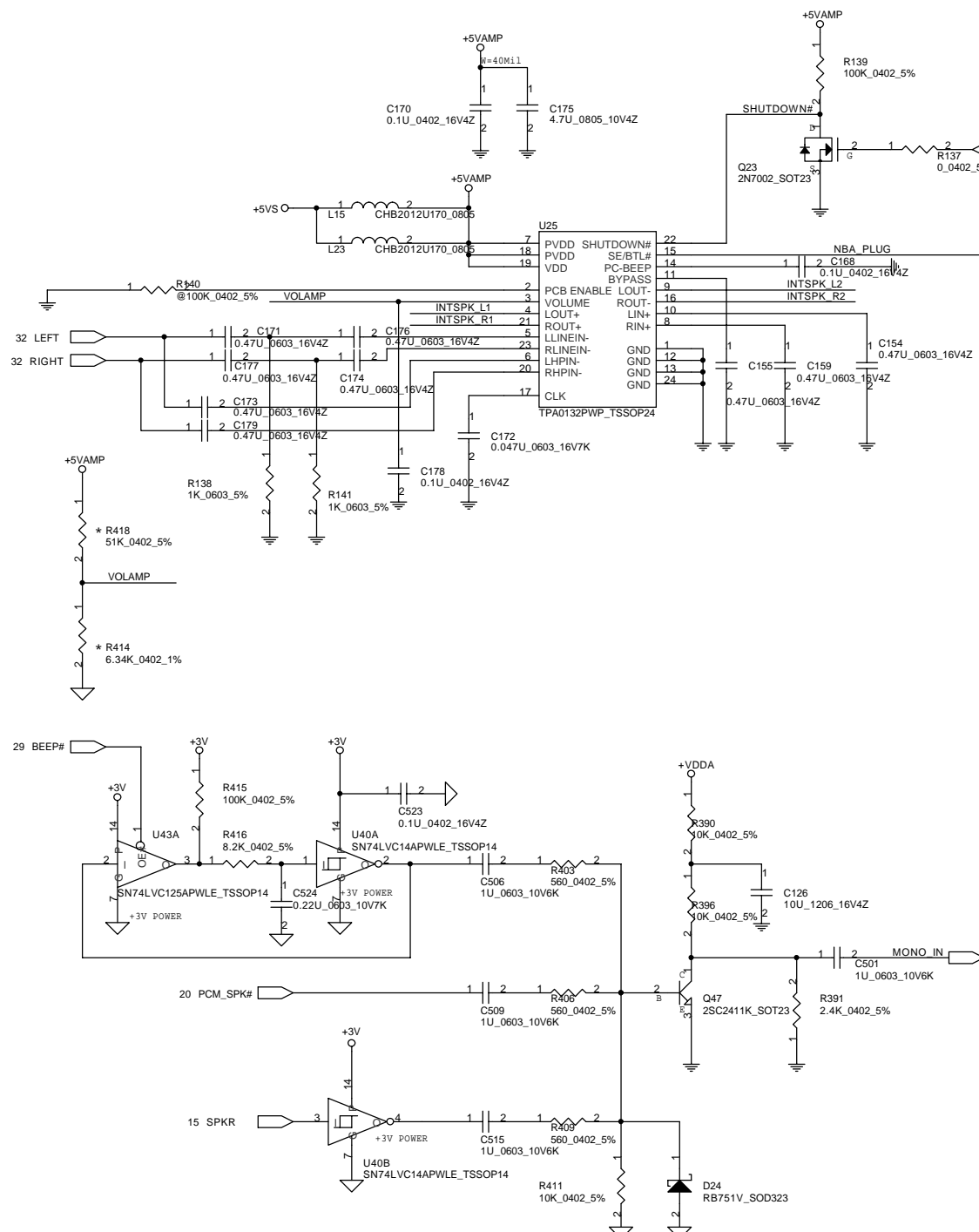
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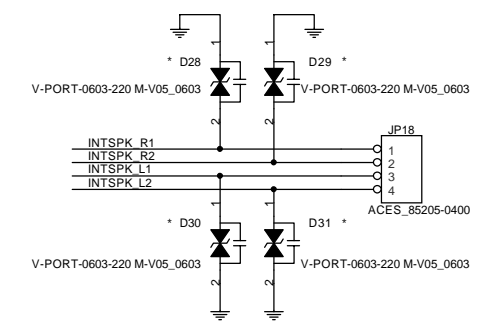
AC97 Codec



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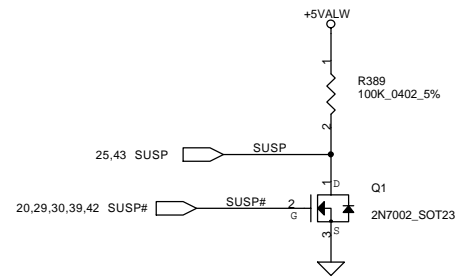
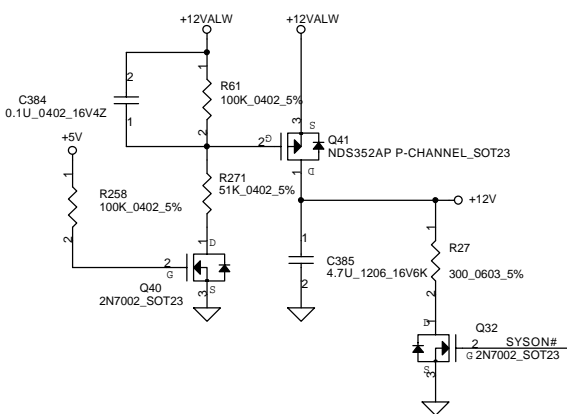
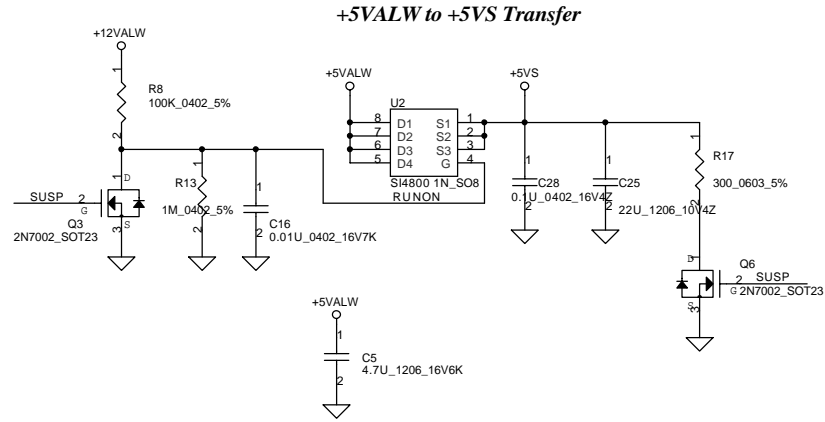
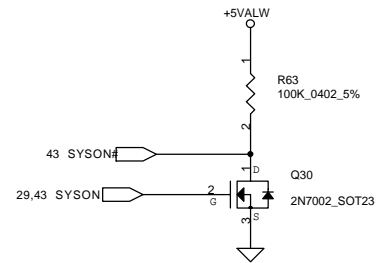
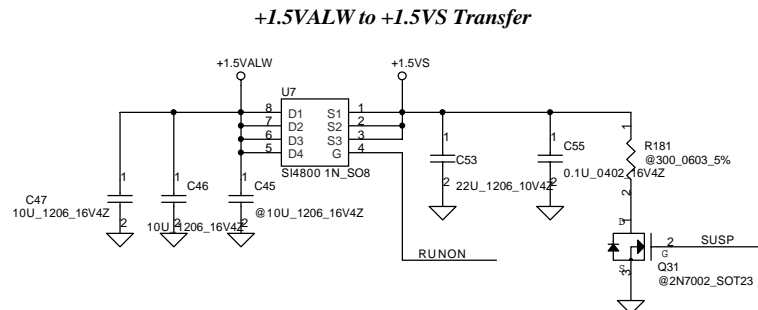
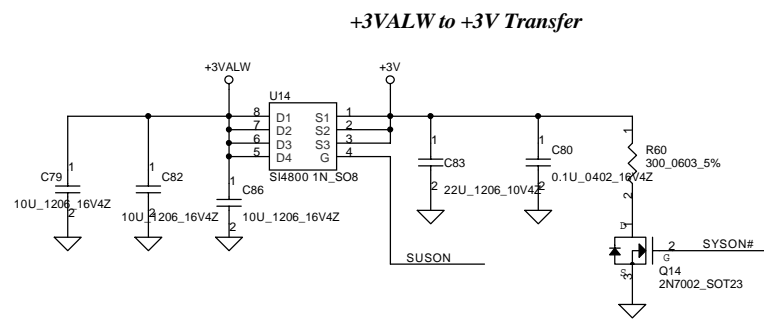
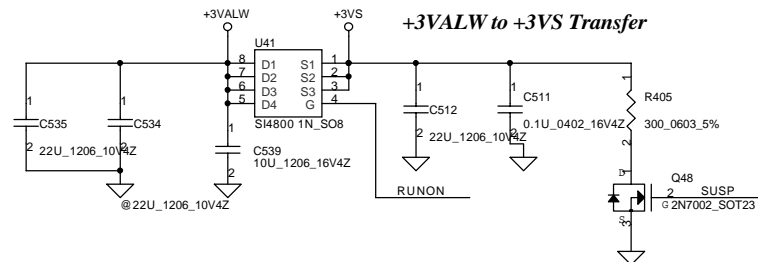
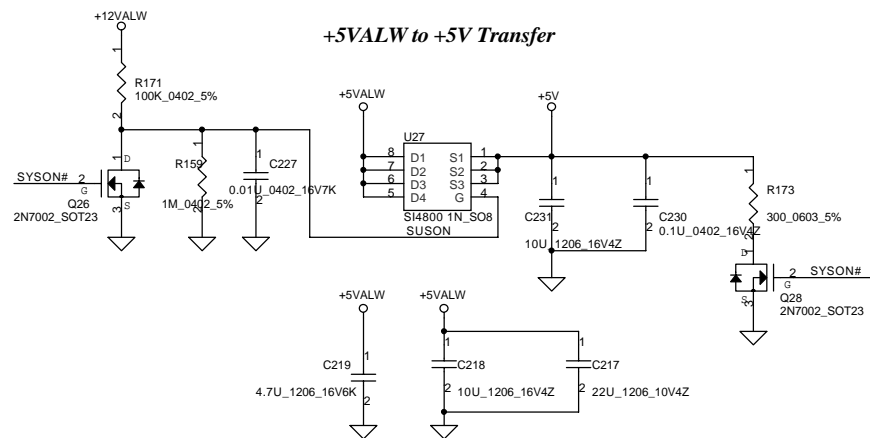


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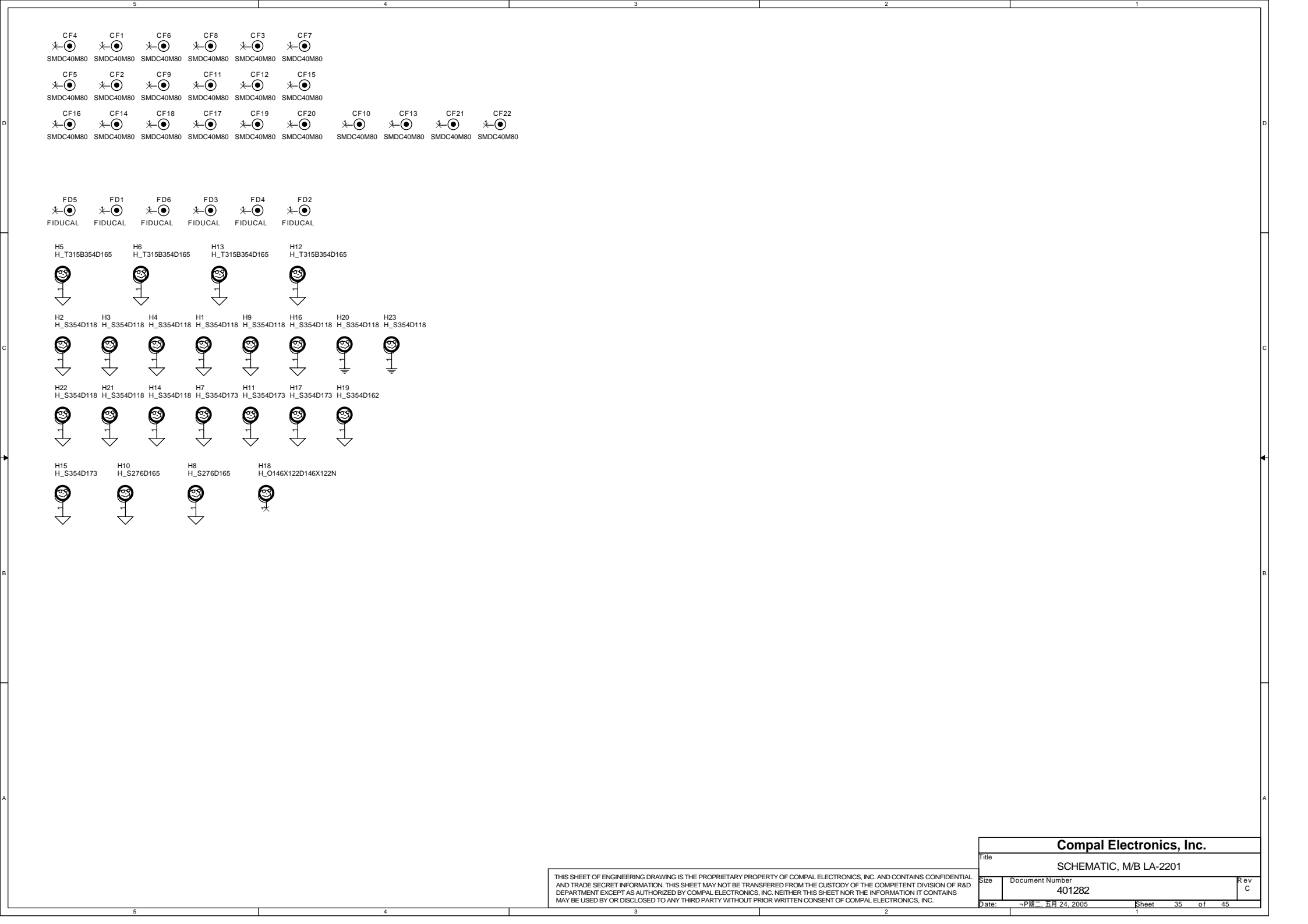
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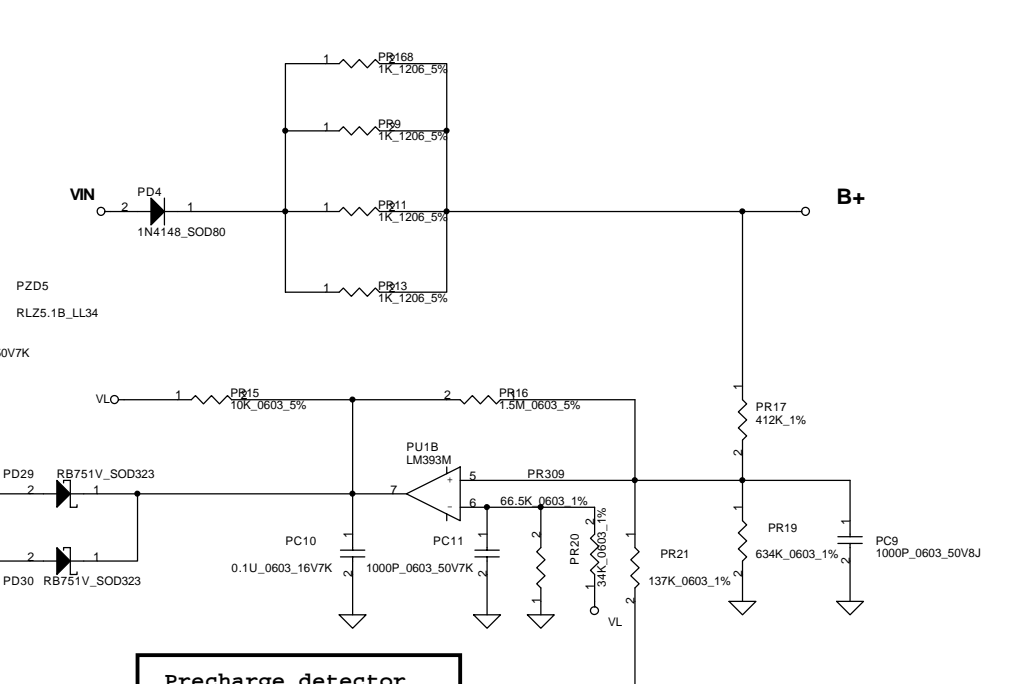
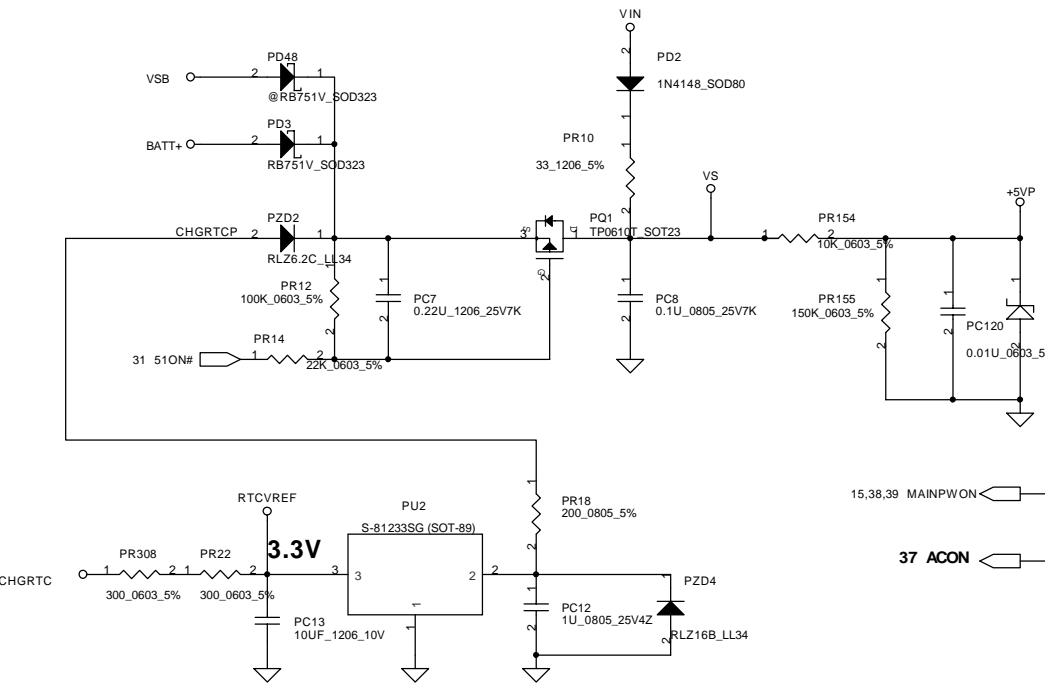
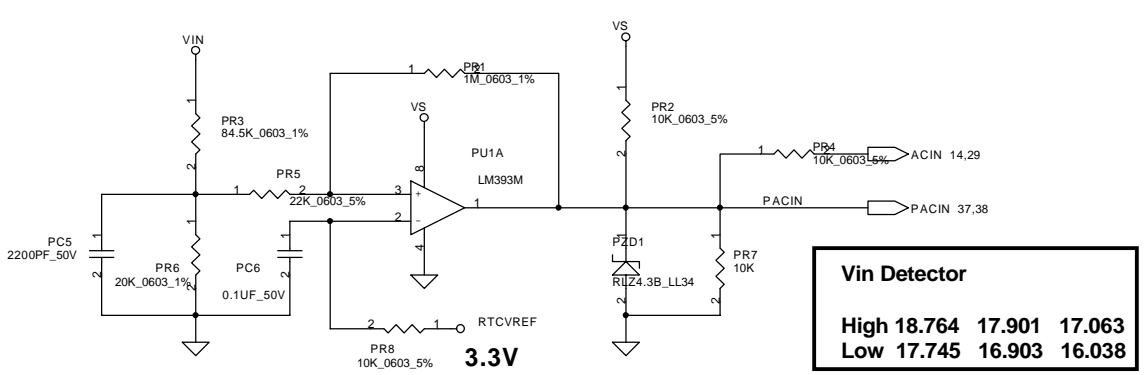
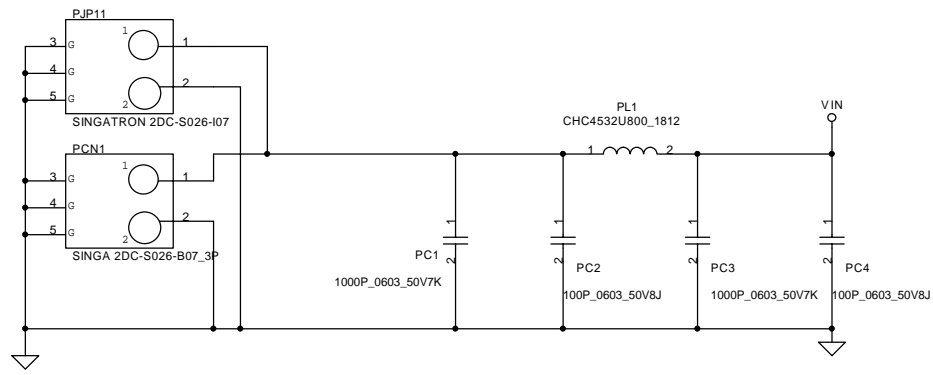
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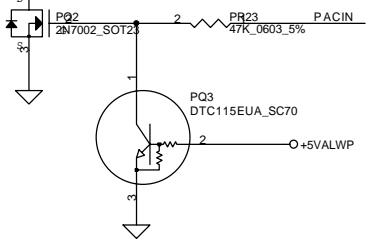
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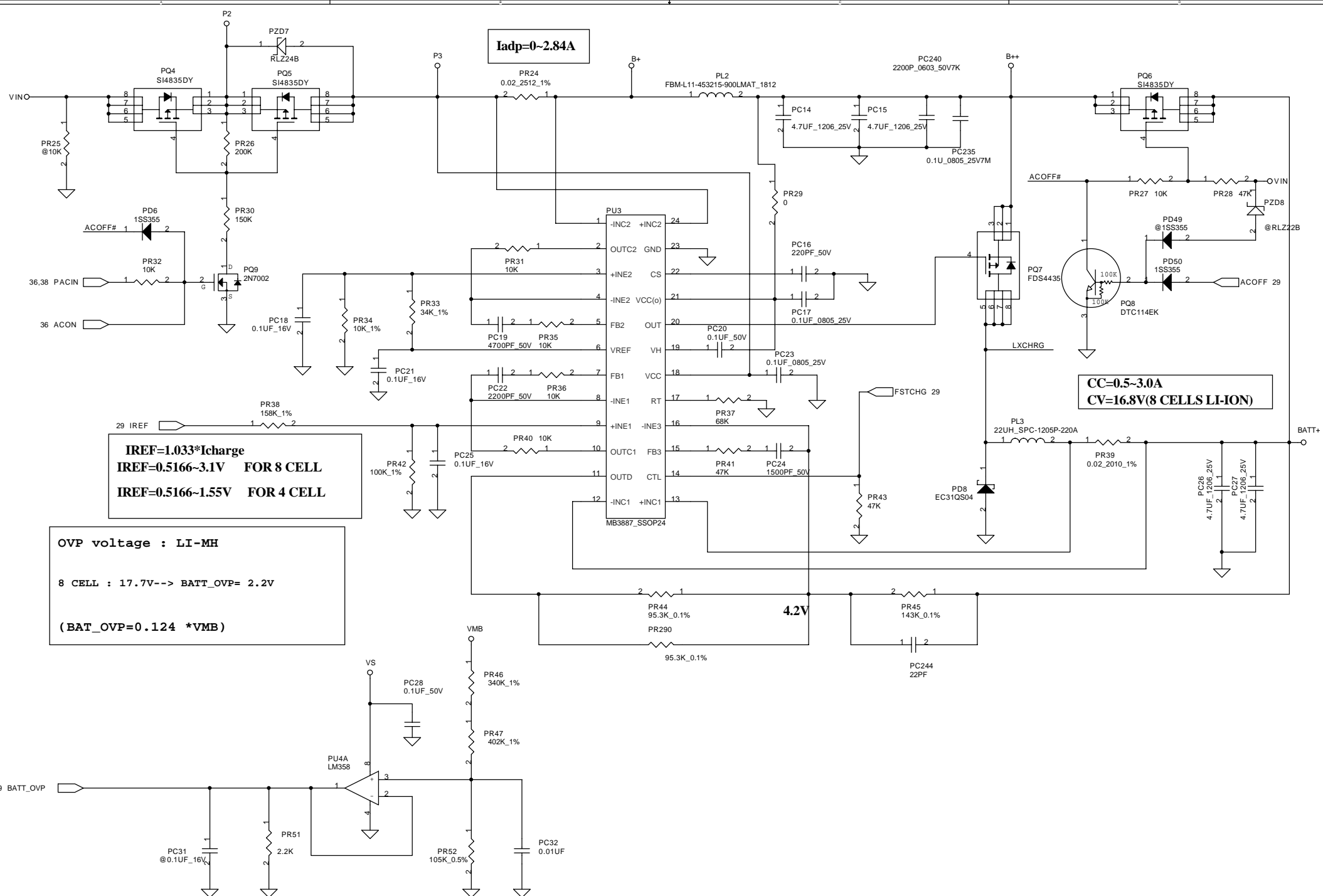




Precharge detector AC ADAPTOR		
16.69	16.05	15.42
15.6	15.02	14.35

Precharge detector AC ADAPTOR		
6.33	6.12	5.92
5.227	5.09	4.85

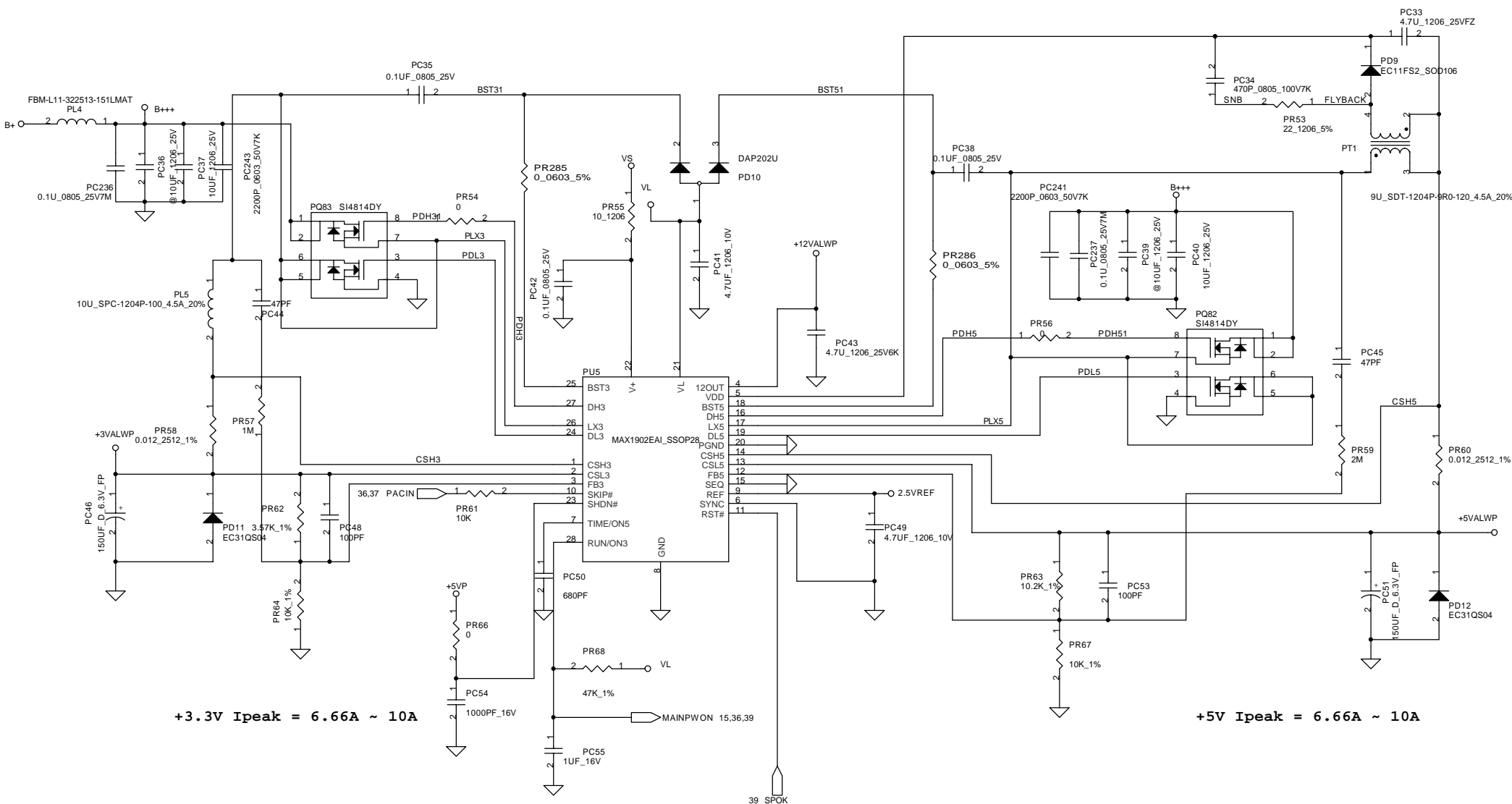




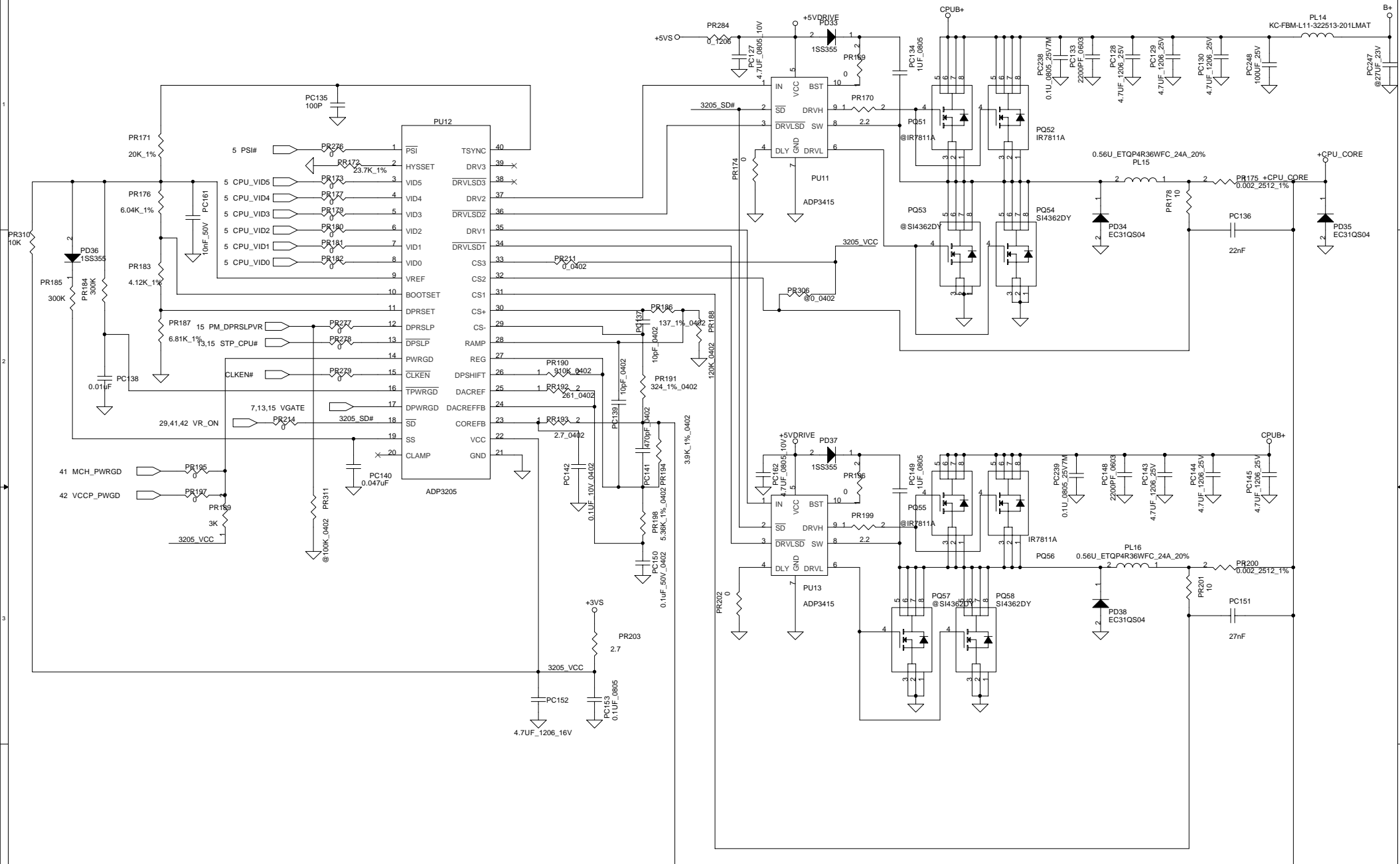
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CPU-CORE



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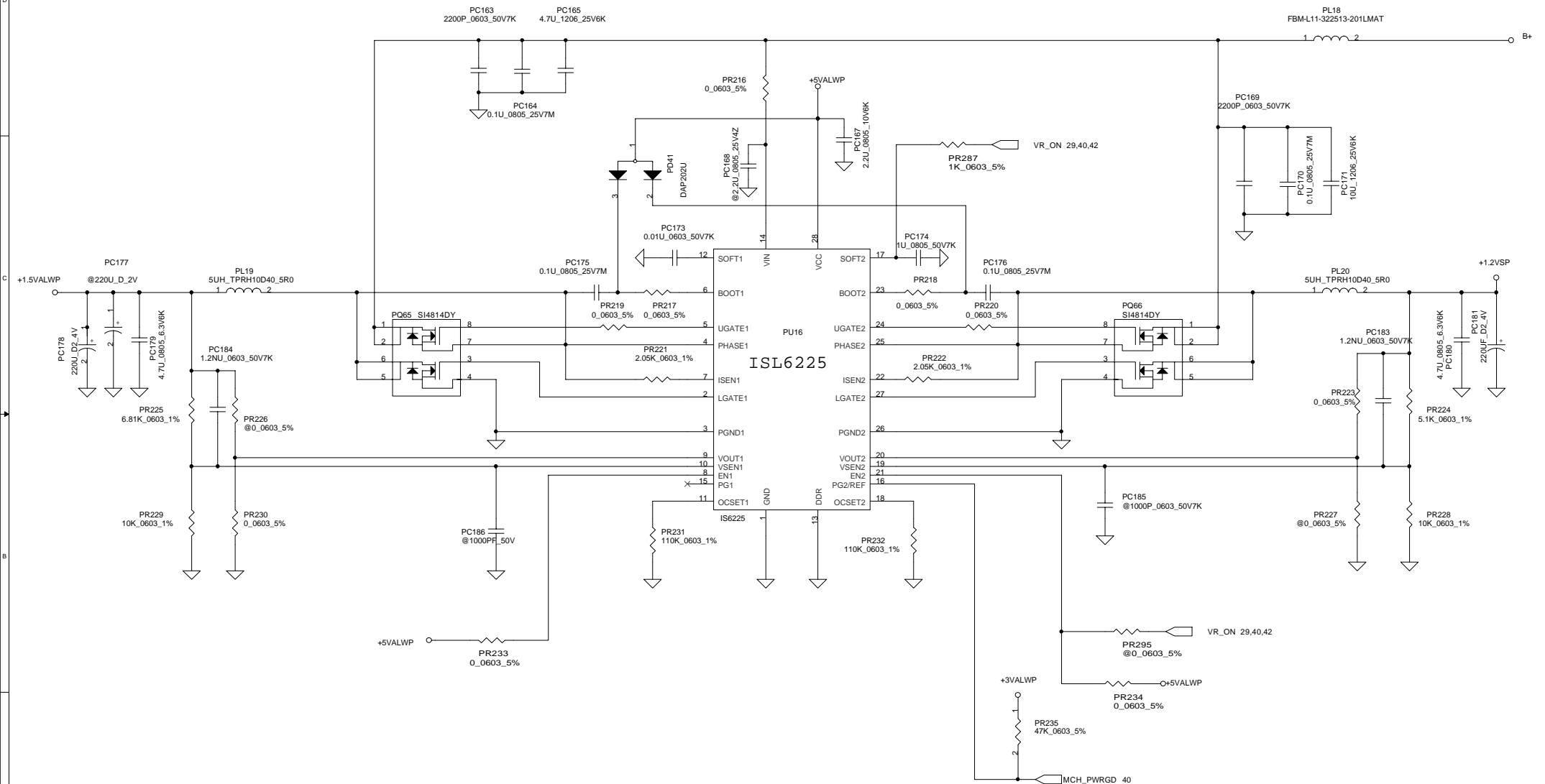
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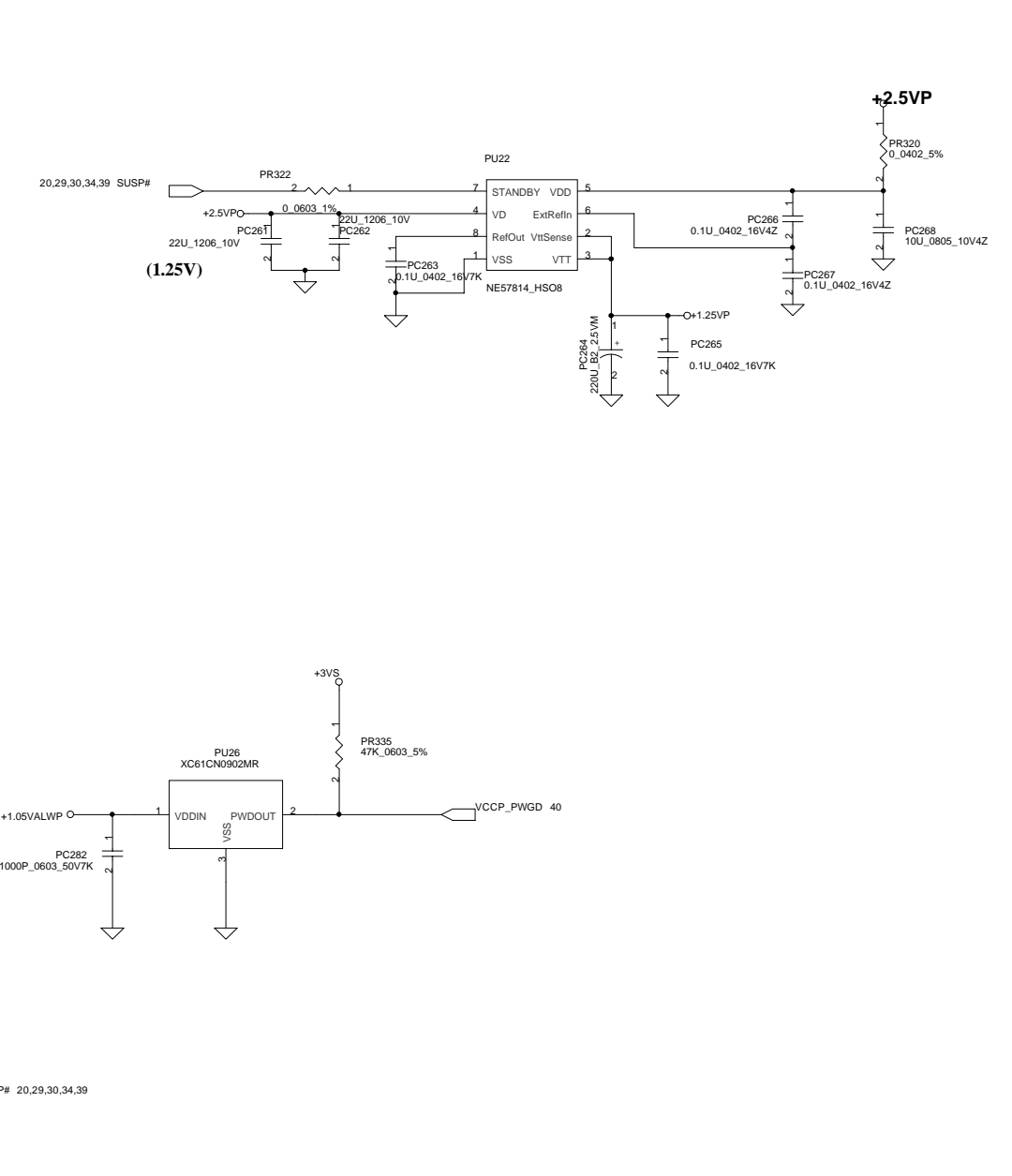
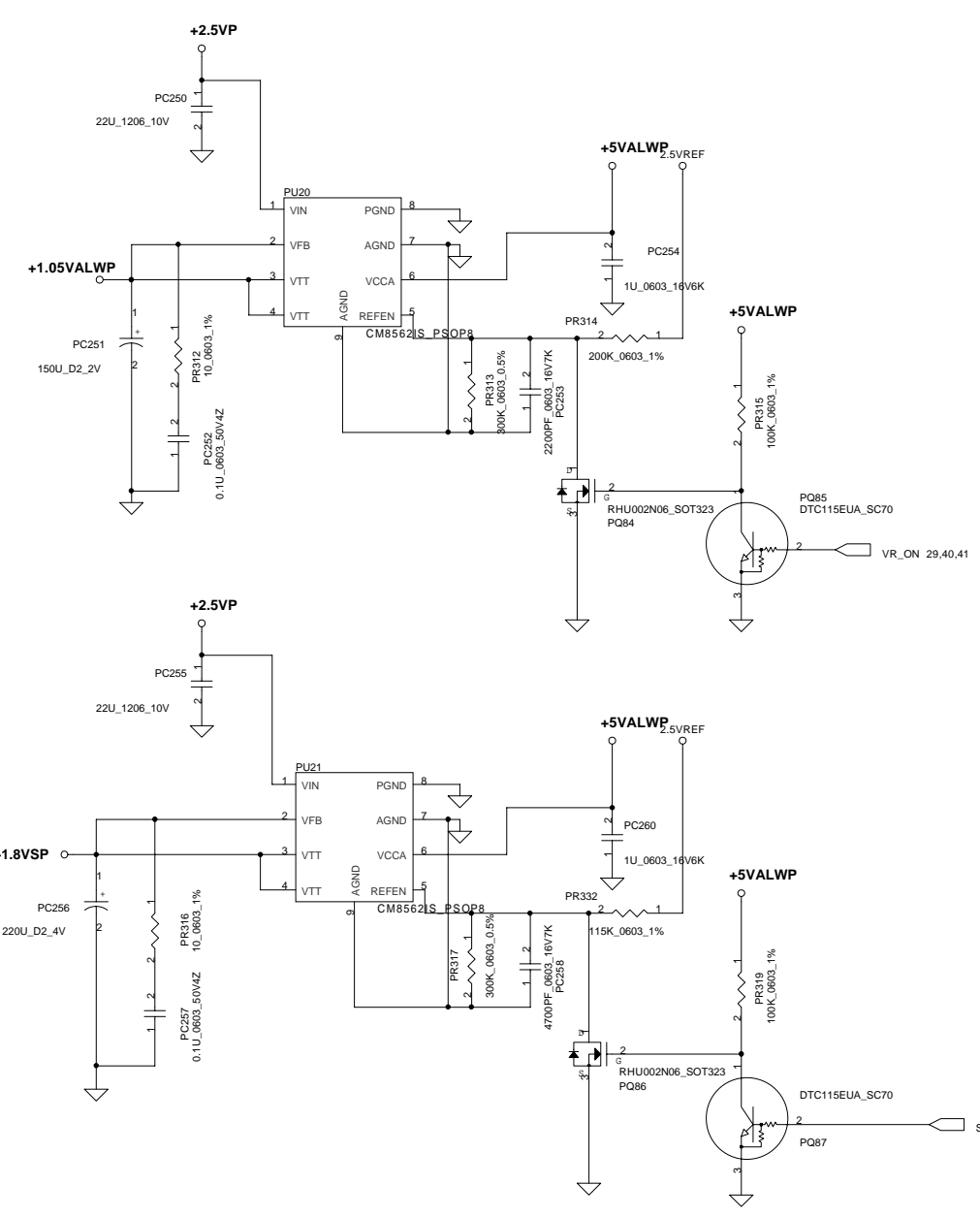


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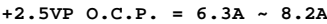
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Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		Set c4 mode controlled by bios based difference CPU		40	DELETE PR311:100K ; ADD PR277:0		DVT
2		Modify 1.05VP voltage level		42	1. change PR314 to 200k		DVT
3		modify 1.05VP,1.8VP soft start time		42	add PC253, PC258 to be 0.1U		DVT
4		add +SDREF signal circuit		43	add PR339:0; PQ89: 2N7002; PC283,PC284 :0.1U 16V;PR336,PR337:100K;PC285:10U 1206		PVT
5		Add one set power good:VCCP_PWGD		42,41	ADD LDO PU26 :XC61CN;PR335:47K;PC282:1000P 50V,PCHANGE R235 FROM 10K TO 47K		PVT
6		modify 1.05VP,1.8VP soft start time		42	CHANGE PC253 from 0.1u to 2200PF, PC258 from 0.1U to 4700PF		PVT
7		CHANGE PU5 from MAX1631 to MAX1902 (BECAUSE MAX1631 shortage)		38	CHANGE PT1 from 10u_1205P to 9u_sdt-1204p-9r0-120;delete PU19;CHANGE p15 FROM 10U_SPC-1205P-100 to 10u_1204p-100_4.5A;change PC39 from 180PF to 470PF;DELETE PZD6;change PU5 from max1631 to max1902		MP
8		FOR CL53A ; To change 1.2VSP to 1.35 VSP		37,41	CHANGE PR224 from 3.48K to 5.1K, delete PD49,DELETE PZD8		
9							

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Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	VER	Phase
1		reserve +SDREF signal circuit		8	reserve R477,R479		PVT
2		reserve +SDREF signal circuit		10	reserve R480,R481		PVT
3		EMI performance		8	change C420_net from MRCOMP to +2.5V		PVT
4		reserve syson,susp#,vr_on pull low resister		29	reserve R482,R483,R484		
5		cost down			change L18,L19,L14,L13,L12,L8,L9,L7 to 0 ohm del C534,C45		PVT
6		board version update		29	change R361 from 8.2k to 18k		PVT
7		for customer request			del TV_out , 1394 funtion		PVT
8		solove leakage			del D15		preMP
9		board version update		29	change R361 from 8.2k to 33k		preMP
10	USB port will be damaged by ESD, add ESD protect diode.	Per Lenovo request, add USB ESD protect diode	Rev3.0	26	Add D18, D32, D33. Change C239, C34, C22, C21, C24, C23 from 470P to 3.3P.		MP

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