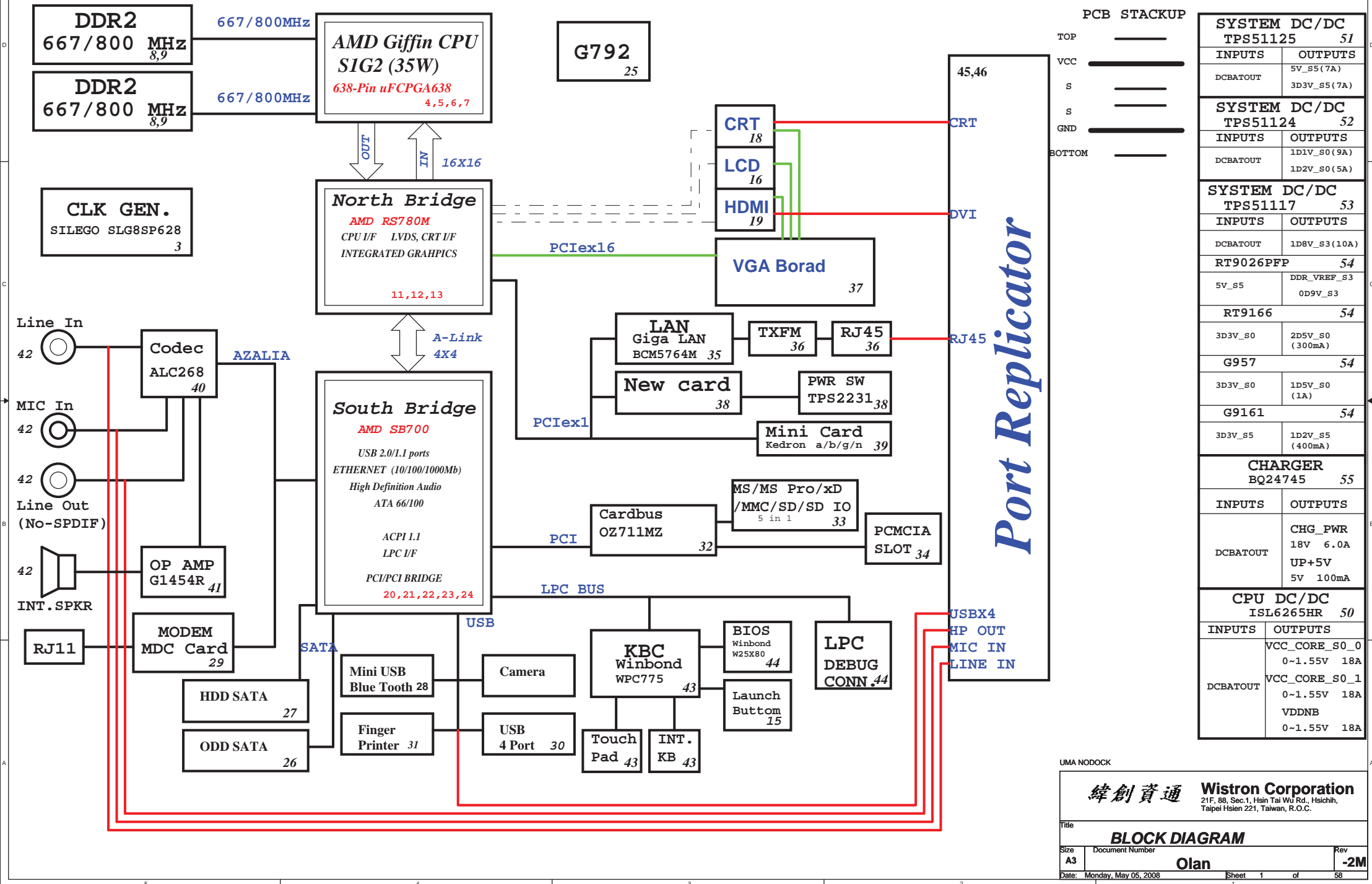
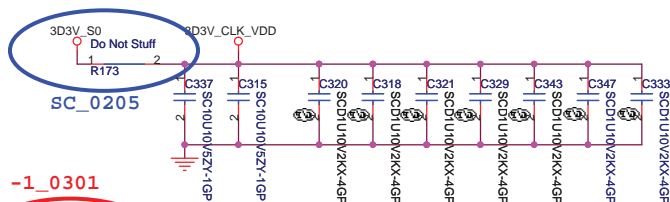


# Olan (TM15") Block Diagram

Project code: 91.4Z701.001  
PCB P/N : 48.4Z701.001  
REVISION : 07249-2M

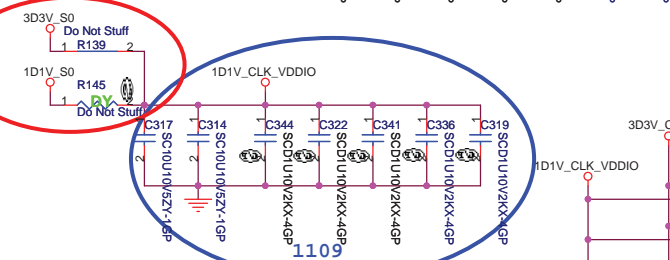






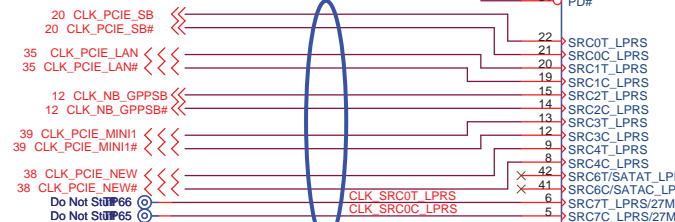
SC\_0205

-1\_0301



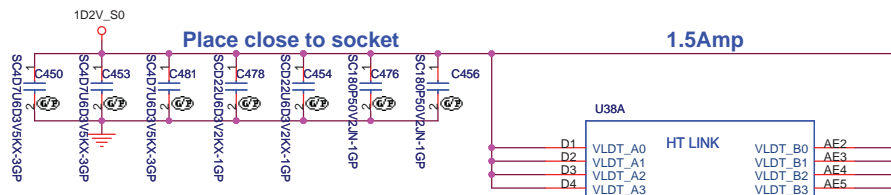
1109

SC\_0205



SC\_0205





State	Specification	Notes	ZM200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1500 MHz
S0.C0.P2	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1300 MHz
	TDP	3	TBD
S0.C0.P3	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
S0.C0.P4	VID_VDD Max	2	1.125 V
	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
S0.C0.P6	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
S0.C0.P7	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V

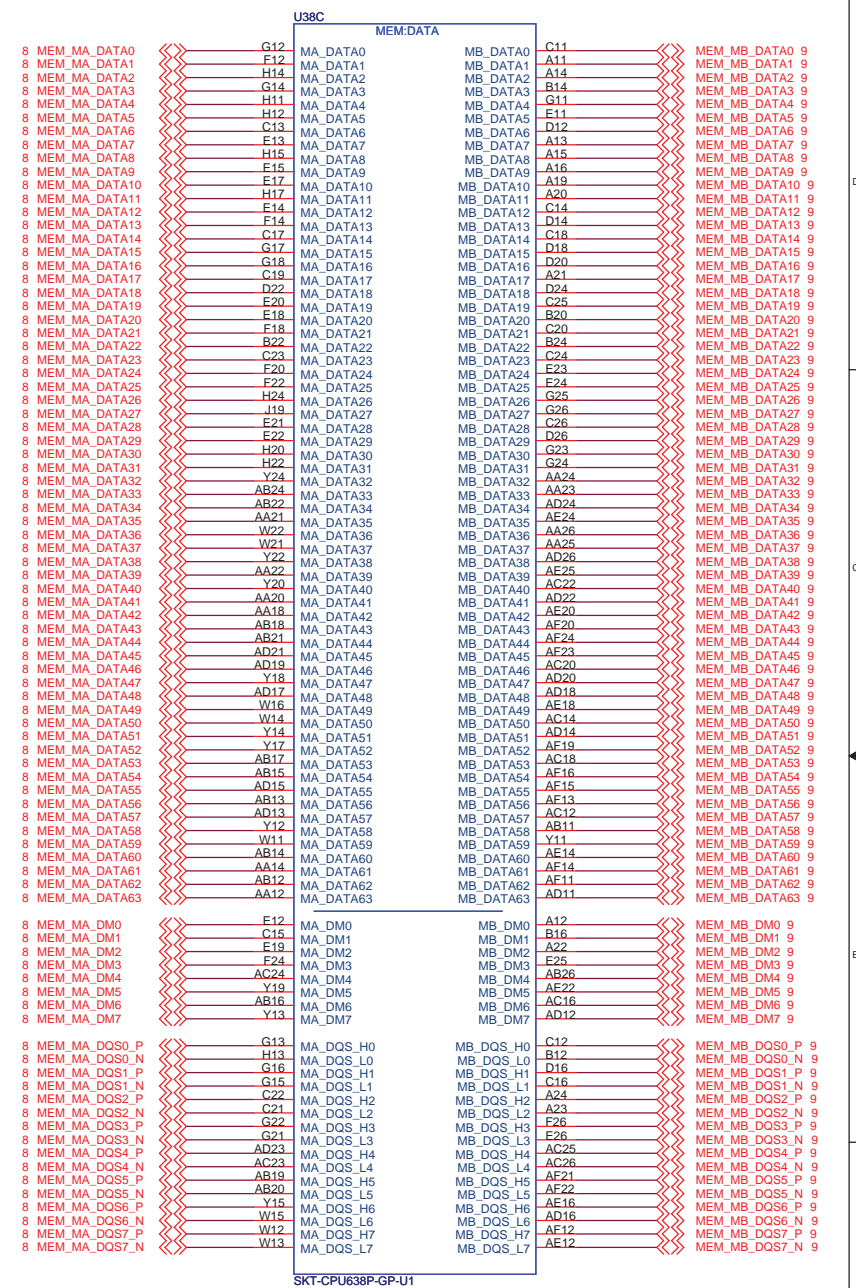
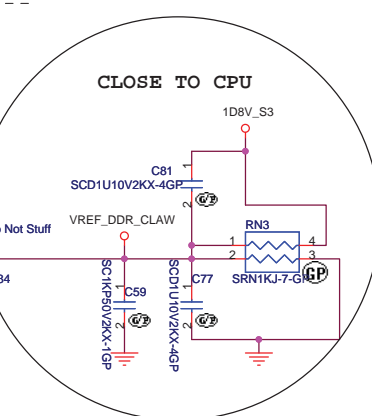
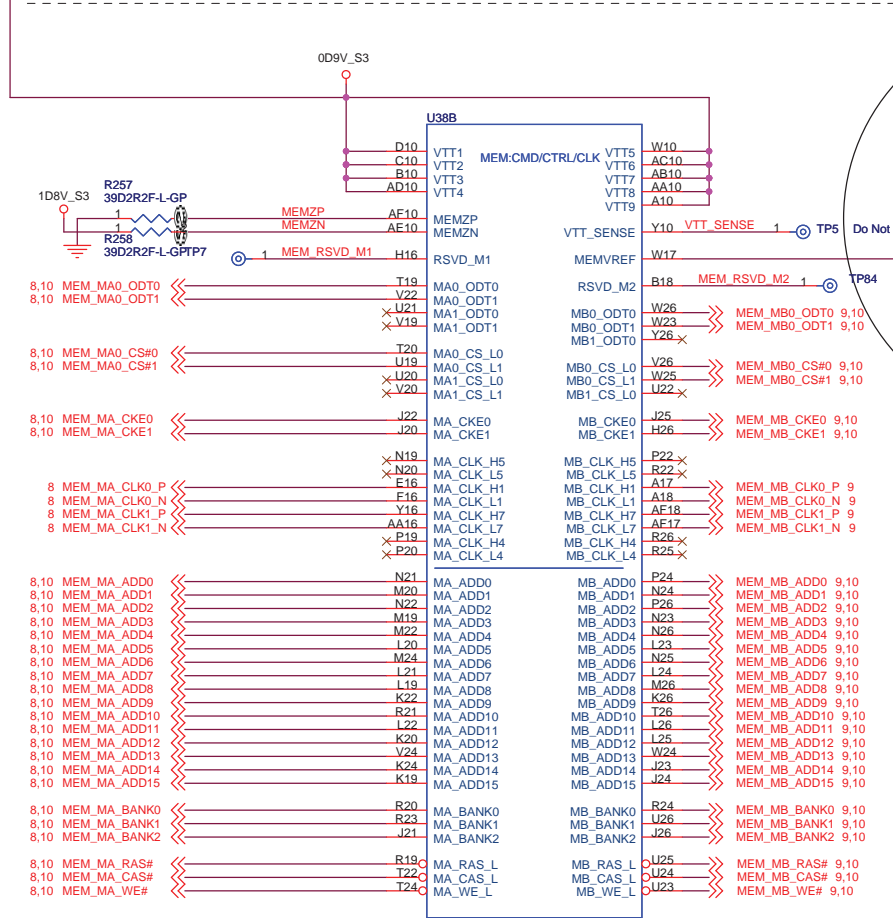
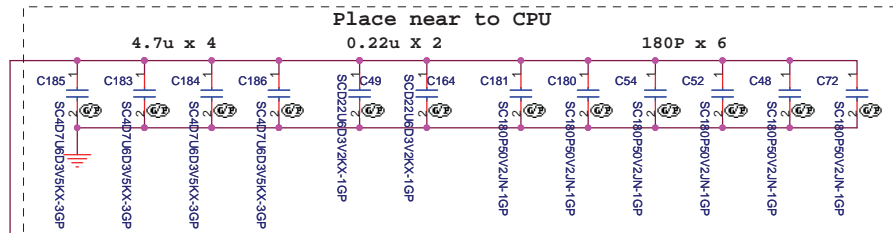
11 HT_NB_CPU_CAD_H0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	11 HT_CPU_NB_CAD_H0
11 HT_NB_CPU_CAD_L0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	11 HT_CPU_NB_CAD_L0
11 HT_NB_CPU_CAD_H1	E1	L0_CADIN_H1	L0_CADOUT_H1	AC2	11 HT_CPU_NB_CAD_H1
11 HT_NB_CPU_CAD_L1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	11 HT_CPU_NB_CAD_L1
11 HT_NB_CPU_CAD_H2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	11 HT_CPU_NB_CAD_H2
11 HT_NB_CPU_CAD_L2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	11 HT_CPU_NB_CAD_L2
11 HT_NB_CPU_CAD_H3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	11 HT_CPU_NB_CAD_H3
11 HT_NB_CPU_CAD_L3	H1	L0_CADIN_L3	L0_CADOUT_L3	AA3	11 HT_CPU_NB_CAD_L3
11 HT_NB_CPU_CAD_H4	J1	L0_CADIN_H4	L0_CADOUT_H4	W2	11 HT_CPU_NB_CAD_H4
11 HT_NB_CPU_CAD_L4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	11 HT_CPU_NB_CAD_L4
11 HT_NB_CPU_CAD_H5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	11 HT_CPU_NB_CAD_H5
11 HT_NB_CPU_CAD_L5	L2	L0_CADIN_L5	L0_CADOUT_L5	U1	11 HT_CPU_NB_CAD_L5
11 HT_NB_CPU_CAD_H6	L1	L0_CADIN_H6	L0_CADOUT_H6	U2	11 HT_CPU_NB_CAD_H6
11 HT_NB_CPU_CAD_L6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	11 HT_CPU_NB_CAD_L6
11 HT_NB_CPU_CAD_H7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	11 HT_CPU_NB_CAD_H7
11 HT_NB_CPU_CAD_L7	N2	L0_CADIN_L7	L0_CADOUT_L7	R1	11 HT_CPU_NB_CAD_L7
11 HT_NB_CPU_CAD_H8	E5	L0_CADIN_H8	L0_CADOUT_H8	AD4	11 HT_CPU_NB_CAD_H8
11 HT_NB_CPU_CAD_L8	F5	L0_CADIN_L8	L0_CADOUT_L8	AD3	11 HT_CPU_NB_CAD_L8
11 HT_NB_CPU_CAD_H9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	11 HT_CPU_NB_CAD_H9
11 HT_NB_CPU_CAD_L9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	11 HT_CPU_NB_CAD_L9
11 HT_NB_CPU_CAD_H10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	11 HT_CPU_NB_CAD_H10
11 HT_NB_CPU_CAD_L10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	11 HT_CPU_NB_CAD_L10
11 HT_NB_CPU_CAD_H11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	11 HT_CPU_NB_CAD_H11
11 HT_NB_CPU_CAD_L11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	11 HT_CPU_NB_CAD_L11
11 HT_NB_CPU_CAD_H12	K3	L0_CADIN_H12	L0_CADOUT_H12	V5	11 HT_CPU_NB_CAD_H12
11 HT_NB_CPU_CAD_L12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	11 HT_CPU_NB_CAD_L12
11 HT_NB_CPU_CAD_H13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	11 HT_CPU_NB_CAD_H13
11 HT_NB_CPU_CAD_L13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	11 HT_CPU_NB_CAD_L13
11 HT_NB_CPU_CAD_H14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	11 HT_CPU_NB_CAD_H14
11 HT_NB_CPU_CAD_L14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	11 HT_CPU_NB_CAD_L14
11 HT_NB_CPU_CAD_H15	N5	L0_CADIN_H15	L0_CADOUT_H15	T4	11 HT_CPU_NB_CAD_H15
11 HT_NB_CPU_CAD_L15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	11 HT_CPU_NB_CAD_L15
11 HT_NB_CPU_CLK_H0	J3	L0_CLKIN_H0	L0_CLKOUT_H0	Y1	11 HT_CPU_NB_CLK_H0
11 HT_NB_CPU_CLK_L0	J2	L0_CLKIN_L0	L0_CLKOUT_L0	W1	11 HT_CPU_NB_CLK_L0
11 HT_NB_CPU_CLK_H1	J5	L0_CLKIN_H1	L0_CLKOUT_H1	Y4	11 HT_CPU_NB_CLK_H1
11 HT_NB_CPU_CLK_L1	K5	L0_CLKIN_L1	L0_CLKOUT_L1	Y3	11 HT_CPU_NB_CLK_L1
11 HT_NB_CPU_CTL_H0	N1	L0_CTLIN_H0	L0_CTLOUT_H0	R2	11 HT_CPU_NB_CTL_H0
11 HT_NB_CPU_CTL_L0	P1	L0_CTLIN_L0	L0_CTLOUT_L0	R3	11 HT_CPU_NB_CTL_L0
11 HT_NB_CPU_CTL_H1	P3	L0_CTLIN_H1	L0_CTLOUT_H1	T5	11 HT_CPU_NB_CTL_H1
11 HT_NB_CPU_CTL_L1	P4	L0_CTLIN_L1	L0_CTLOUT_L1	R5	11 HT_CPU_NB_CTL_L1

SKT-CPU638P-GP-U1  
62.10055.111  
ZND = 62.10040.471  
SKT-BGA638H176

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Taipei Hsien 221, Taiwan, R.O.C.

Title			CPU_HT_LINK I/F (1/4)	
Size	Document Number	Olan		Rev
A3				-1
Date:	Friday, April 18, 2008	Sheet	4	of 58



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Taipei Hsien 221, Taiwan, R.O.C.

Title
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**CPU\_DDR\_(2/4)**

Size

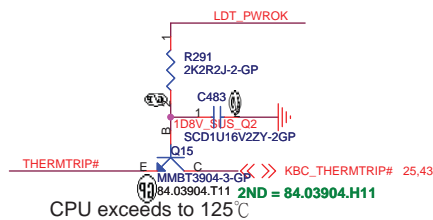
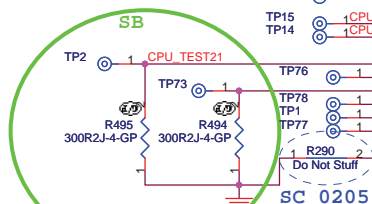
Document Number	
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## Olar

Date \_\_\_\_\_

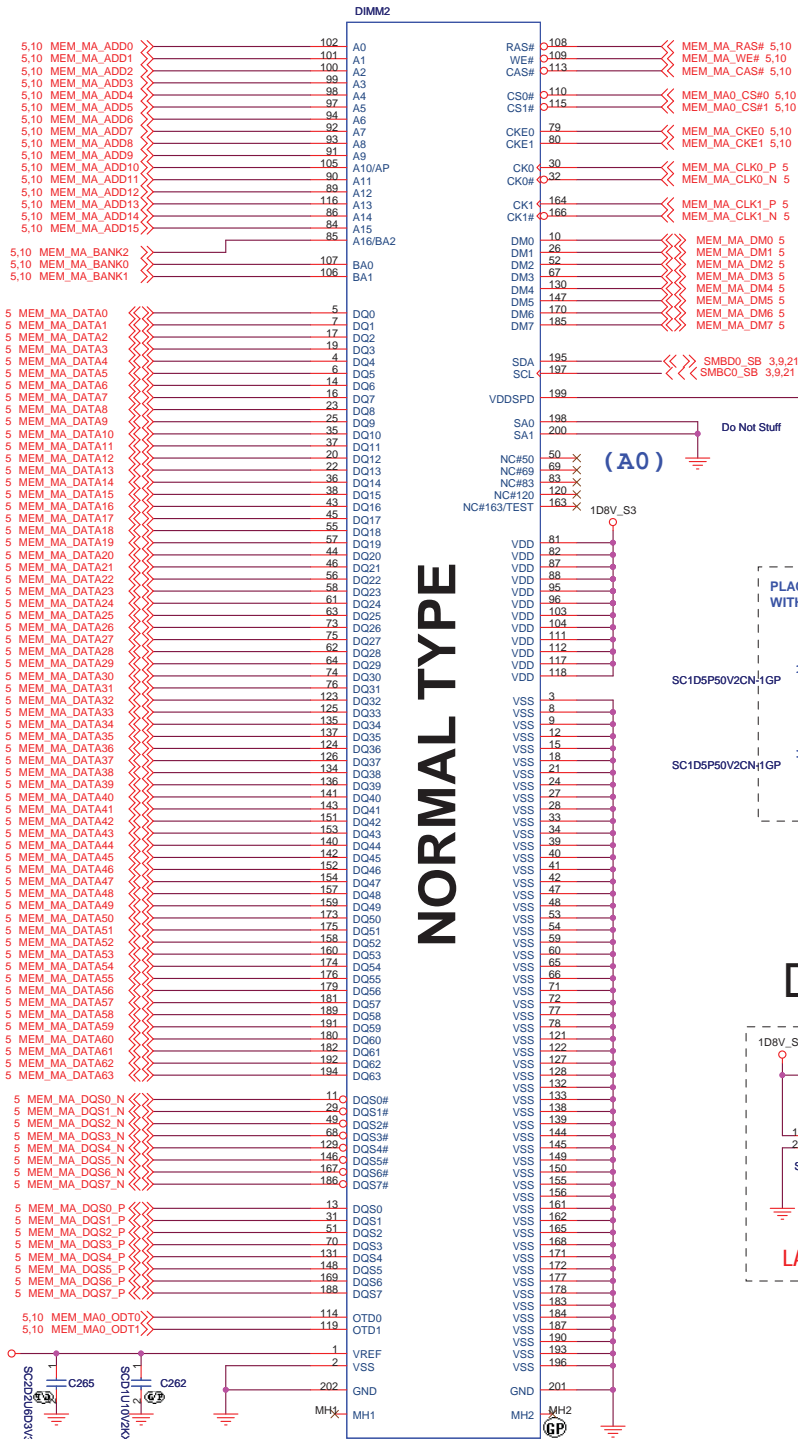
Friday, April 18, 2008

Sheet 5 of 58

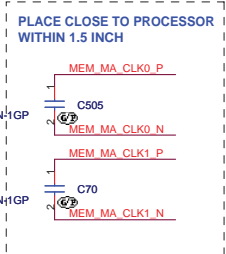
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Title			
<b>CPU_Control&amp;Debug_(3/4)</b>			
Size	Document Number	Rev	
<b>A3</b>	<b>Olan</b>	<b>-2M</b>	
Date:	Monday, May 05, 2008	Sheet 6 of	58

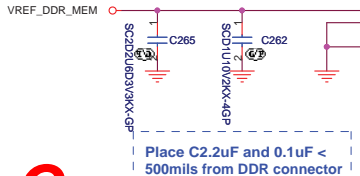
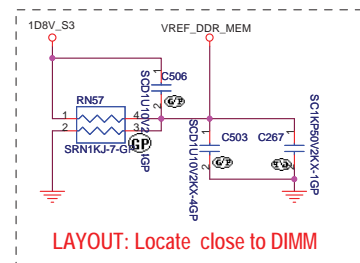




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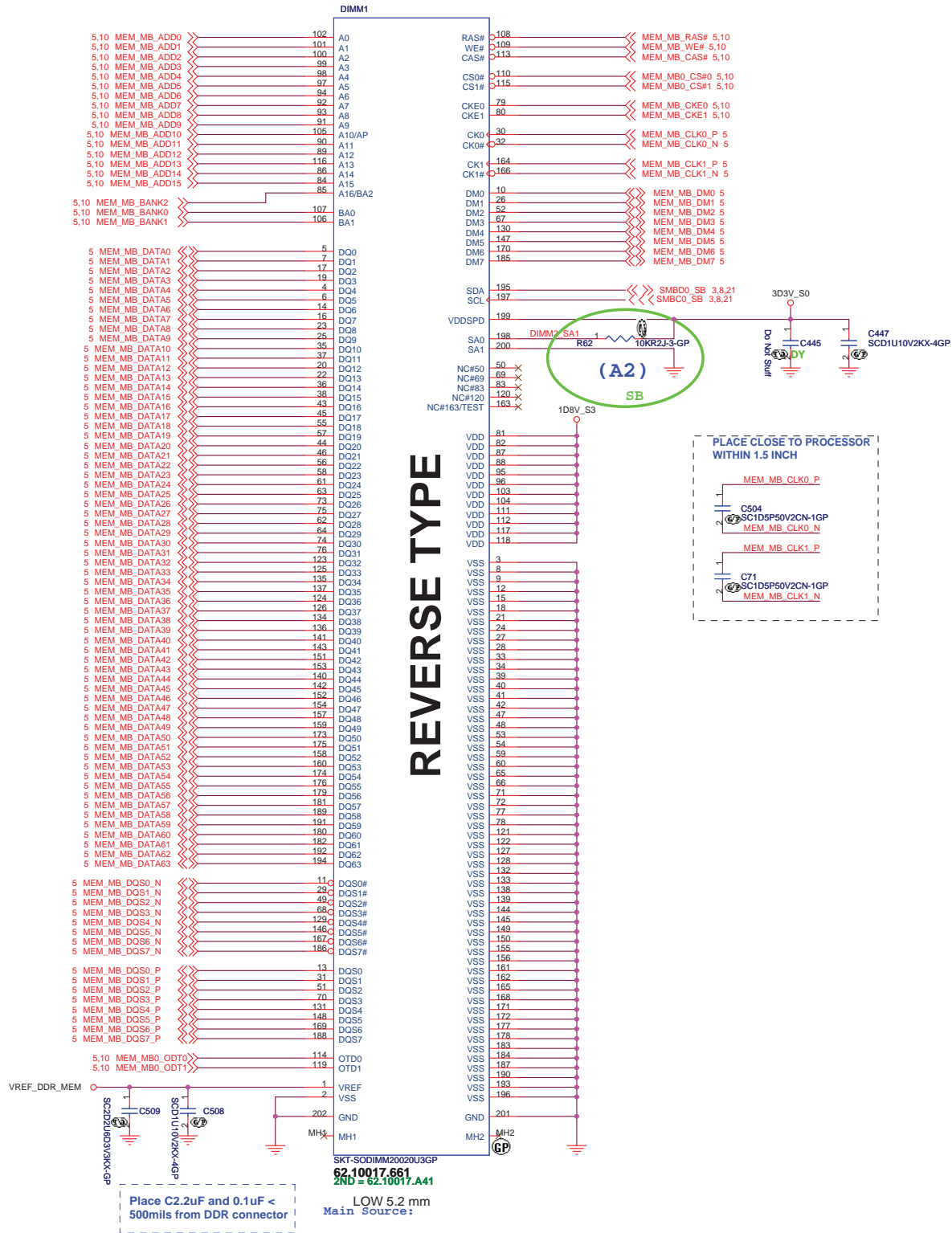


### DDR\_VREF



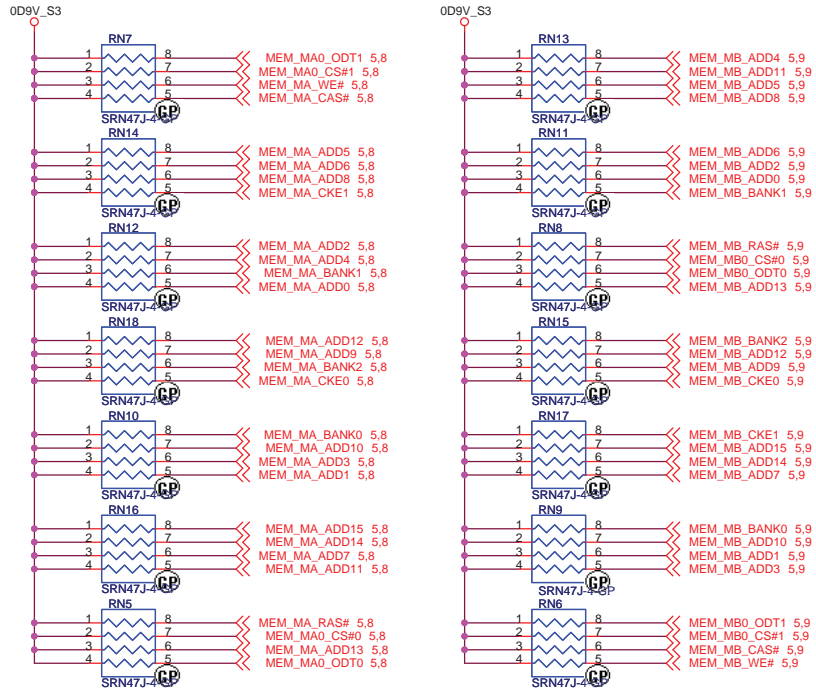
DDR2-200P-22-GP-U2  
62.10017.A61  
2ND = 62.10017.A51  
HI 9.2mm

Main Source:

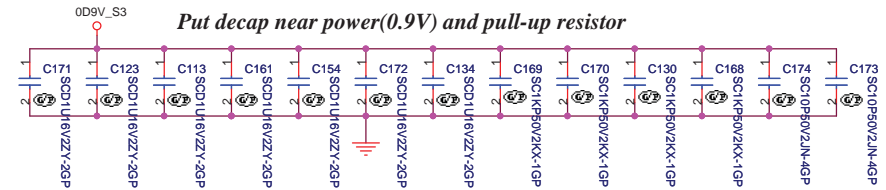


## PARALLEL TERMINATION

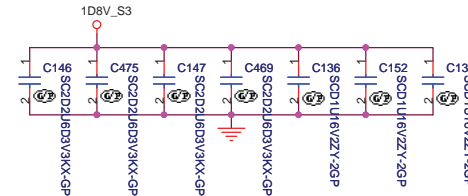
Put decap near power(0.9V) and pull-up resistor



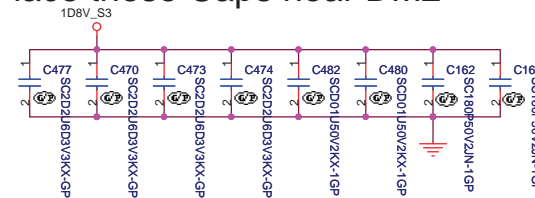
## Decoupling Capacitor



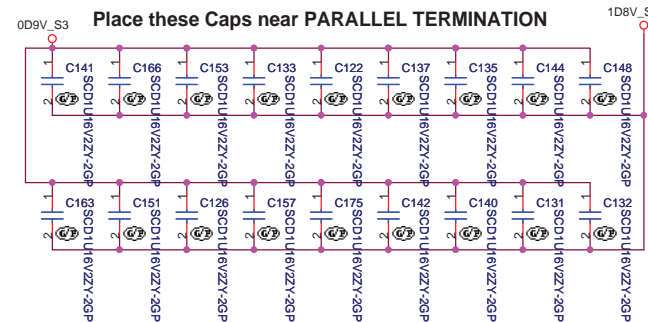
## Place these Caps near DM1



## Place these Caps near DM2



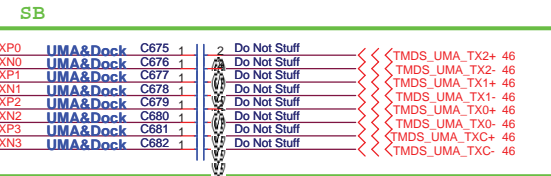
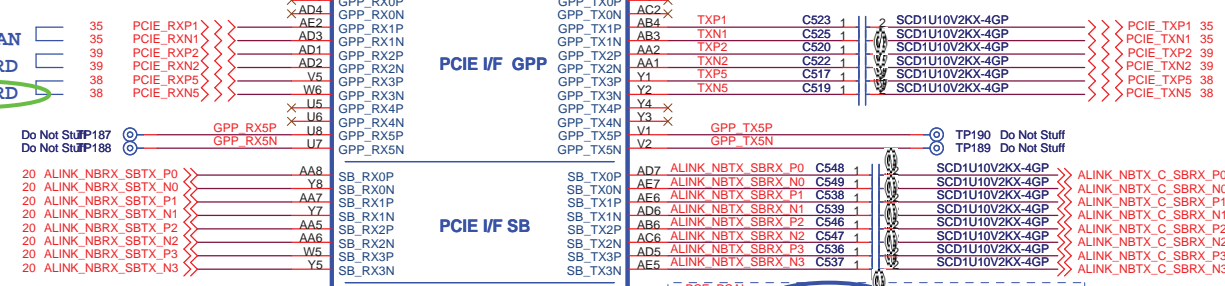
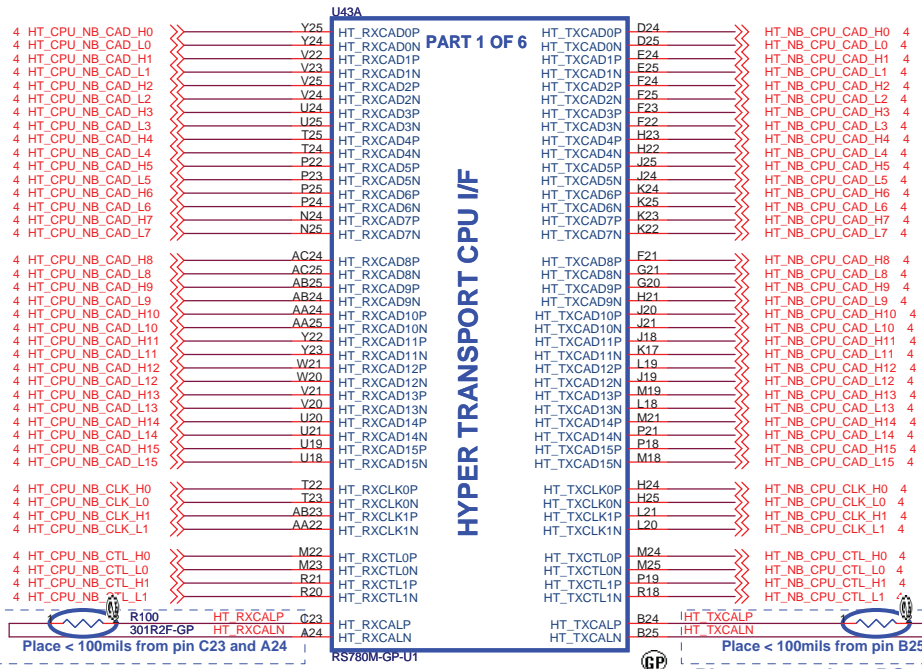
## Place these Caps near PARALLEL TERMINATION



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Taipei Hsien 221, Taiwan, R.O.C.

Title		
<b>DDR DAMPING &amp; TERMINATION</b>		
Size	Document Number	Rev
A3	Olan	-1
Date:	Friday, April 18, 2008	Sheet 10 of 58



RS780M Display Port Support(muxed on GFX)

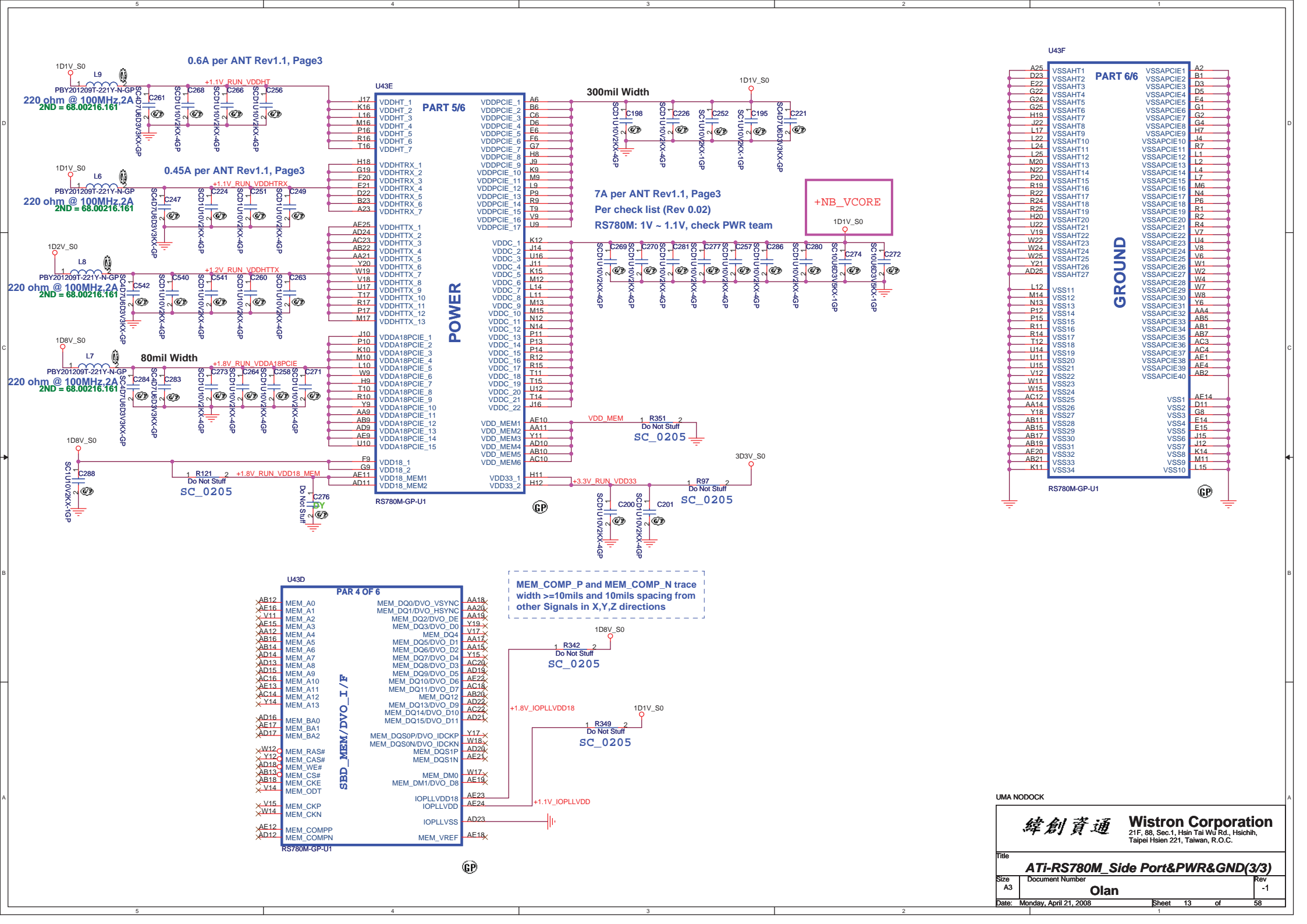
DP0	GFX_TX0, TX1, TX2, TX3, AUX0, HPD0
DP1	GFX_TX4, TX5, TX6, TX7, AUX1, HPD1

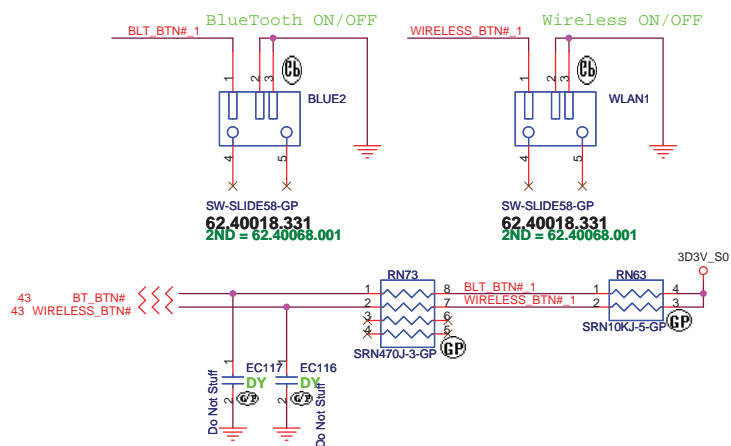
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title <b>ATI-RS780M_HT LINK&amp;PCIE(1/3)</b>		
Size A3	Document Number <b>Olan</b>	Rev -1
Date: Monday, April 21, 2008		Sheet 11 of 58





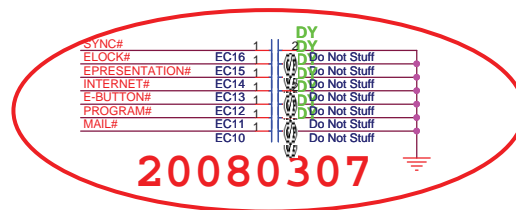
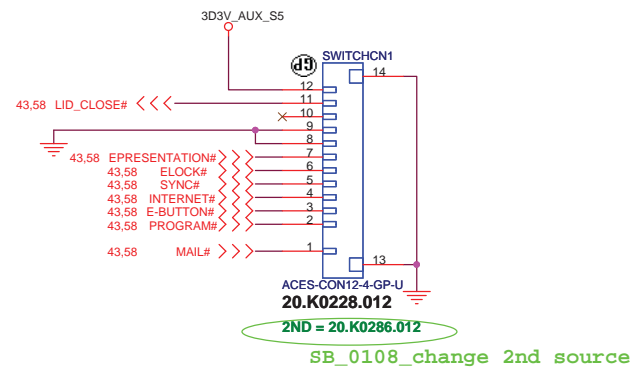
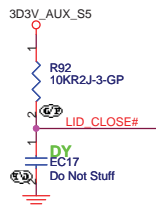
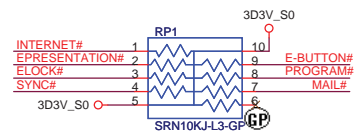


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Title		<b>SWITCH</b>	
Size	Document Number	Rev	
A3	Olan	-1	
Date:	Friday, April 18, 2008	Sheet	14 of 58

# LAUNCH

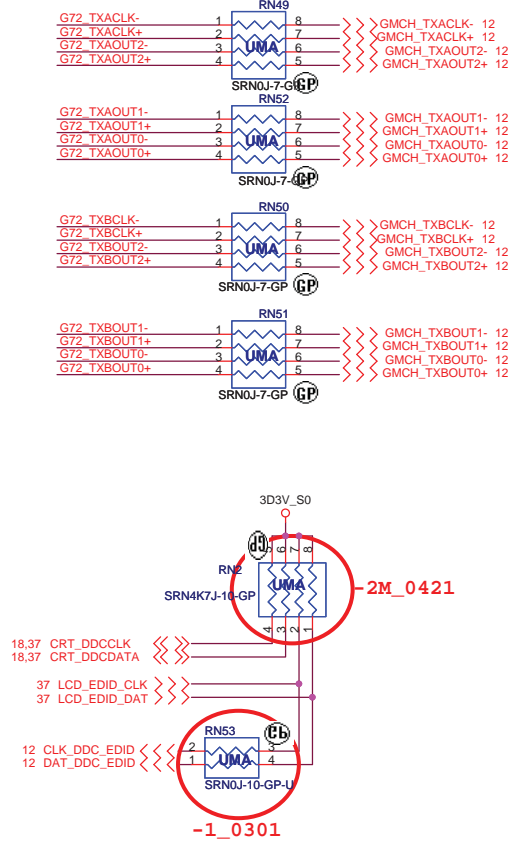


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**緯創資通** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

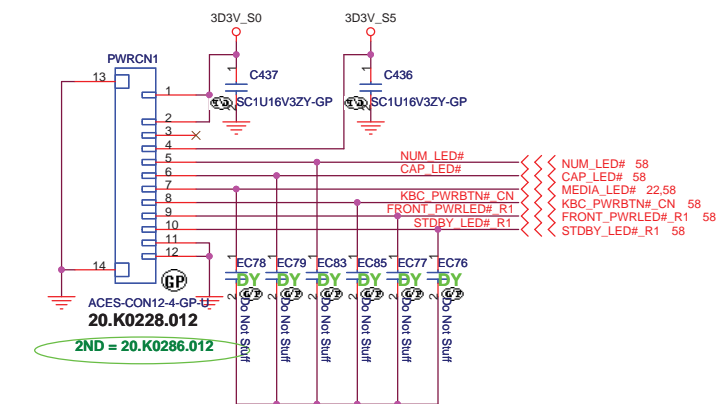
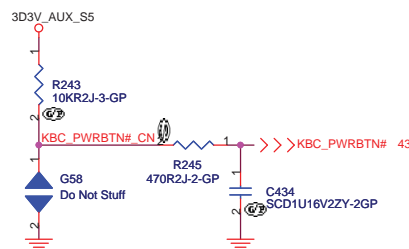
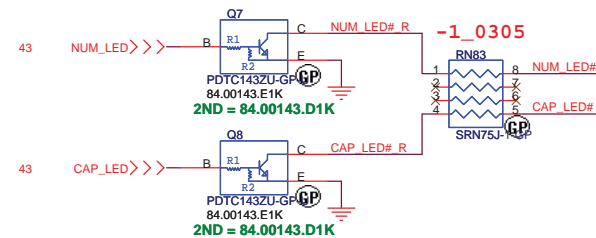
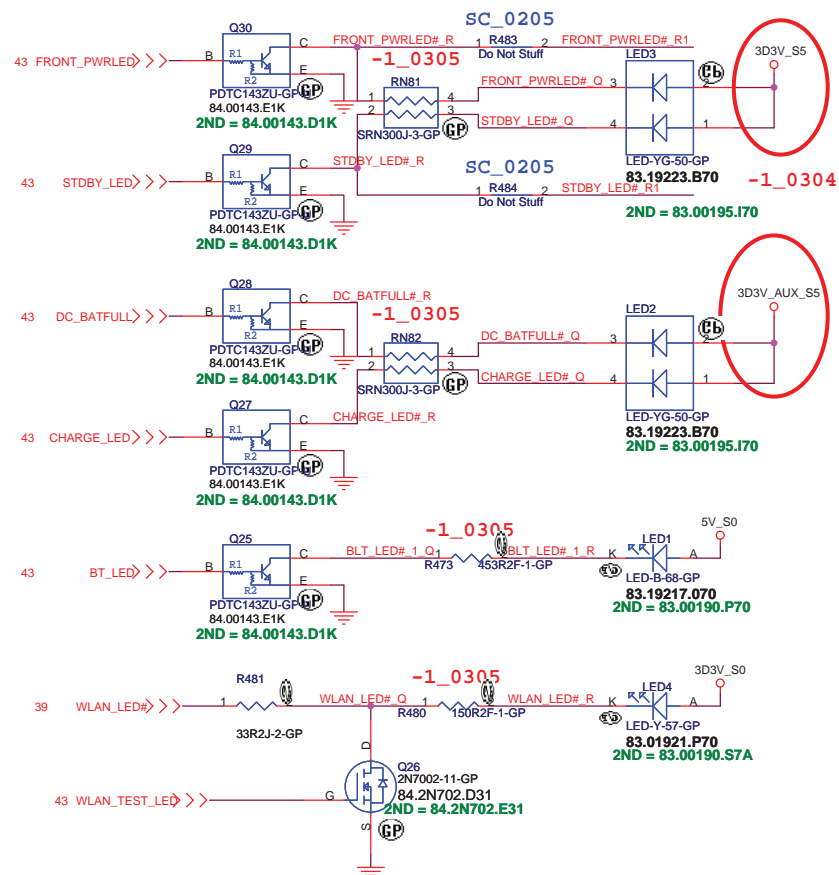
Title				
LAUNCH				
Size	Document Number			Rev
A3	Olan			-1
Date:	Friday, April 18, 2008		Sheet 15 of	58

**WWW.AliSaler.Com**

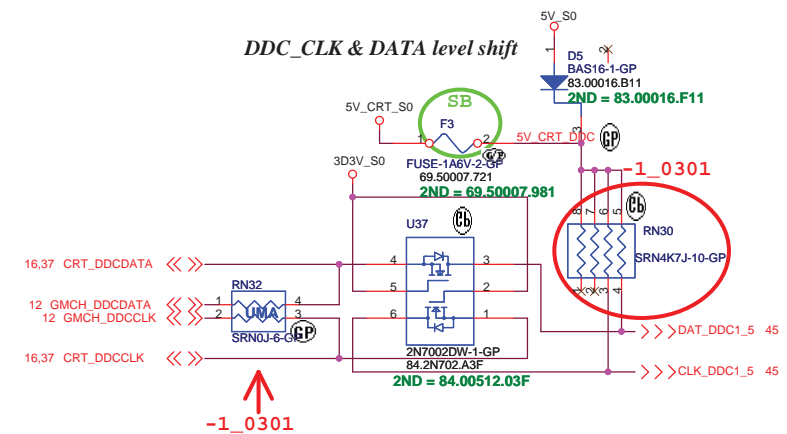
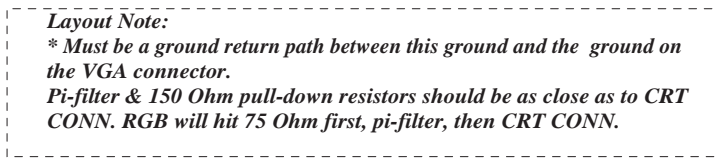


Title			
<b>LCD CONN</b>			
Size	Document Number		Rev
<b>A3</b>	<b>Olan</b>		<b>-2M</b>
Date:	Monday, May 05, 2008	Sheet	16 of 58

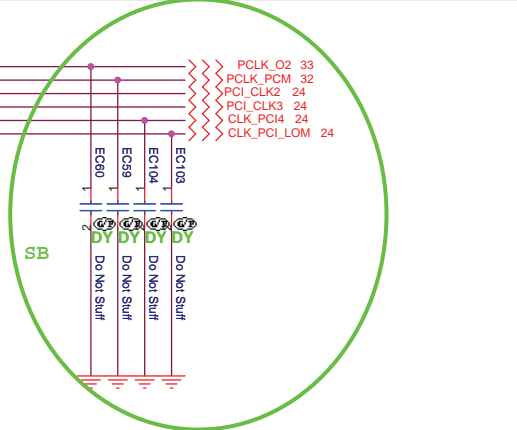
## LED

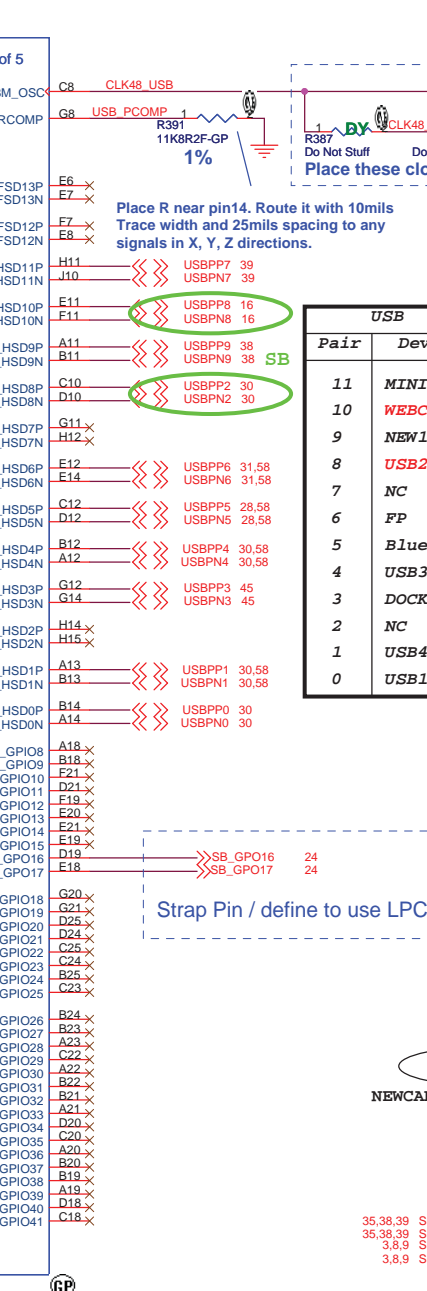
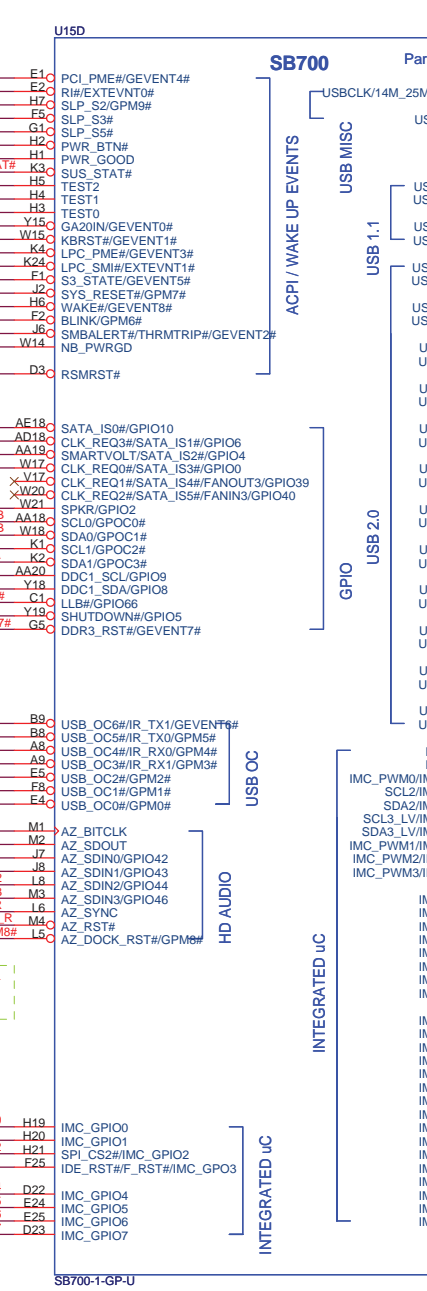
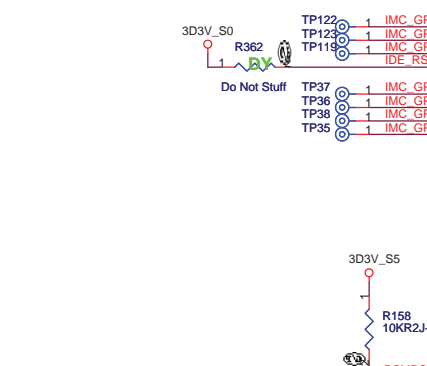
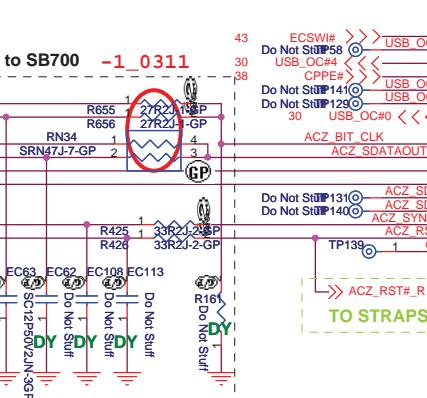
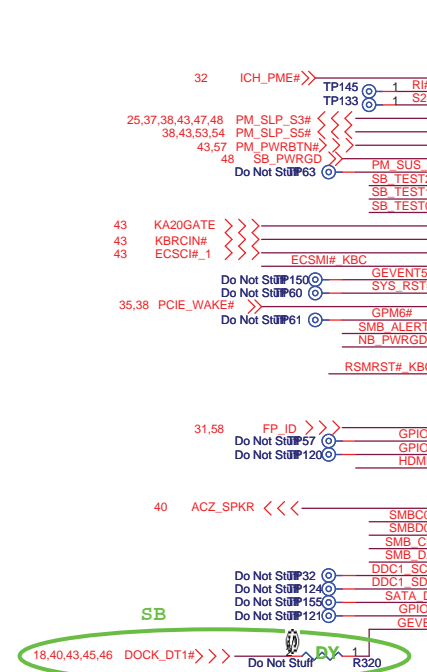
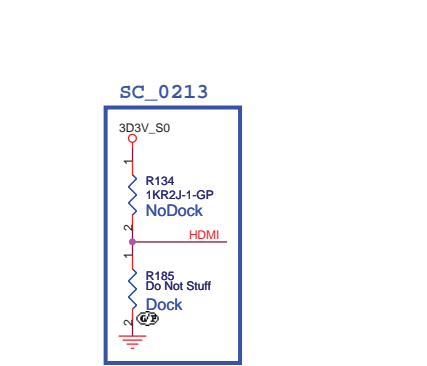
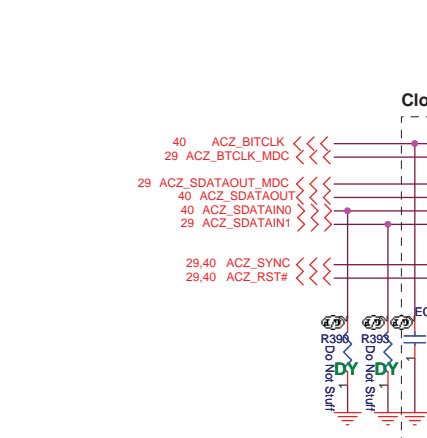
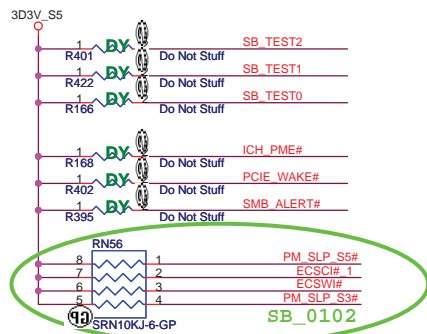


SB\_0108\_change 2nd source

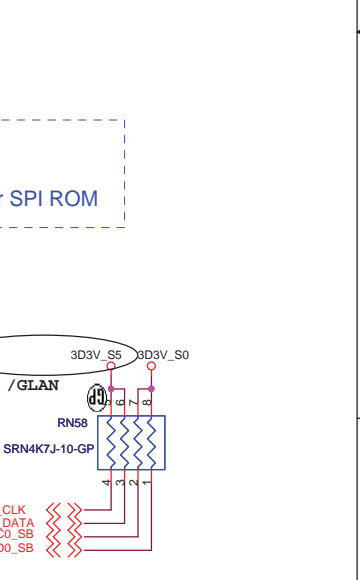
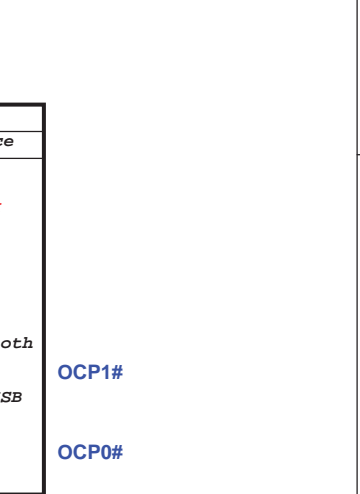
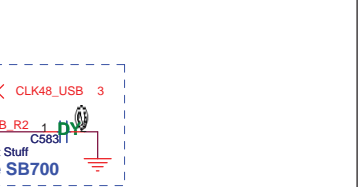
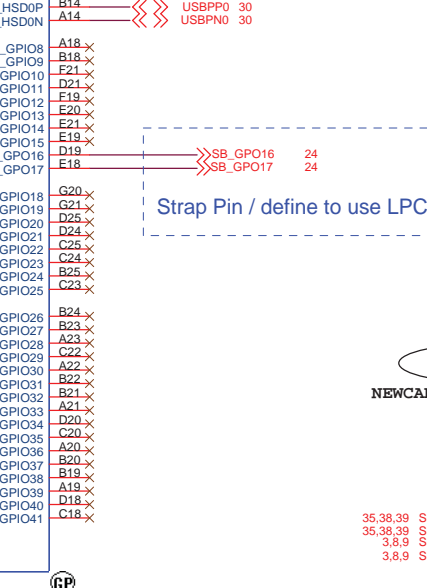








USB	
Pair	Device
11	MINIC1
10	WEBCAM
9	NEW1
8	USB2
7	NC
6	FP
5	Bluetooth
4	USB3
3	DOCK USB
2	NC
1	USB4
0	USB1

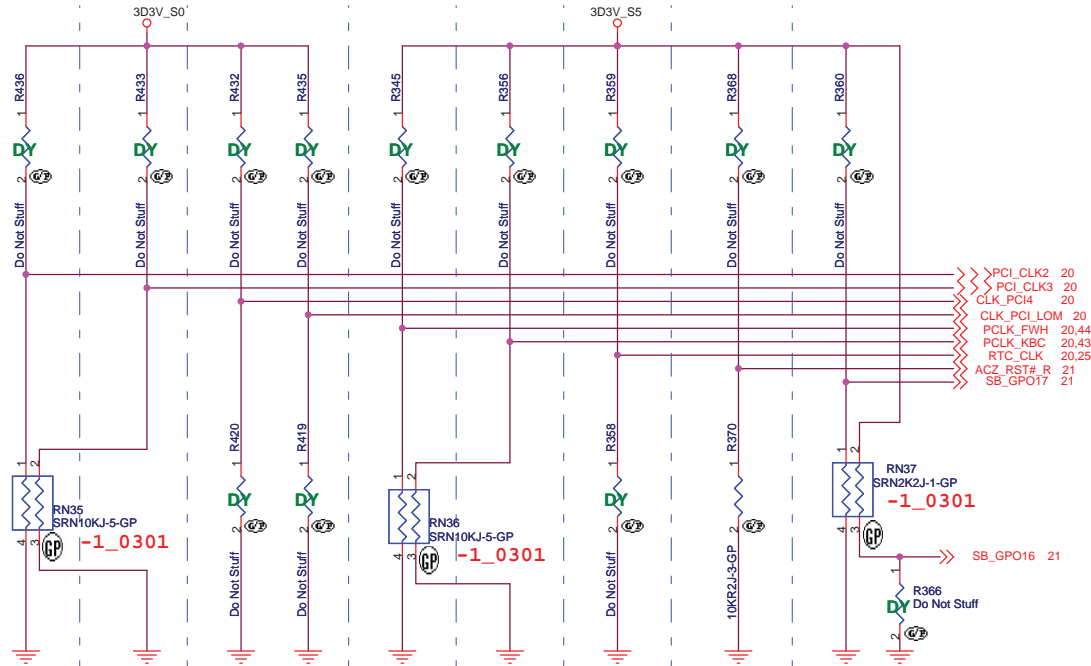




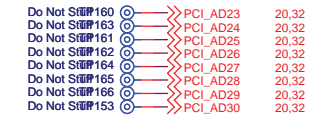


## REQUIRED STRAPS

### REQUIRED SYSTEM STRAPS



## DEBUG STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17, SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI\_AD[30:23]

UMA NODOCK

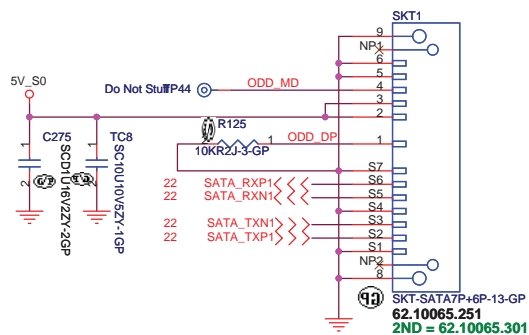
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		<b>ATI-SB700 STRAPPING (5/5)</b>	
Size	Document Number	Rev	
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Date:	Friday, April 18, 2008	Sheet	24 of 58

Olan



## ODD Connector



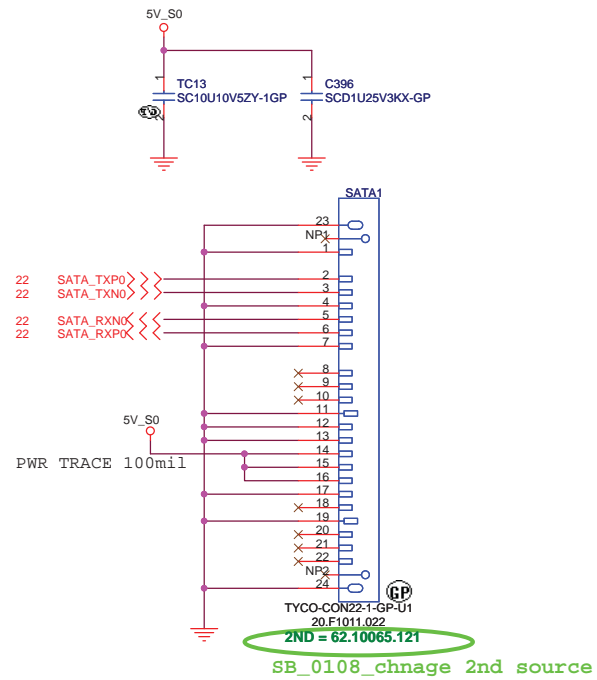
-1\_0305

UMA NODOCK

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Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>CDROM</b>
Size	Document Number	Rev	
		<b>Olan</b>	
Date:	Friday, April 18, 2008	Sheet	26 of 58

## SATA HDD Connector



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**HDD**

Size

Document Number

Rev

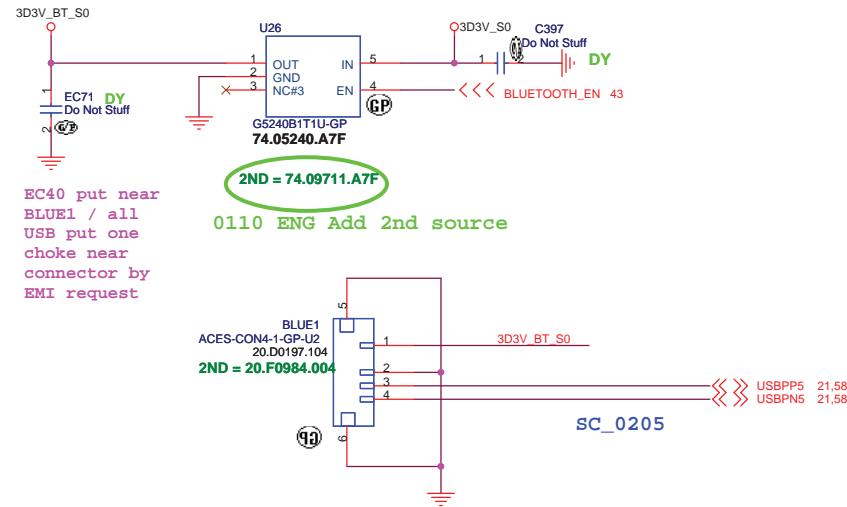
**Olan**

-1

Date: Friday, April 18, 2008

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# BLUETOOTH MODULE

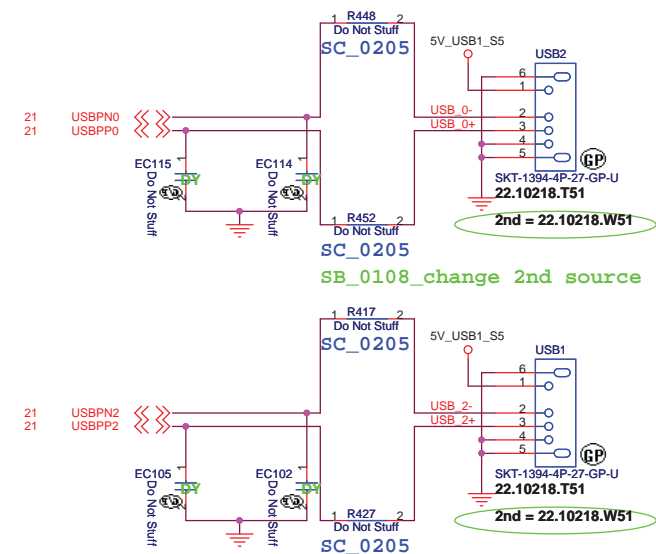
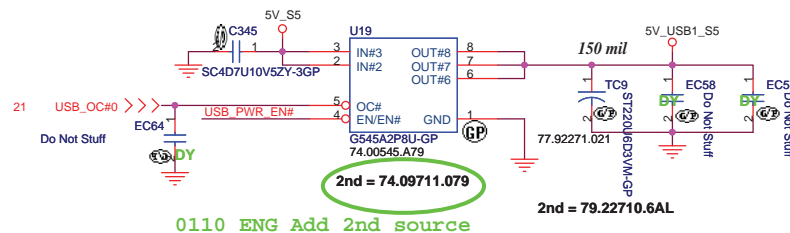


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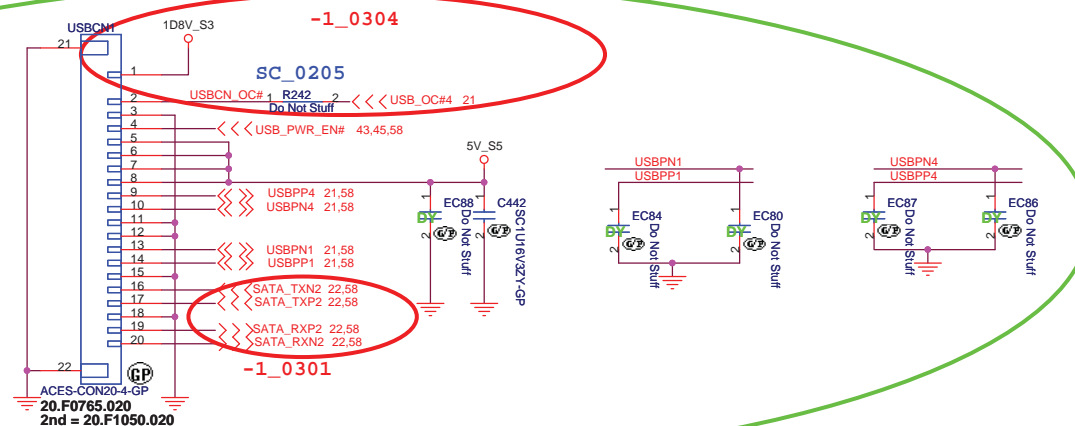
**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			<b>BLUETOOTH</b>	
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SB\_0102



58 USB\_CN\_OC# <<< USB\_CN\_OC#

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Title

USB

Size

Document Number

Rev

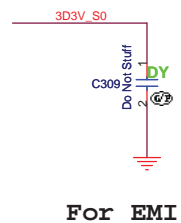
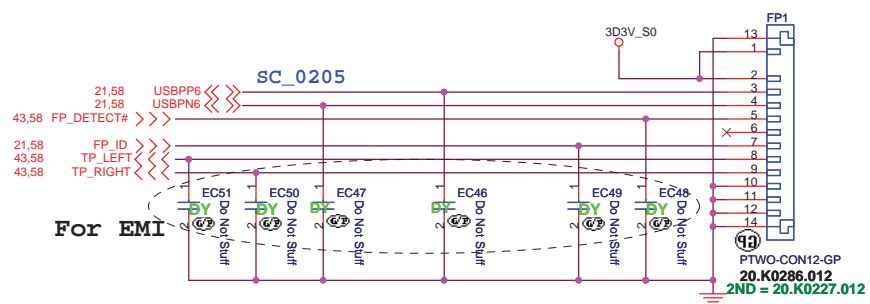
Olan

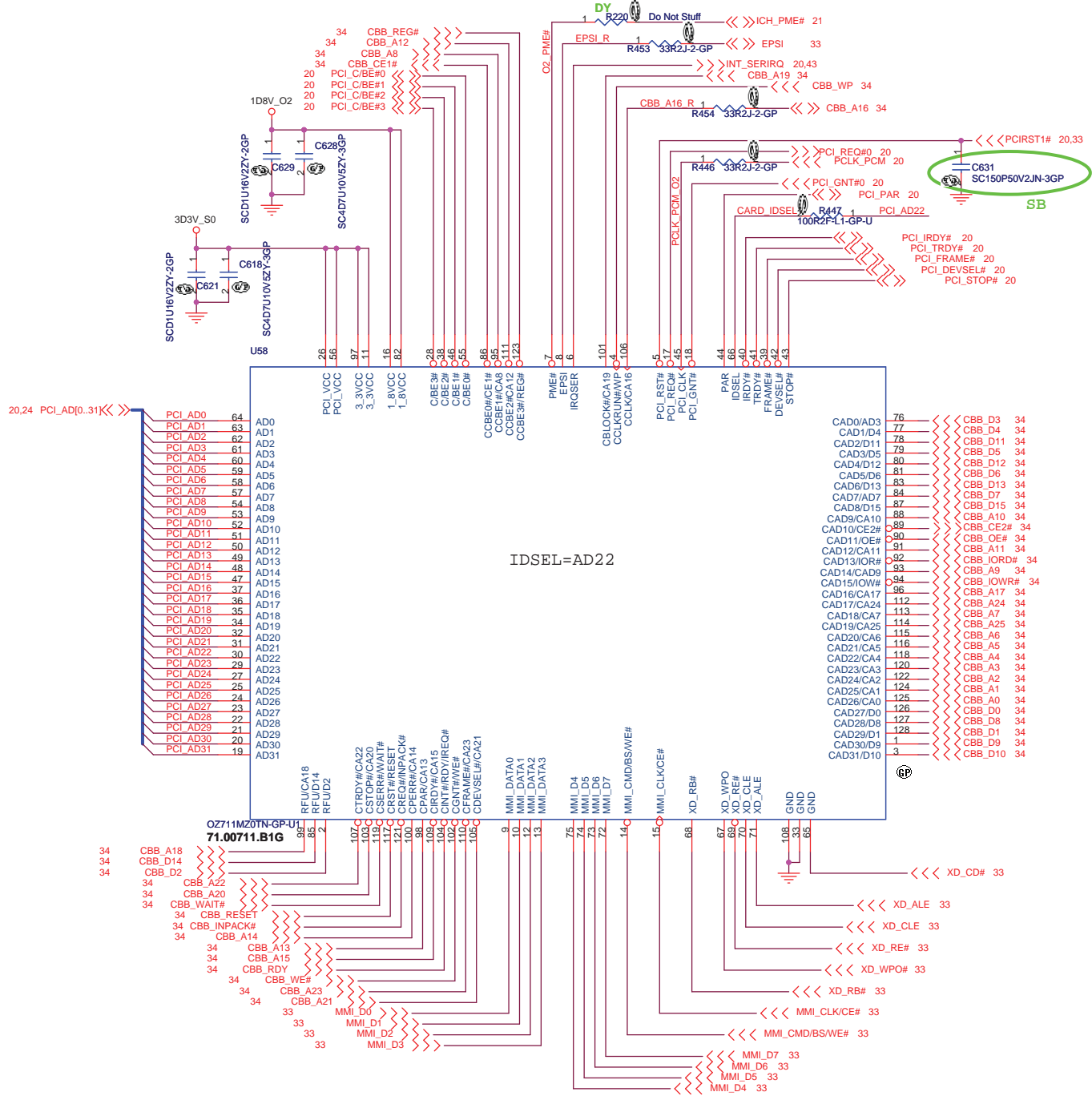
-2M

Date: Monday, May 05, 2008

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## Finger printer

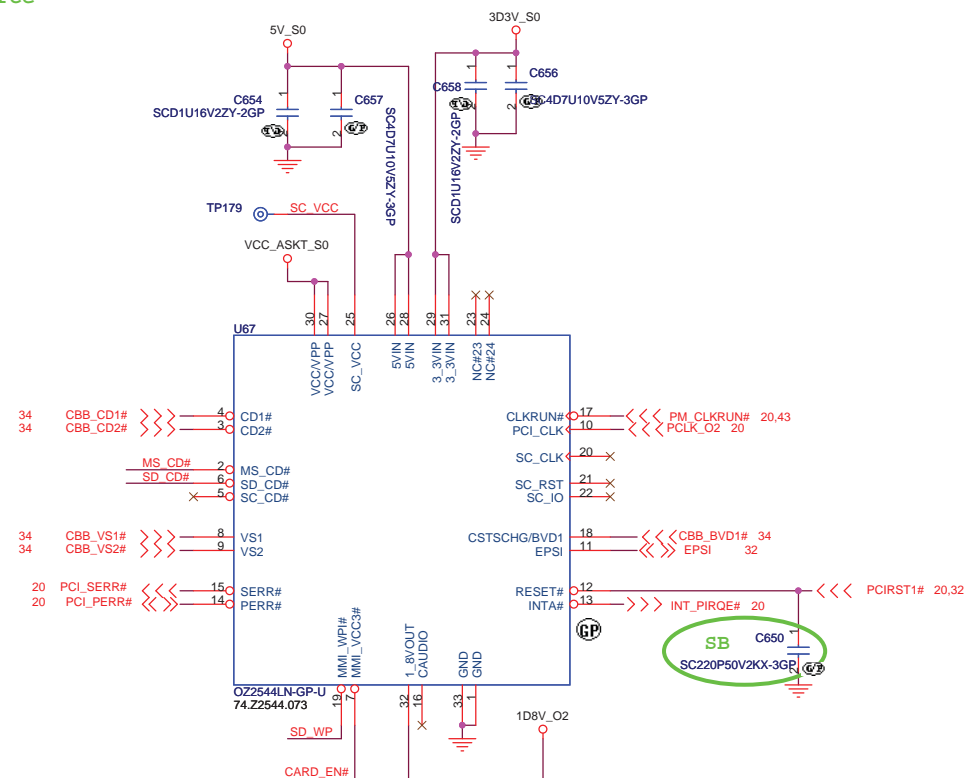
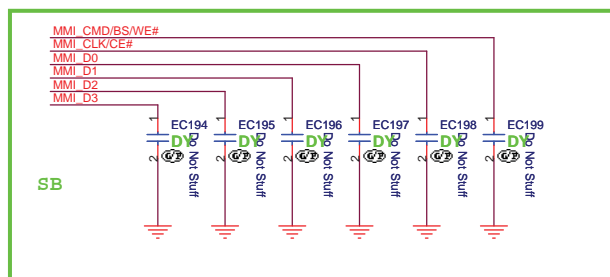




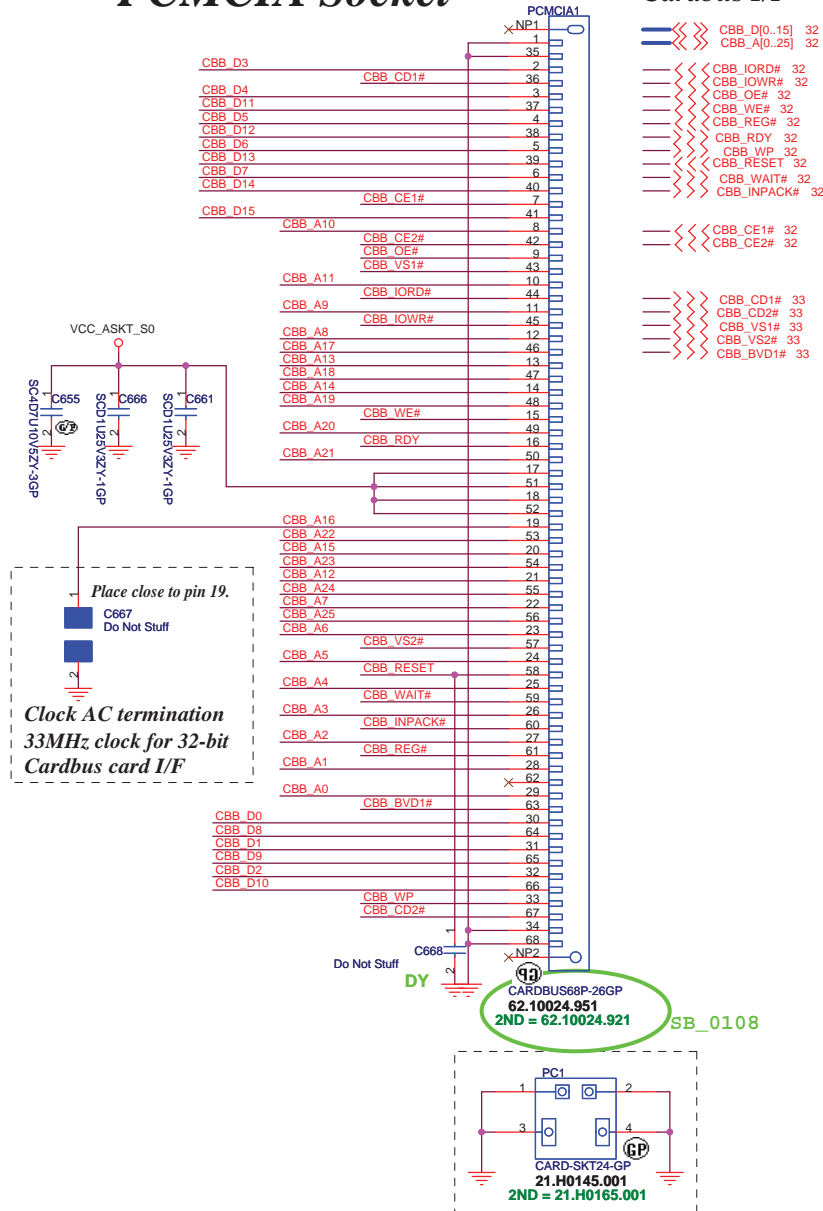
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		OZ711M20	
Size	Document Number	Rev	
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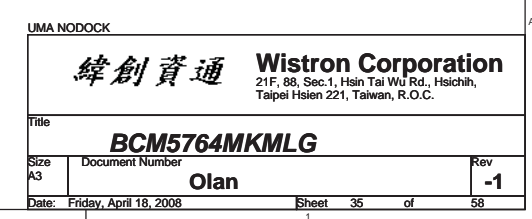
# PCMCIA Socket



UMA NODOCK

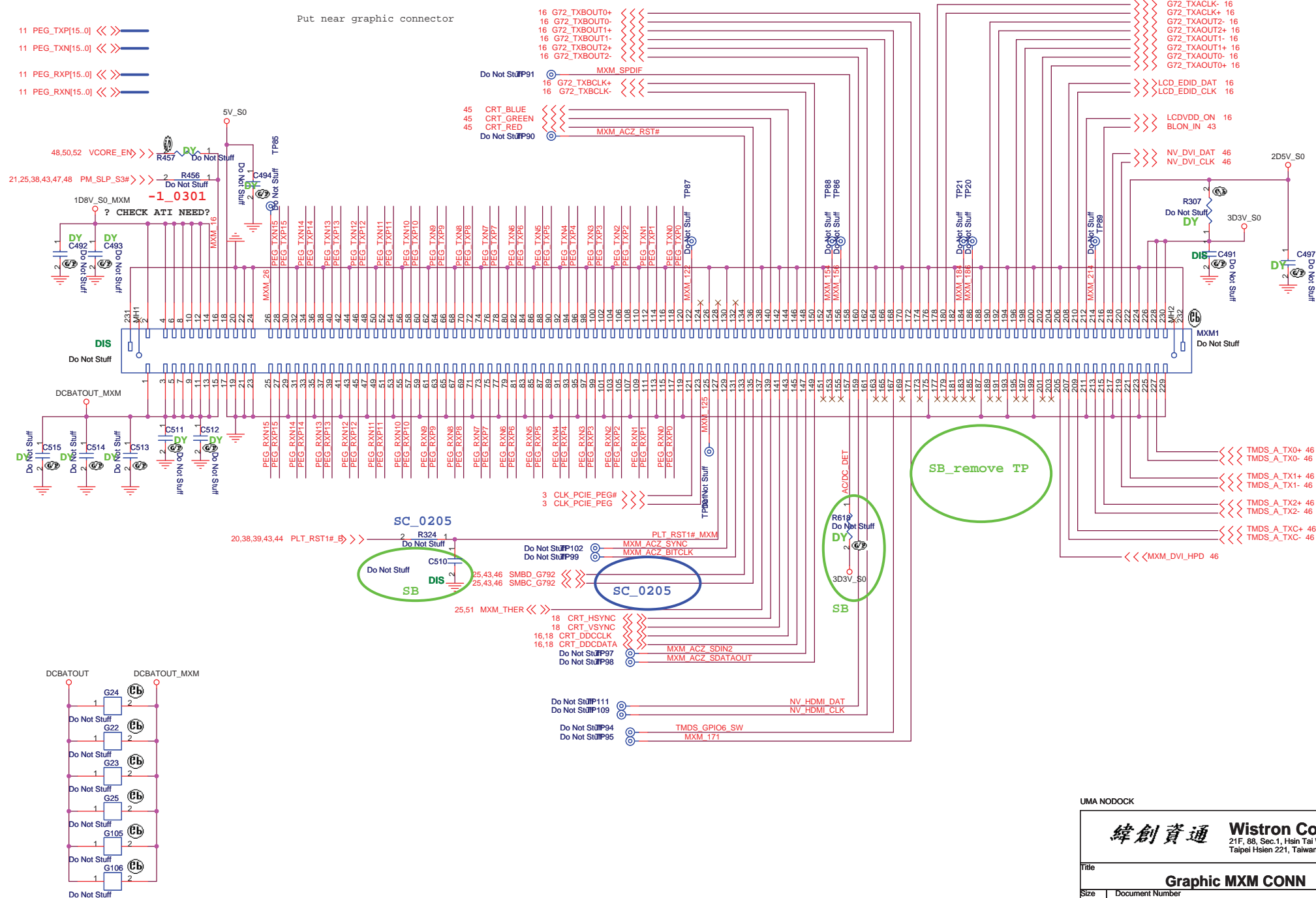
**緯創資通 Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			PCMCIA
Size	Document Number	Rev	
A3	Olan	-1	
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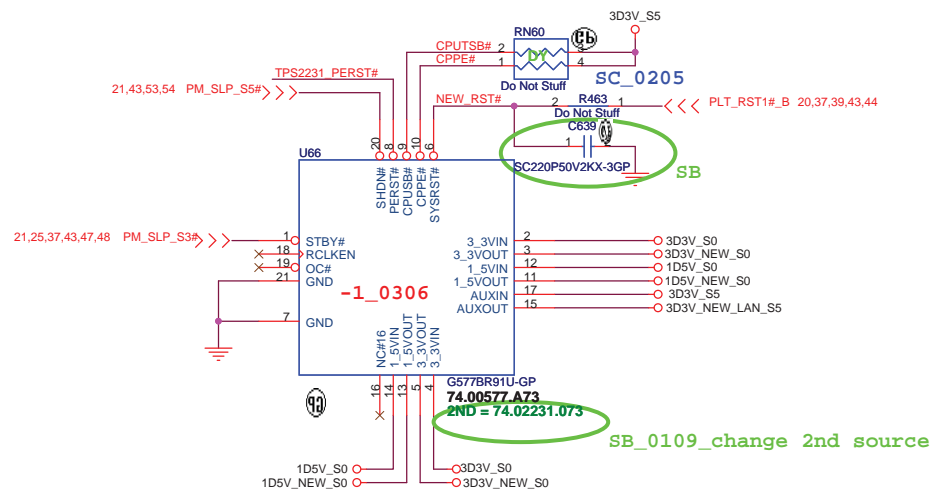
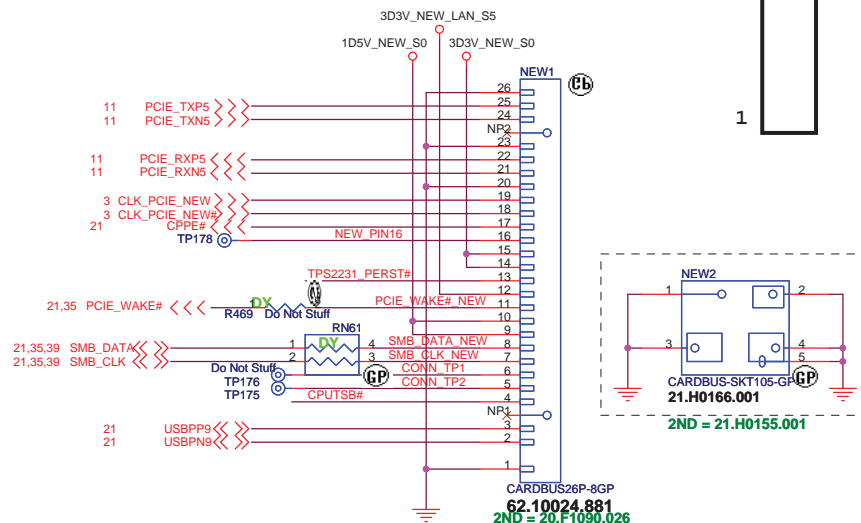


Title			
Graphic MXM CONN			
Size A3	Document Number		Rev -1
Olan			
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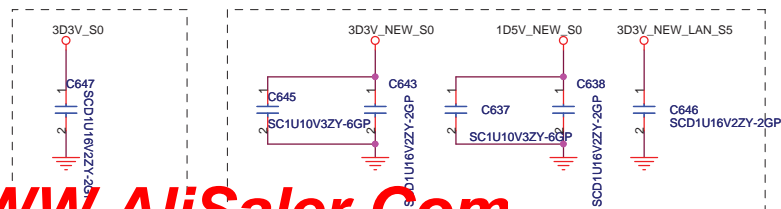


26

1



Place them Near to ChipPlace them Near to Connector



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Title

**NEW CARD**Size  
A2

Document Number

## Olan

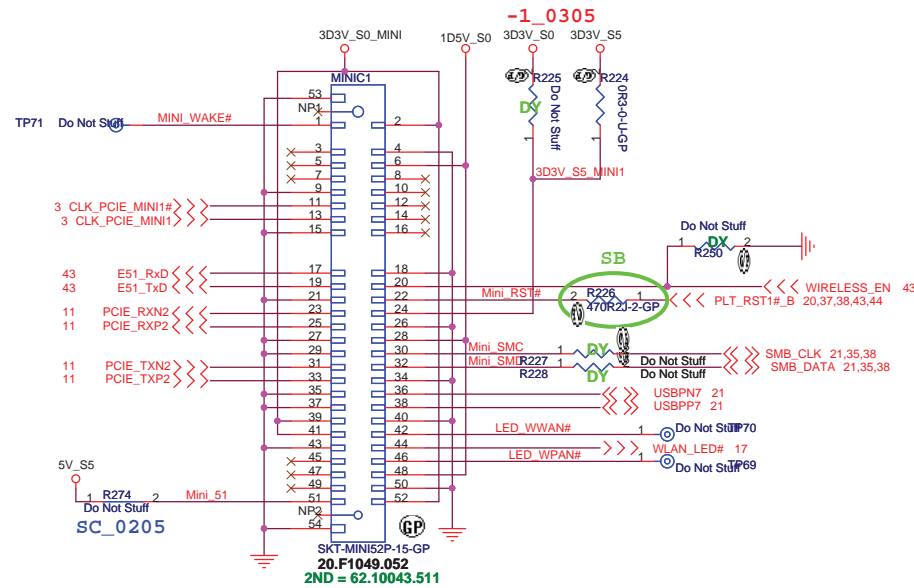
Rev	-1
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Date: Friday, April 18, 2008

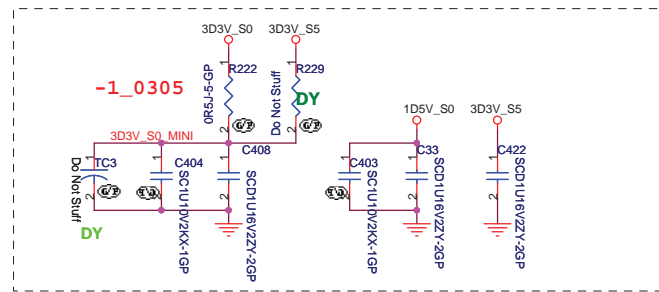
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58

# Mini Card Connector(WLAN)



Place near MINIC1



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Taipei Hsien 221, Taiwan, R.O.C.

Title

**Mini Card**

Size  
**A3**

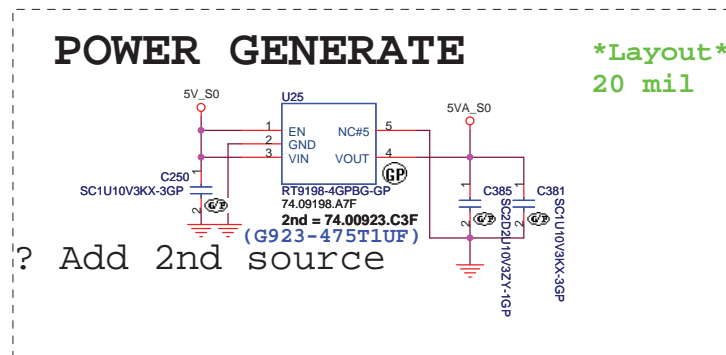
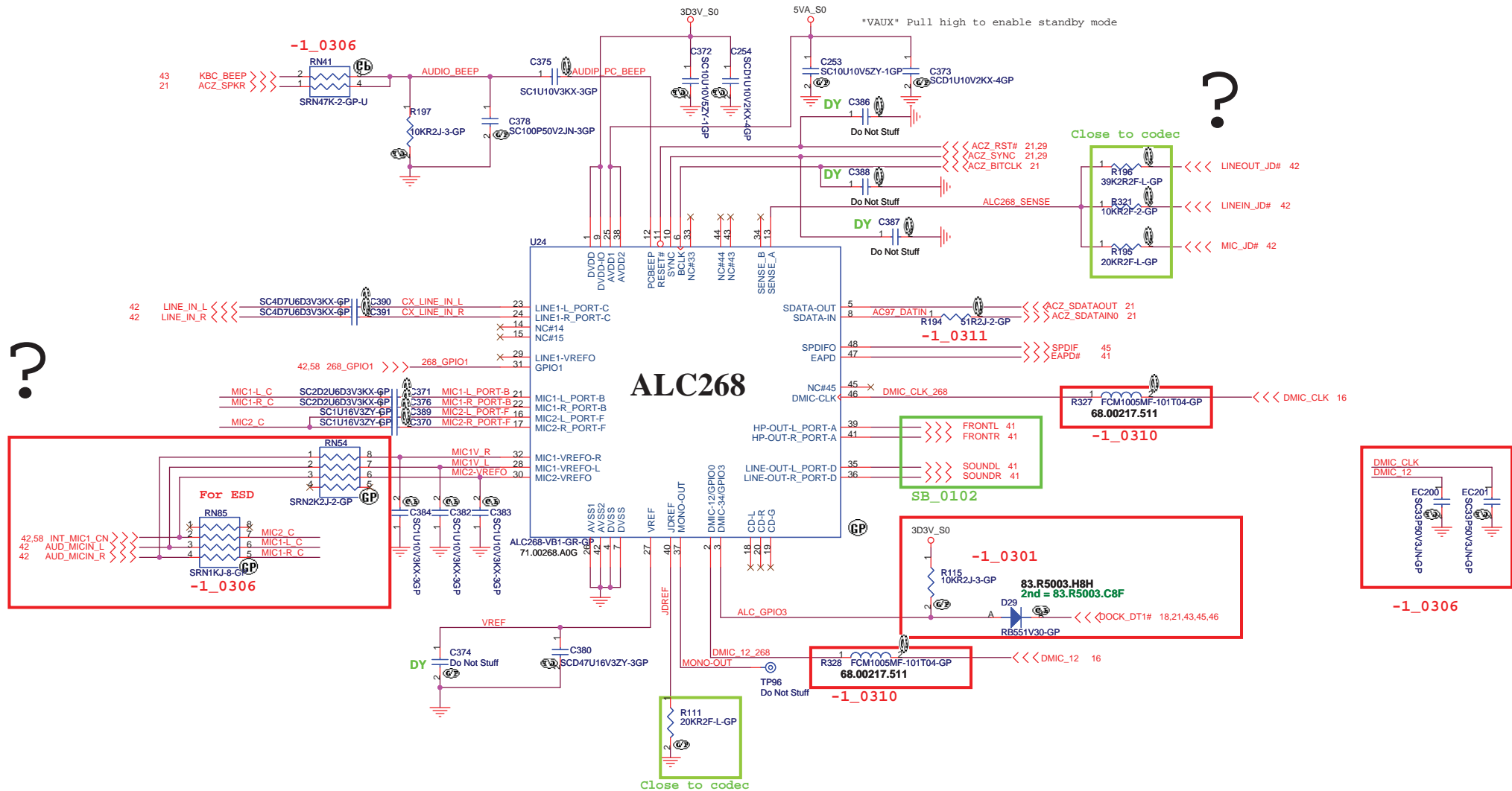
Document Number

**Olan**

Rev  
**-1**

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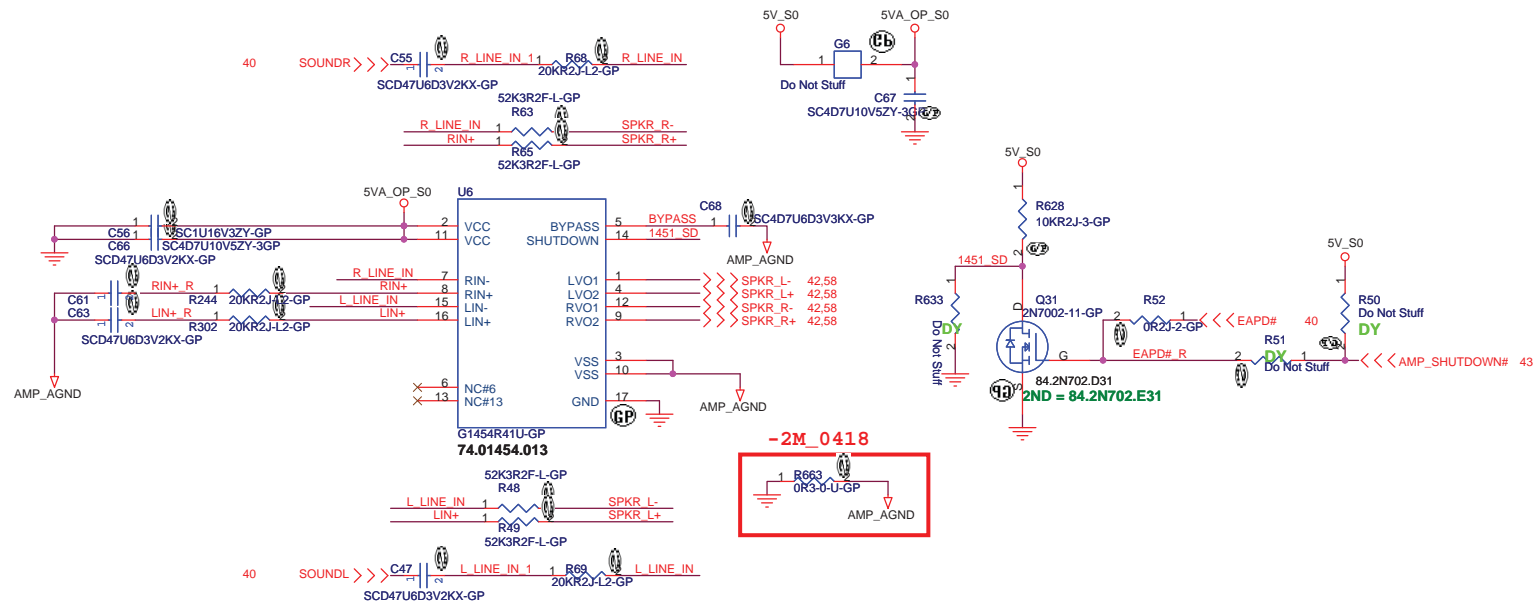
UMA NODOCK

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title Azalia codec ALC268

Size A3	Document Number	Rev -2M
Olan		
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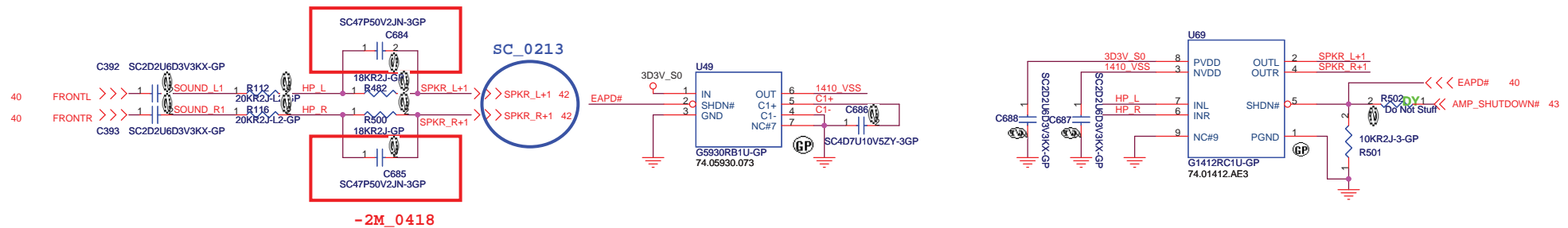
# AUDIO OP AMPLIFIER



SB

KBC\_MUTE\_GPIO8

-2M\_0418

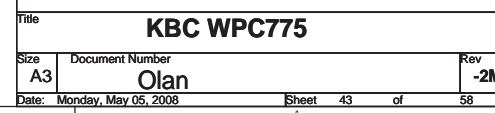


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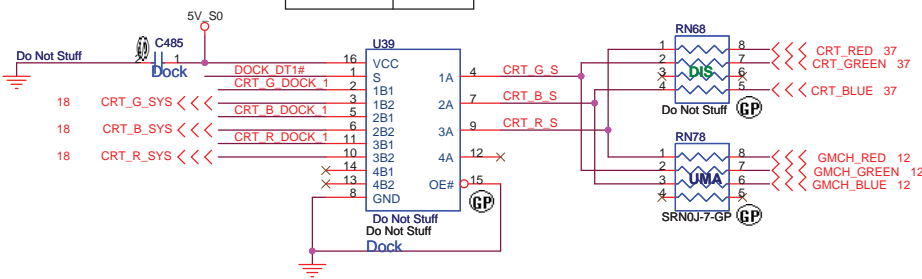
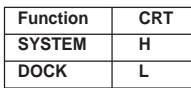
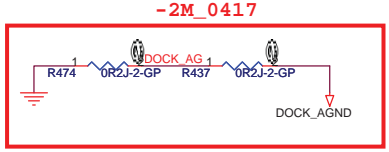
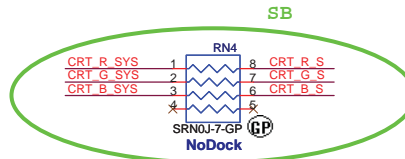
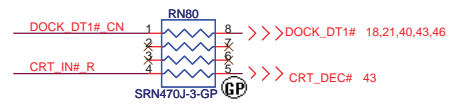
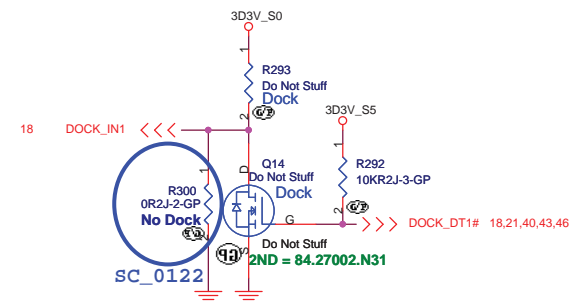
緯創資通 Wistron Corporation  
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
AUDIO AMP		
Size	Document Number	Rev
A3	Olan	-2M
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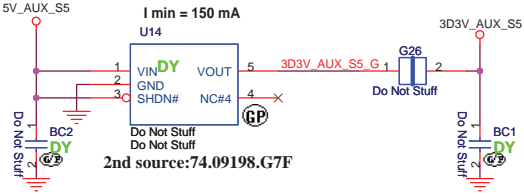




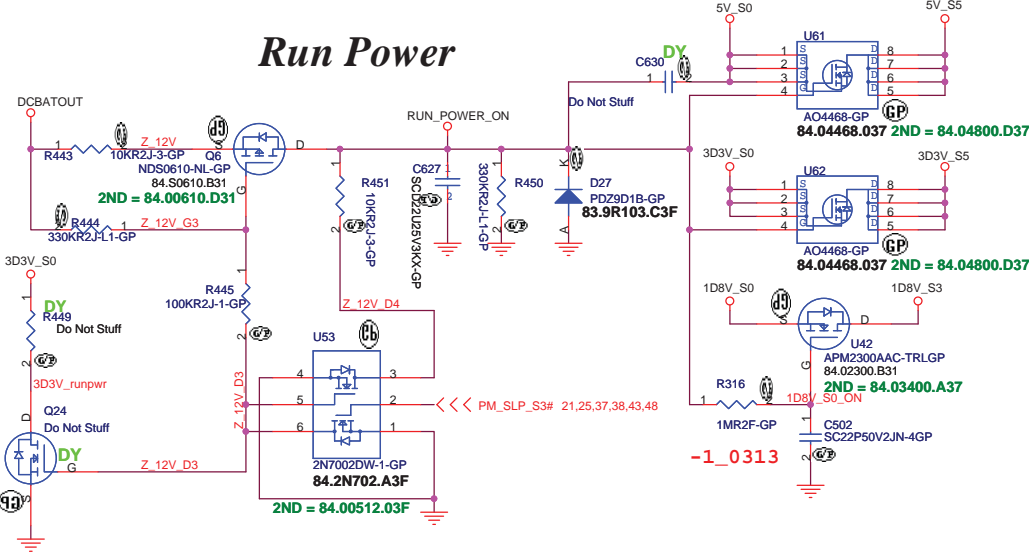


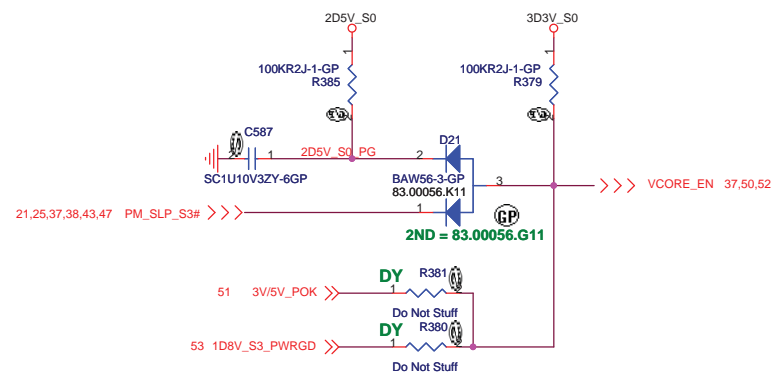


Aux Power 3D3V\_AUX\_S5

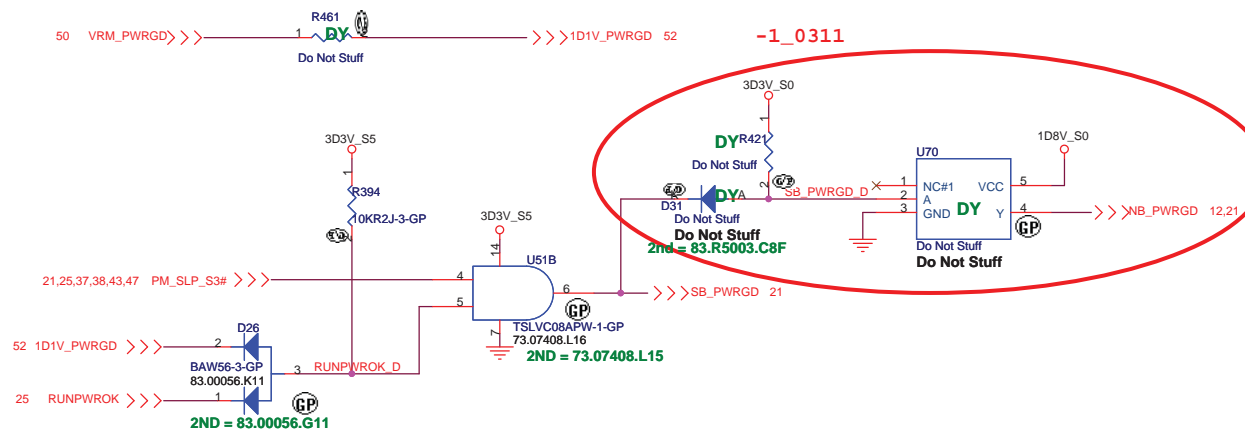


Run Power





# P/H @ 1D8V\_S3 PAGE

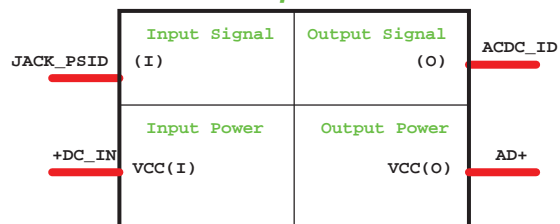


UMA NODOCK

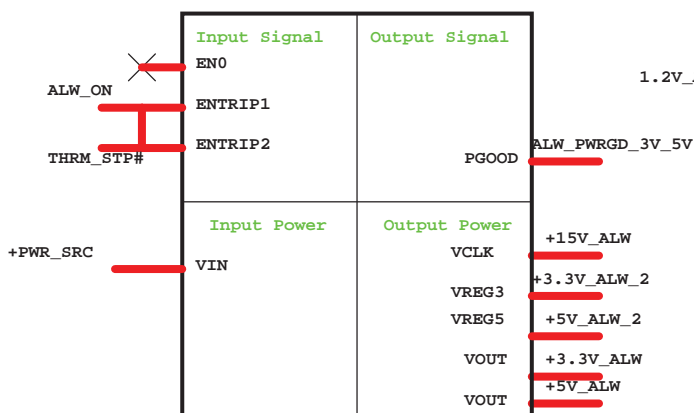
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		POWER ON LOGIC	
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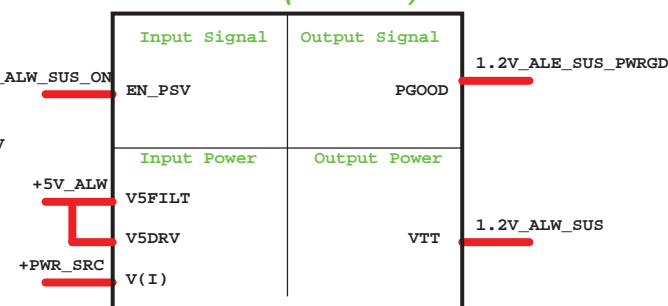
## Adapter



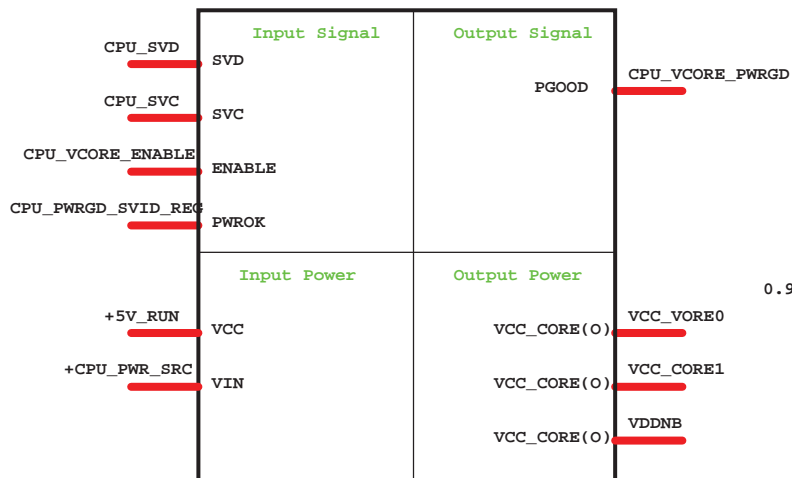
## SN0608098



## DCDC 1D2V(TPS5117)

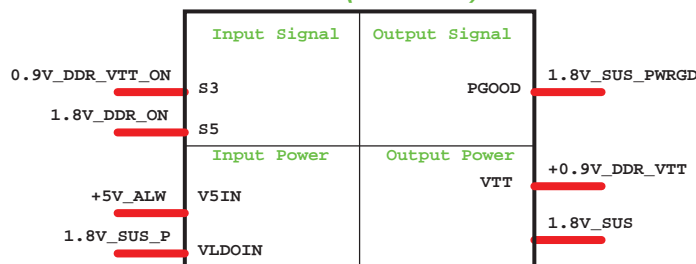


## CPU\_CORE ISL6265HRTZ

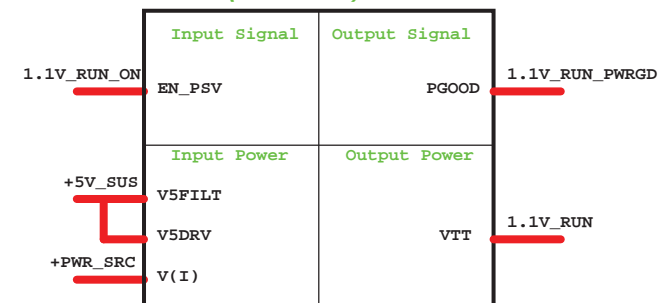


	S3	S5	VDDQ	VTTREF	VTT
S0	1	1	1	1	1
S4	0	0	0	0	0

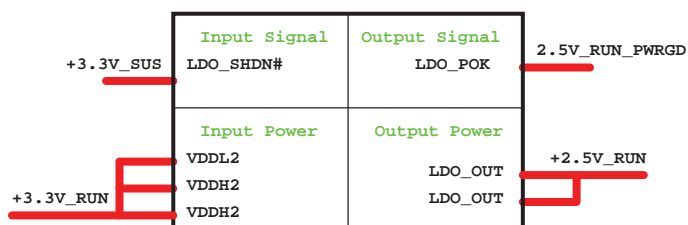
## 1D8V/0D9V(TPS5116)



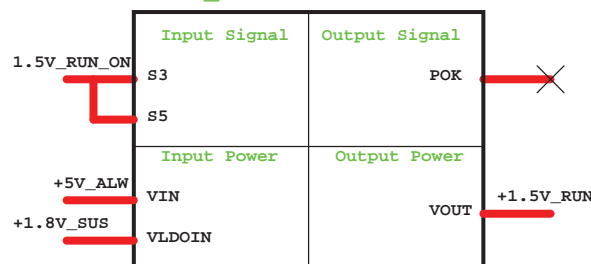
## 1D1V(TPS5117)



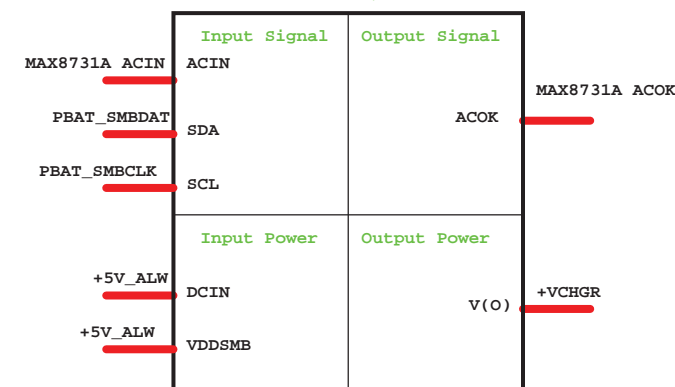
## 2.5V LDO EMC4002



## 1.5V LDO



## CHARGER BQ24745



UMA NODOCK

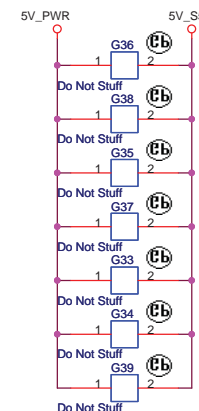
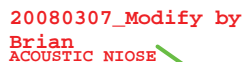
緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title Power Block Diagram

Size A3 Document Number Olan Rev -1  
Date: Friday, April 18, 2008 Sheet 49 of 58



**Brian**  
ACOUSTIC NIOSE

[illegible]

**緯創資通** **Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Size <b>A3</b>	Document Number <b>Olan</b>	Rev <b>-2M</b>
Date: Monday, May 05, 2008	Sheet 51 of 58	

20080307\_Modify by

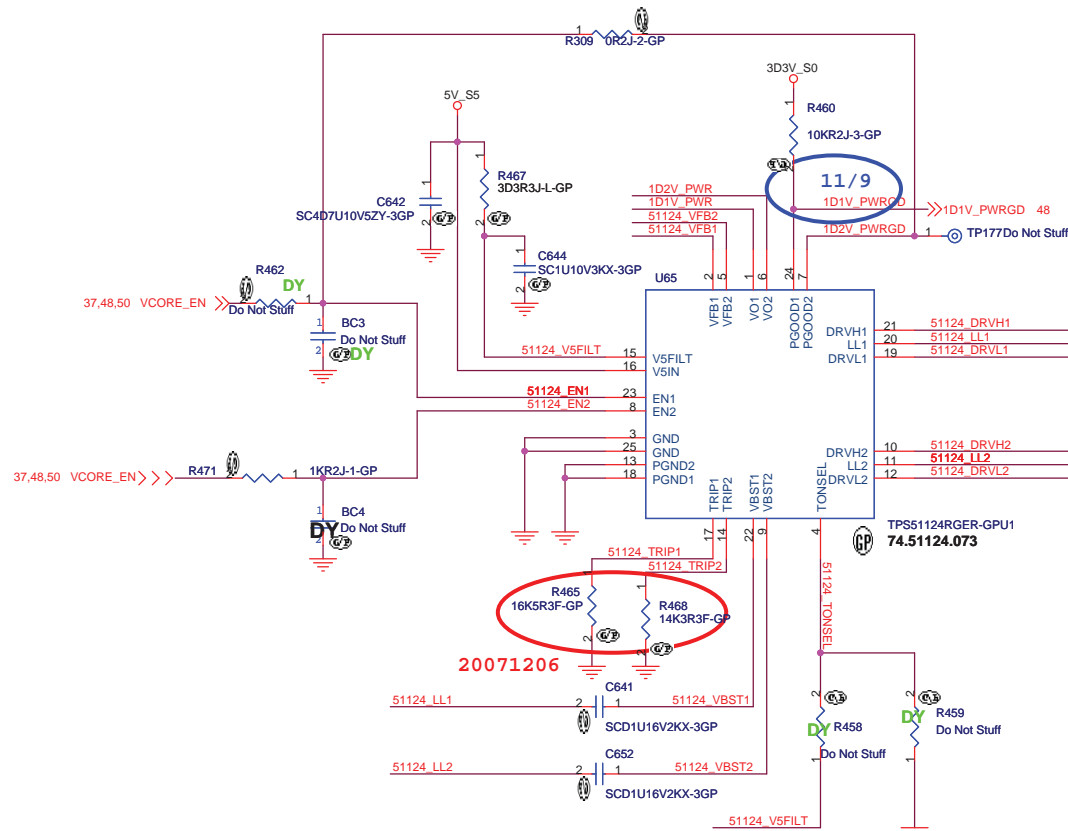
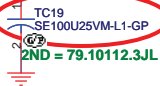
Brian  
ACOUSTIC NIOSE

$$V_{trip}(mV) = R_{trip}(K\Omega) * 10(\mu A)$$

$$I_{ocp} = (V_{trip}/R_{dson}) + ((1/(2 * L * f)) * ((V_{in} - V_{out}) * V_{out}) / V_{in}))$$

I/P cap: 10U 25V K1206 X5R/ 78.10622.52L

-1\_0306

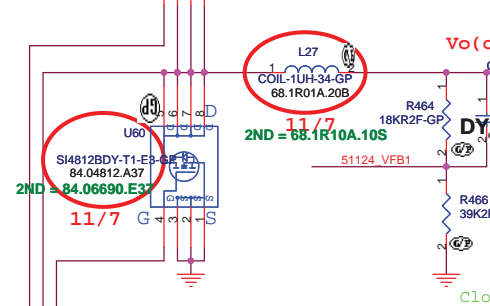
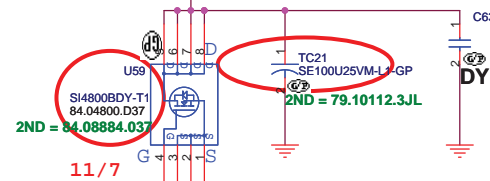


	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

$V_{out} = 0.758V * (R1 + R2) / R2$  --> PWM mode  
 $V_{out} = 0.764V * (R1 + R2) / R2$  --> Skip Mode

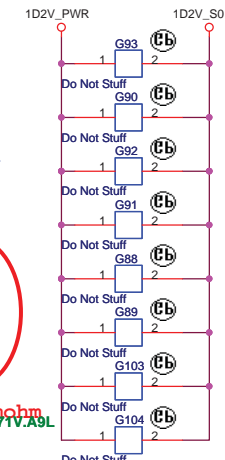
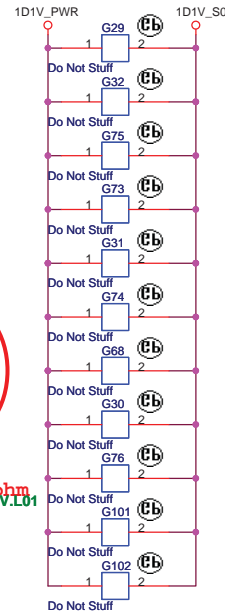
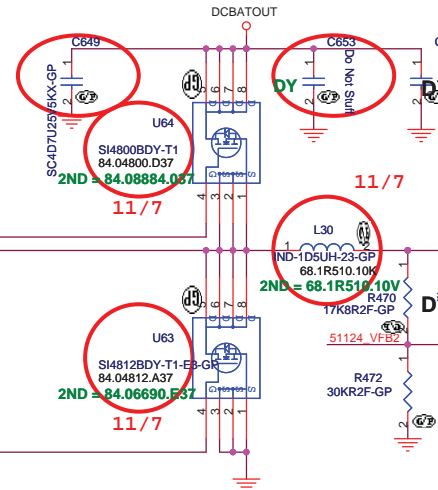
20080307\_Modify by

Brian  
ACOUSTIC NIOSE



20080307\_Modify by

Brian  
ACOUSTIC NIOSE

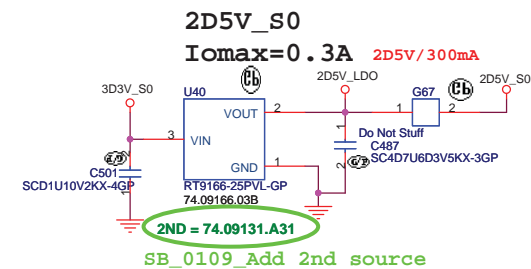
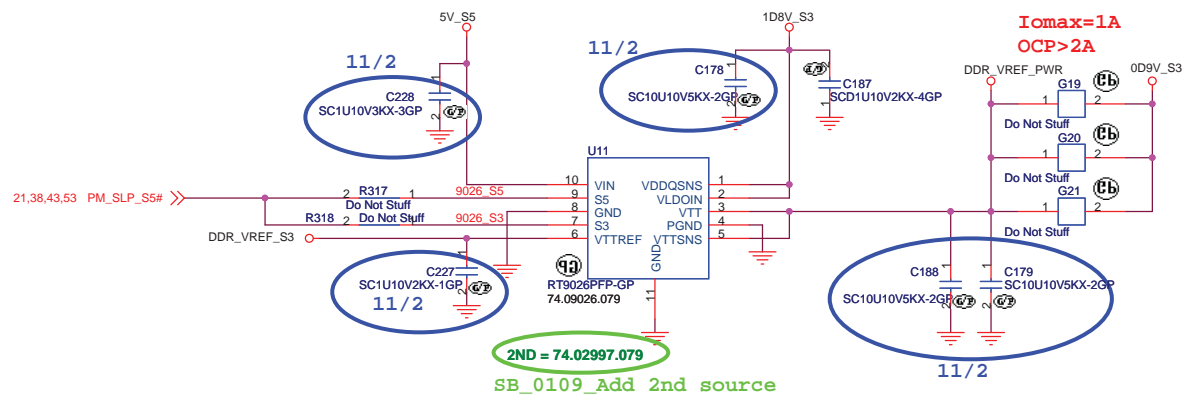
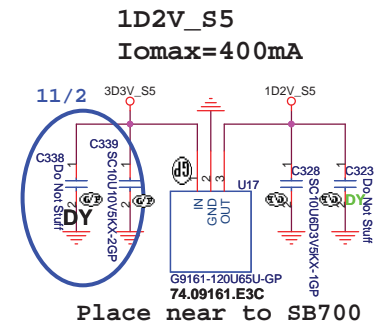
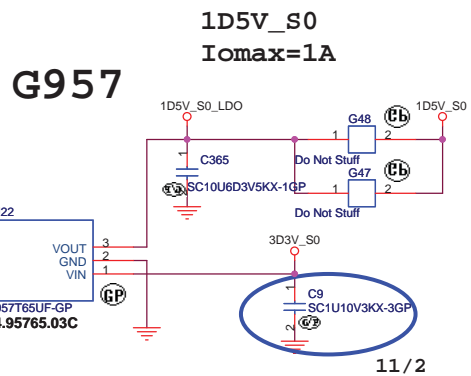


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Title		TPS51124 1D1V 1D2V	
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Title		<b>0D9V&amp;2D5V&amp;1D25V&amp;1D5V</b>	
Size A3	Document Number	Olan	
Date: Friday, April 18, 2008	Sheet 54 of 58	Rev -1	



Jeff modify 20071031



## BATTERY CONNECTOR



UMA NODOCK

**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title
-------

**AD/BATT CONN**

Size  
A4

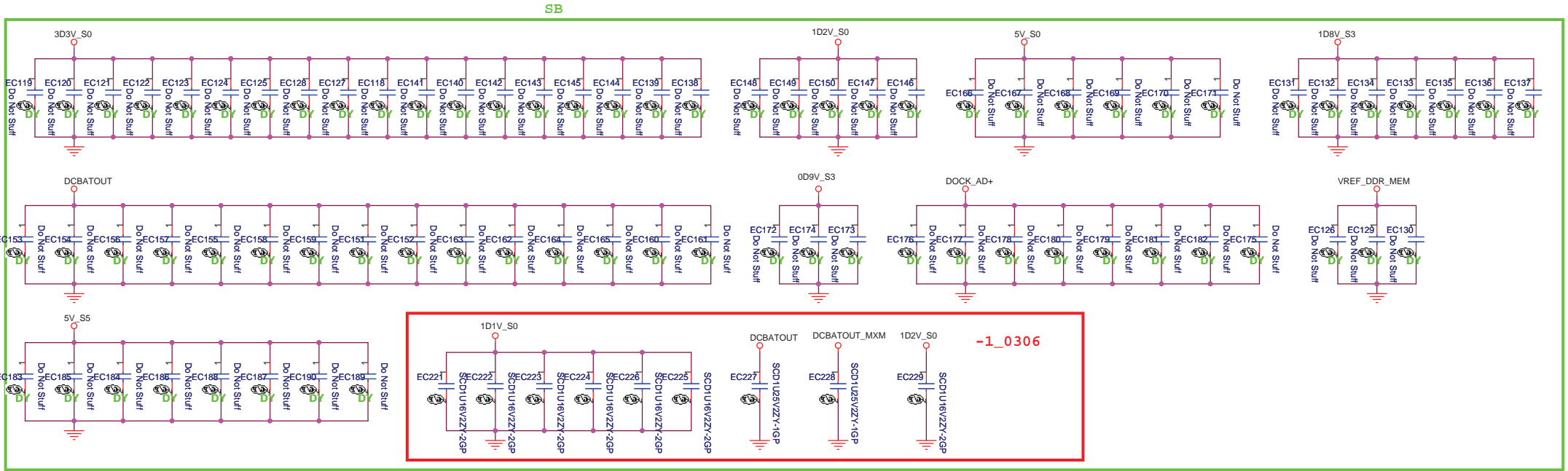
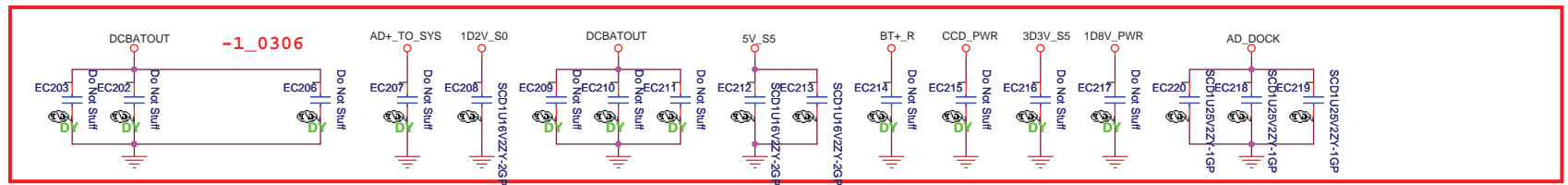
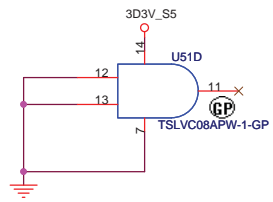
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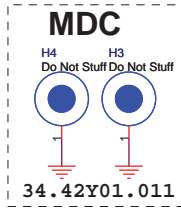
Rev	-1
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Date: Tuesday, April 29, 2008

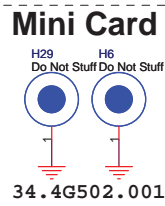
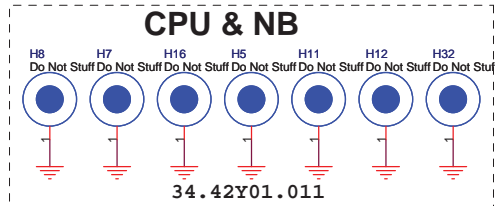
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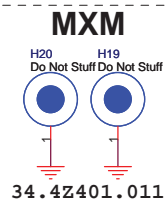
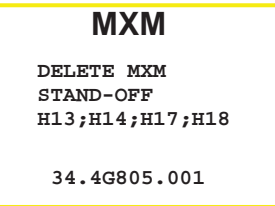
STAND OFF ON TOP



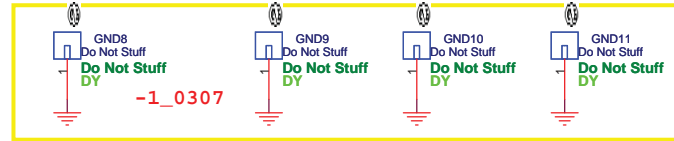
STAND OFF ON BOTTOM



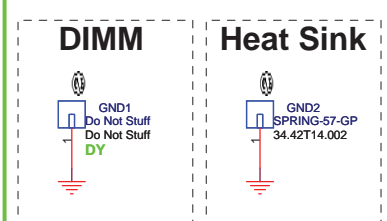
20080307\_Modify by Brian



MXM SPRING -1 20080307



SPRING ON BOTTOM



Check test point

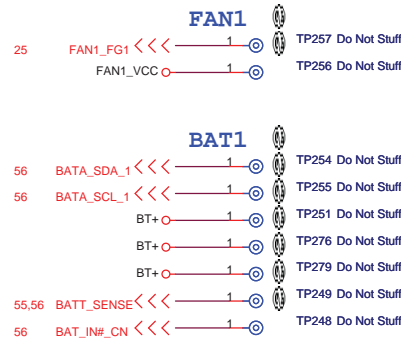
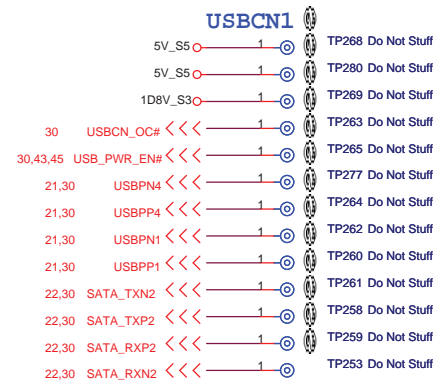
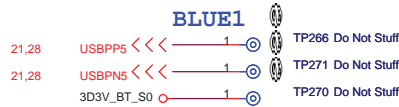
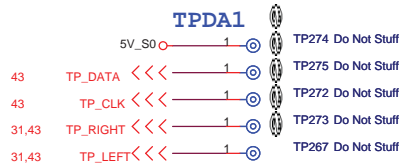
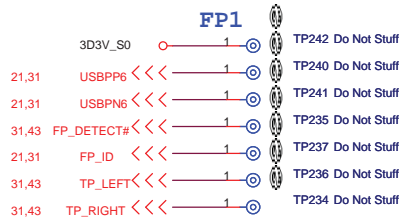
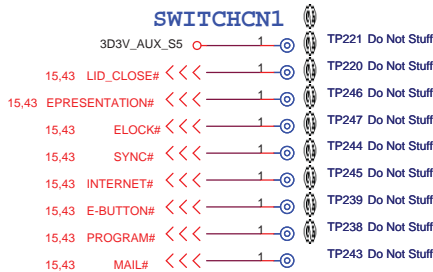
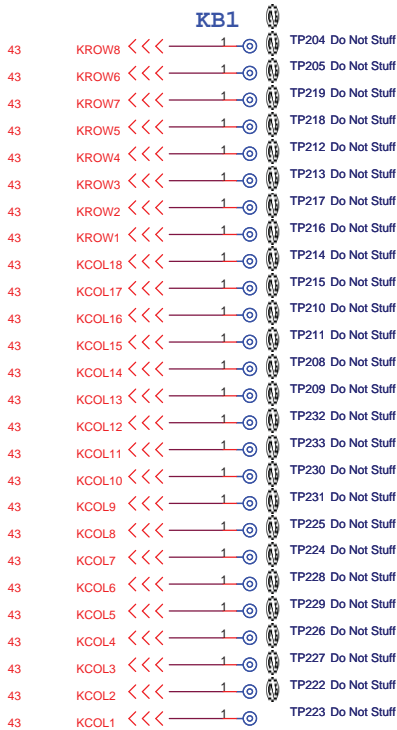
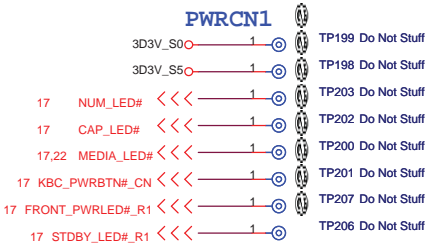
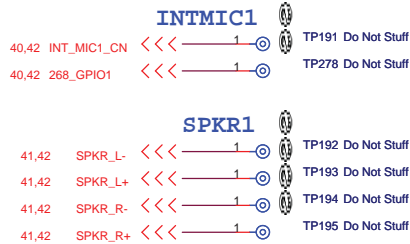
- 3D3V\_S0 TP180 Do Not Stuff
- 3D3V\_AUX\_S5 TP4 Do Not Stuff
- 3D3V\_S5 TP183 Do Not Stuff
- 5V\_S5 TP186 Do Not Stuff
- 21.43 PM\_PWRBTN# TP185 Do Not Stuff
- 6.20 CPU\_PWRGD TP184 Do Not Stuff
- 25.43 SS\_ENABLE TP181 Do Not Stuff
- 6.20 CPU\_LDT\_RST# TP182 Do Not Stuff

Test Point放在Dimm Door打開可量測處

UMA NODOCK

緯創資通 Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title			
EMI/Spring/Boss			
Size	Document Number		Rev
A3	Olan		-1
Date:	Monday, April 21, 2008		Sheet 57 of 58



UMA NODOCK

<b>緯創資通</b>			<b>Wistron Corporation</b>		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.					
Title					
<b>AFTE TP</b>					
Size A3	Document Number				Rev
	<b>Olan</b>				<b>-2M</b>
Date: Monday, May 05, 2008	Sheet	58	of	58	