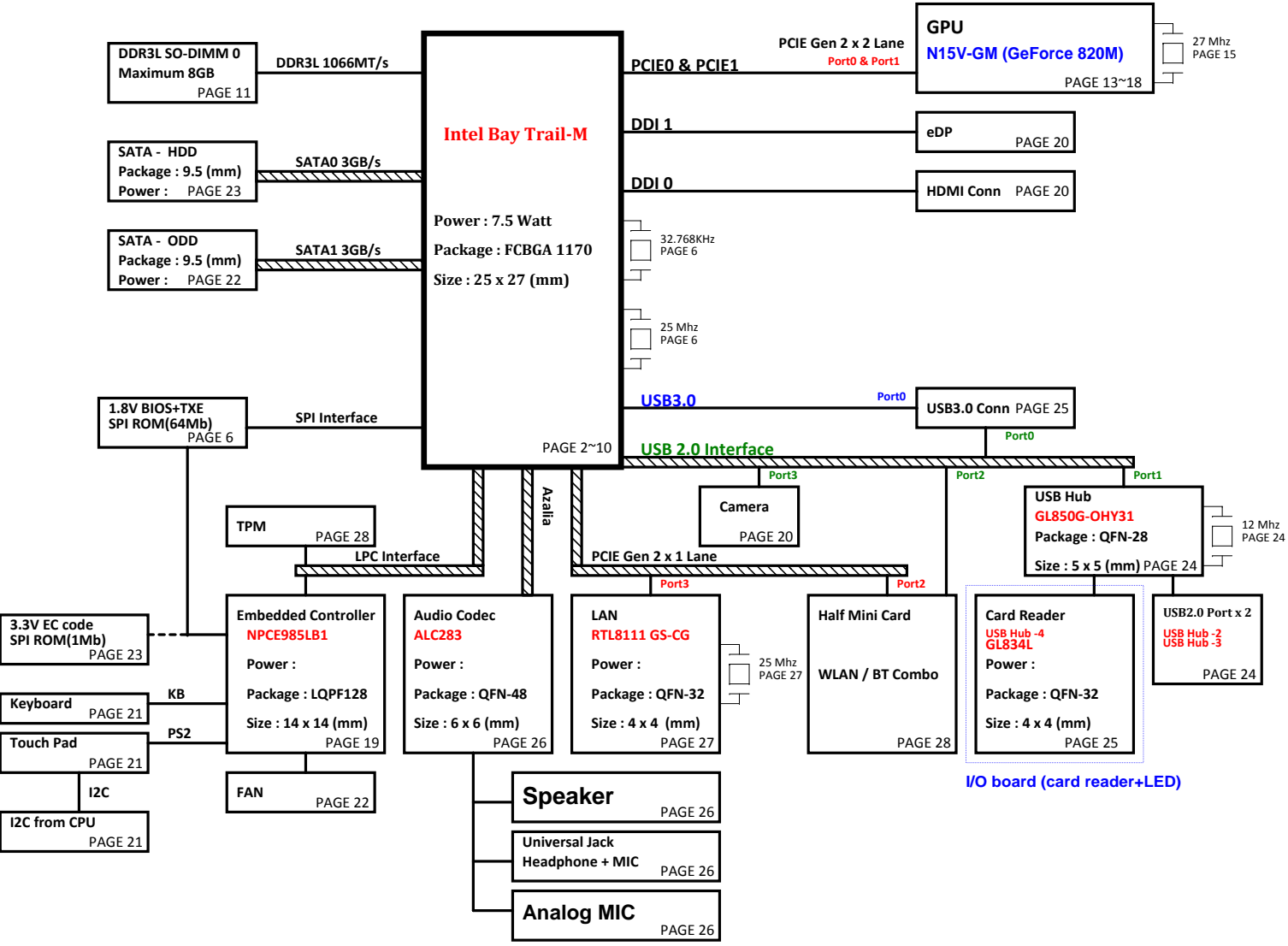


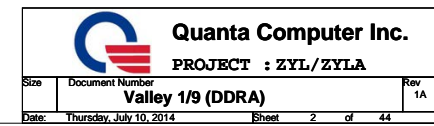
ZYL (17")

Intel Bay Trail-M Platform Block Diagram

PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SGND
LAYER 6 : BOT





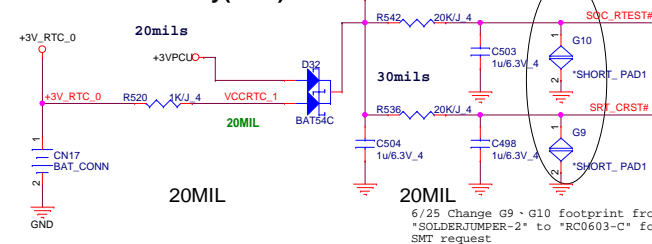
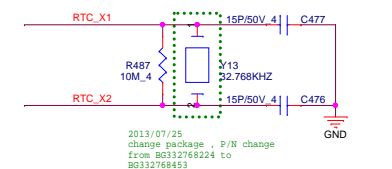
U29B

AY45	DRAM1_MA_00	DRAM1_DQ_00	BG38
BB47	DRAM1_MA_11	DRAM1_DQ_11	BD40
AW46	DRAM1_MA_22	DRAM1_DQ_22	BA42
BB44	DRAM1_MA_33	DRAM1_DQ_33	BD42
BC45	DRAM1_MA_44	DRAM1_DQ_44	BC38
BC45	DRAM1_MA_55	DRAM1_DQ_55	BC36
BB40	DRAM1_MA_66	DRAM1_DQ_66	BF42
BF40	DRAM1_MA_77	DRAM1_DQ_77	BC44
BC42	DRAM1_MA_88	DRAM1_DQ_88	BH32
BE45	DRAM1_MA_99	DRAM1_DQ_99	BC32
AY48	DRAM1_MA_1010	DRAM1_DQ_1010	BG36
BD47	DRAM1_MA_1111	DRAM1_DQ_1111	BH37
BAG1	DRAM1_MA_1212	DRAM1_DQ_1212	BG33
BH40	DRAM1_MA_1313	DRAM1_DQ_1313	BG37
BH40	DRAM1_MA_1414	DRAM1_DQ_1414	BH38
BH40	DRAM1_MA_1515	DRAM1_DQ_1515	BH36
BD38	DRAM1_DM_00	DRAM1_DQ_1616	AT36
BH36	DRAM1_DM_11	DRAM1_DQ_1717	AV40
BC36	DRAM1_DM_22	DRAM1_DQ_1818	AT40
BH42	DRAM1_DM_33	DRAM1_DQ_1919	BH36
AT40	DRAM1_DM_44	DRAM1_DQ_2020	AV36
AM42	DRAM1_DM_55	DRAM1_DQ_2121	AV42
AK40	DRAM1_DM_66	DRAM1_DQ_2222	AV40
AK42	DRAM1_DM_77	DRAM1_DQ_2323	BH41
AV43	DRAM1_RAS	DRAM1_DQ_2424	BG41
AV43	DRAM1_CAS	DRAM1_DQ_2525	BH45
BB47	DRAM1_WE	DRAM1_DQ_2626	BH46
AY47		DRAM1_DQ_2727	BG40
AY46	DRAM1_BS_00	DRAM1_DQ_2828	BH40
BF42	DRAM1_BS_11	DRAM1_DQ_2929	BH48
AT44	DRAM1_BS_22	DRAM1_DQ_3030	BH47
AT44	DRAM1_CS_0	DRAM1_DQ_3131	AV52
AT45	DRAM1_CS_2	DRAM1_DQ_3232	AV51
		DRAM1_DQ_3333	AV52
		DRAM1_DQ_3434	AP51
		DRAM1_DQ_3535	AV51
		DRAM1_DQ_3636	AV53
		DRAM1_DQ_3737	AP51
		DRAM1_DQ_3838	AP53
BG47	DRAM1_CKE_00	DRAM1_DQ_3939	AP47
BE46	RESERVED_BE46	DRAM1_DQ_4040	AP45
BD44	DRAM1_CKE_22	DRAM1_DQ_4141	AK40
BF46	RESERVED_BF48	DRAM1_DQ_4242	AM41
AP41	DRAM1_ODT_0	DRAM1_DQ_4343	AP48
AT42	DRAM1_ODT_2	DRAM1_DQ_4444	AP50
		DRAM1_DQ_4545	AK42
		DRAM1_DQ_4646	BH40
AV50		DRAM1_DQ_4747	AM45
AV48	DRAM1_CKP_0	DRAM1_DQ_4848	AM47
AV48	DRAM1_CKN_0	DRAM1_DQ_4949	BF48
		DRAM1_DQ_5050	BF50
		DRAM1_DQ_5151	AM48
		DRAM1_DQ_5252	AM50
AT50	DRAM1_CKP_2	DRAM1_DQ_5353	BH44
AT48	DRAM1_CKN_2	DRAM1_DQ_5454	AK45
		DRAM1_DQ_5555	AM52
		DRAM1_DQ_5656	AL51
		DRAM1_DQ_5757	BG53
AT41	DRAM1_DRAMRST	DRAM1_DQ_5858	BG51
		DRAM1_DQ_5959	AL53
		DRAM1_DQ_6060	AK51
		DRAM1_DQ_6161	BF52
		DRAM1_DQ_6262	BF51
		DRAM1_DQ_6363	
		DRAM1_DQSP_00	BF40
		DRAM1_DQSN_00	BD40
		DRAM1_DQSP_11	BG35
		DRAM1_DQSN_11	BH34
		DRAM1_DQSP_22	BA38
		DRAM1_DQSN_22	AT38
		DRAM1_DQSP_33	BH44
		DRAM1_DQSN_33	BG43
		DRAM1_DQSP_44	BH53
		DRAM1_DQSN_44	AV52
		DRAM1_DQSP_55	AP42
		DRAM1_DQSN_55	AP44
		DRAM1_DQSP_66	AK47
		DRAM1_DQSN_66	AK48
		DRAM1_DQSP_77	BH52
		DRAM1_DQSN_77	BH51

2 OF 13

VLV_M_D/BGA
REV = 1.15





+1.8V_S5 [6,9,12,21,37]
+1.8V [4,5,6,9,12,19,20,21,27,28,37]
+3V [4,5,9,11,12,13,17,19,20,22,24,25,26,27,28,35,37,39,40]

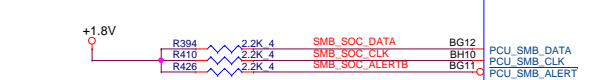
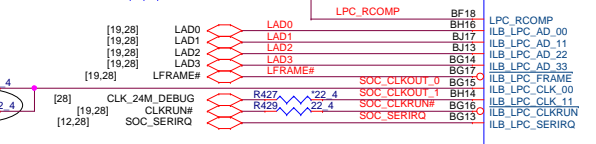
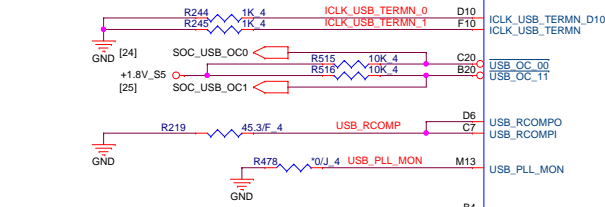
Port 1 is debug port

USB3.0

USB 2.0 HUB

Bluetooth

CAMERA



PJ4N3KDW

U29F

G2 GPIO_S5_31
M3 GPIO_S5_32
K2 GPIO_S5_33
K3 GPIO_S5_34
M2 GPIO_S5_35
N3 GPIO_S5_36
P2 GPIO_S5_37
L3 GPIO_S5_38
X3 GPIO_S5_39

J3 GPIO_S5_40
P3 GPIO_S5_41
H3 GPIO_S5_42
B12 GPIO_S5_43

M16 USB_DP0
K16 USB_DN0
J14 USB_DP1
G14 USB_DN1
K12 USB_DP2
J12 USB_DN2
K10 USB_DP3
H10 USB_DN3

D10 ICLK_USB_TERM0
F10 ICLK_USB_TERM1
C20 USB_OC_00
B20 USB_OC_11

D6 USB_RCOMP0
C7 USB_RCOMP1
M13 USB_PLL_MON

B4 USB_HSIC0_DATA
B6 USB_HSIC0_STROBE
E2 USB_HSIC1_DATA
D2 USB_HSIC1_STROBE

A7 USB_HSIC_RCOMP

BF18 LPC_RCOMP
BH16 ILB_LPC_AD_00
BJ17 ILB_LPC_AD_11
BJ13 ILB_LPC_AD_22
BG14 ILB_LPC_AD_33
BG17 ILB_LPC_FRAME
BG16 ILB_LPC_CLK_00
BH14 ILB_LPC_CLK_11
BG16 ILB_LPC_CLKRUN
BG13 ILB_LPC_SERIRQ

BG12 PCU_SMB_DATA
BH10 PCU_SMB_CLK
BG11 PCU_SMB_ALERT

VLV_M_D/BGA

REV = 1.15

6 OF 13

RESERVED_M10
RESERVED_M9
RESERVED_P7
RESERVED_P6

RESERVED_M7
USB3_REXT0
RESERVED_P10
RESERVED_P12

RESERVED_M4
RESERVED_M6

USB3_RXP0
USB3_RXN0
USB3_TXP0
USB3_TXN0

RESERVED_H8
RESERVED_H7

RESERVED_H5
RESERVED_H4

GPIO_S0_SC_55
GPIO_S0_SC_56
GPIO_S0_SC_57
GPIO_S0_SC_58
GPIO_S0_SC_59
GPIO_S0_SC_60
GPIO_S0_SC_61

ILB_B254_SPKR

SIO_I2C0_DATA
SIO_I2C0_CLK

SIO_I2C1_DATA
SIO_I2C1_CLK

SIO_I2C2_DATA
SIO_I2C2_CLK

SIO_I2C3_DATA
SIO_I2C3_CLK

SIO_I2C4_DATA
SIO_I2C4_CLK

SIO_I2C5_DATA
SIO_I2C5_CLK

SIO_I2C6_DATA
SIO_I2C6_CLK

GPIO_S0_SC_092
GPIO_S0_SC_093

M10
P7
P6

M7
M12
P10
P12

M4
M6

D4
E3
K6
K7

H8
H7

H5
H4

BD12
BC12
BG14
BF14
BD16
BC16

BH12

BH22
BG23

BG24
BH24

BG25
BJ25

BG26
BH26

BF27
BG27

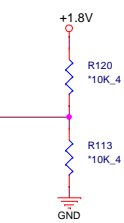
BH28
BG28

BJ29
BG29

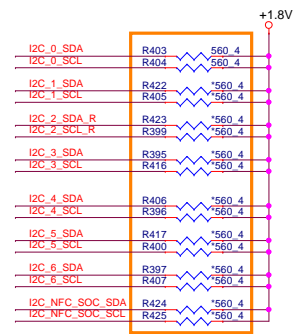
BH30
BG30

T10
T9

Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted

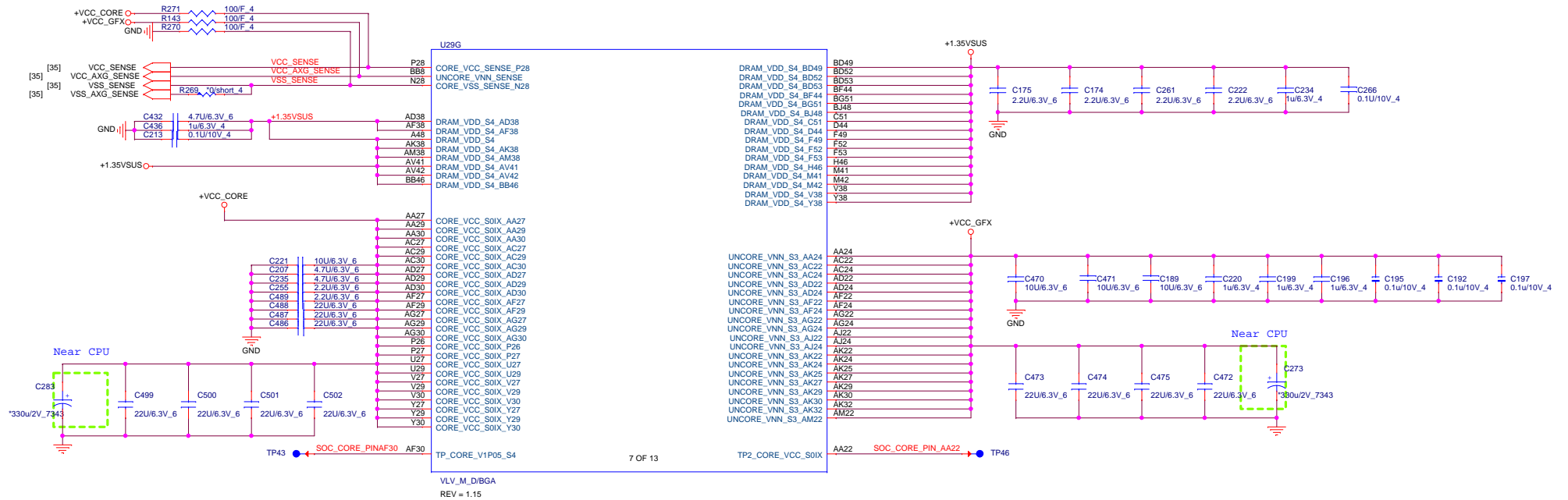


Touch pad

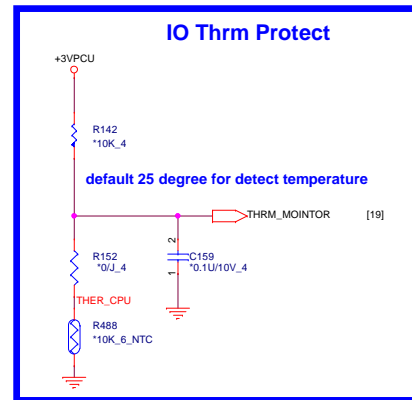


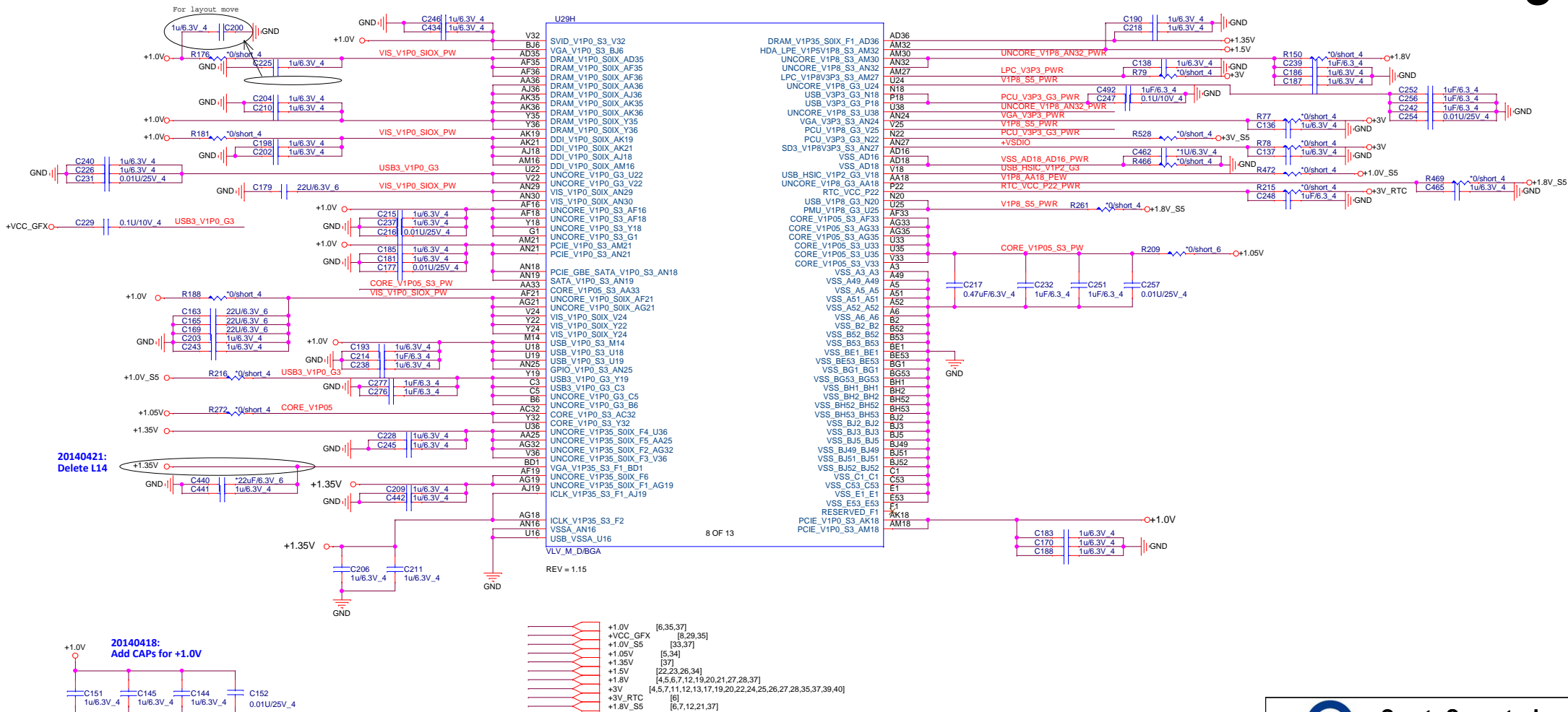
I2C pull up:
Standard/ Fast Mode ---> 560 ohm
High speed mode ---> CLK- 560 ohm;
DATA- 910 ohm

Quanta Computer Inc.
PROJECT : ZYL/ZYLA
Valley 6/9 (USB/LPC/I2C)
Size: Document Number: Rev: 1A
Date: Thursday, July 10, 2014 Sheet: 7 of 44



+VCC_CORE [29,35]
 +VCC_GFX [9,29,35]
 +1.35VSUS [2,11,36,37]
 +3VPCU [6,19,21,22,25,26,30,31,32,37,39,40]



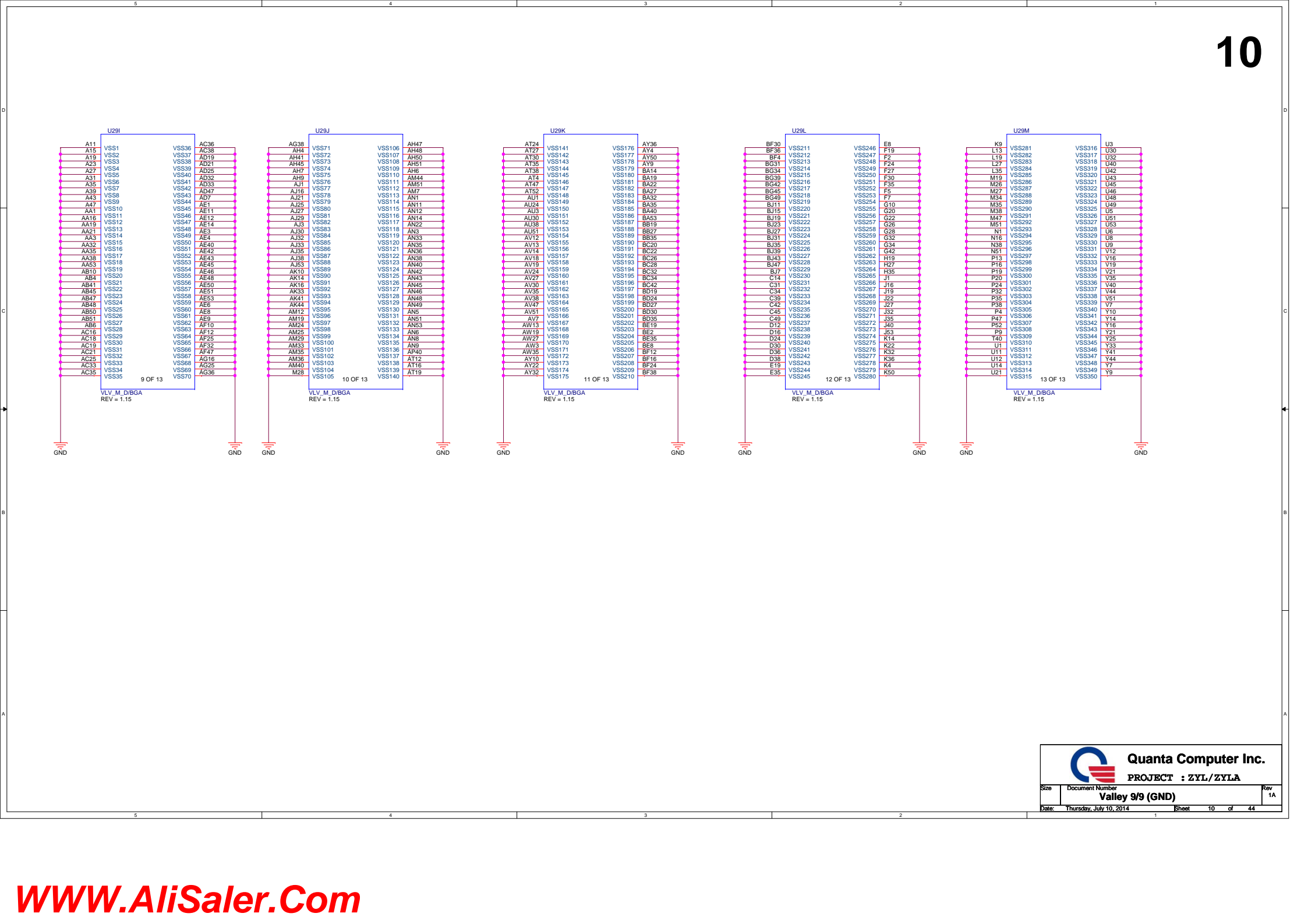


Quanta Computer Inc.

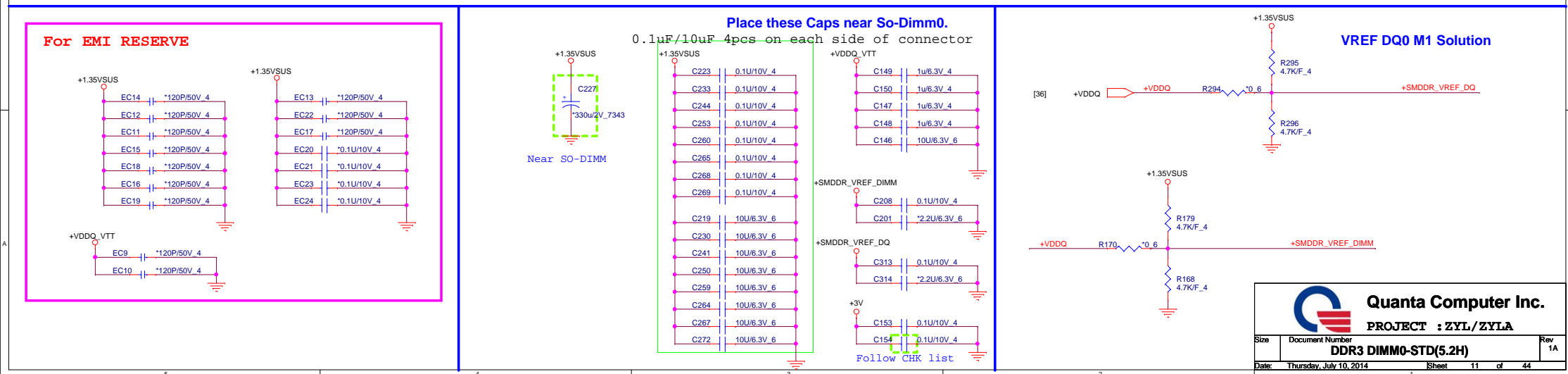
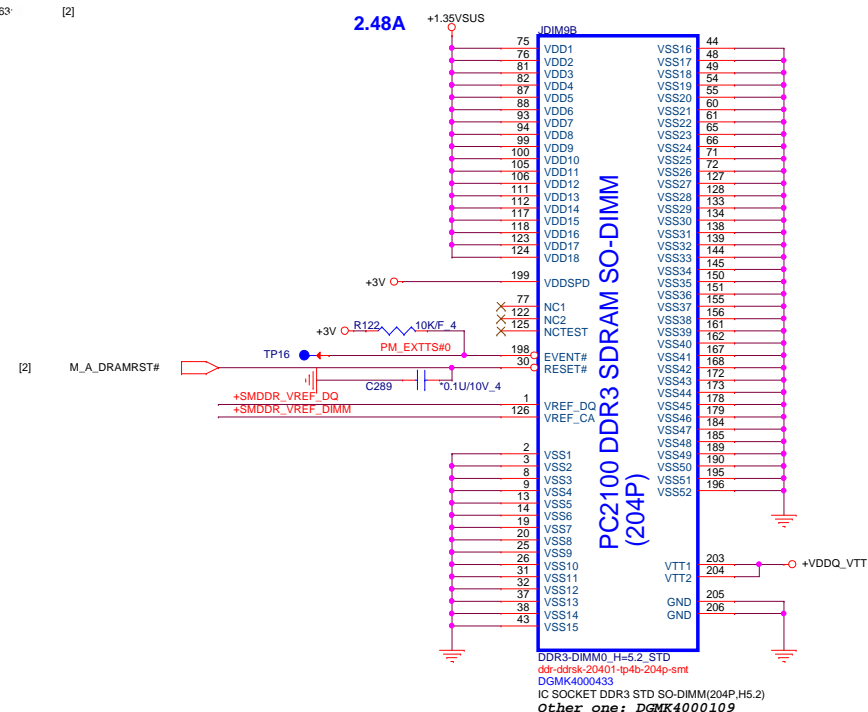
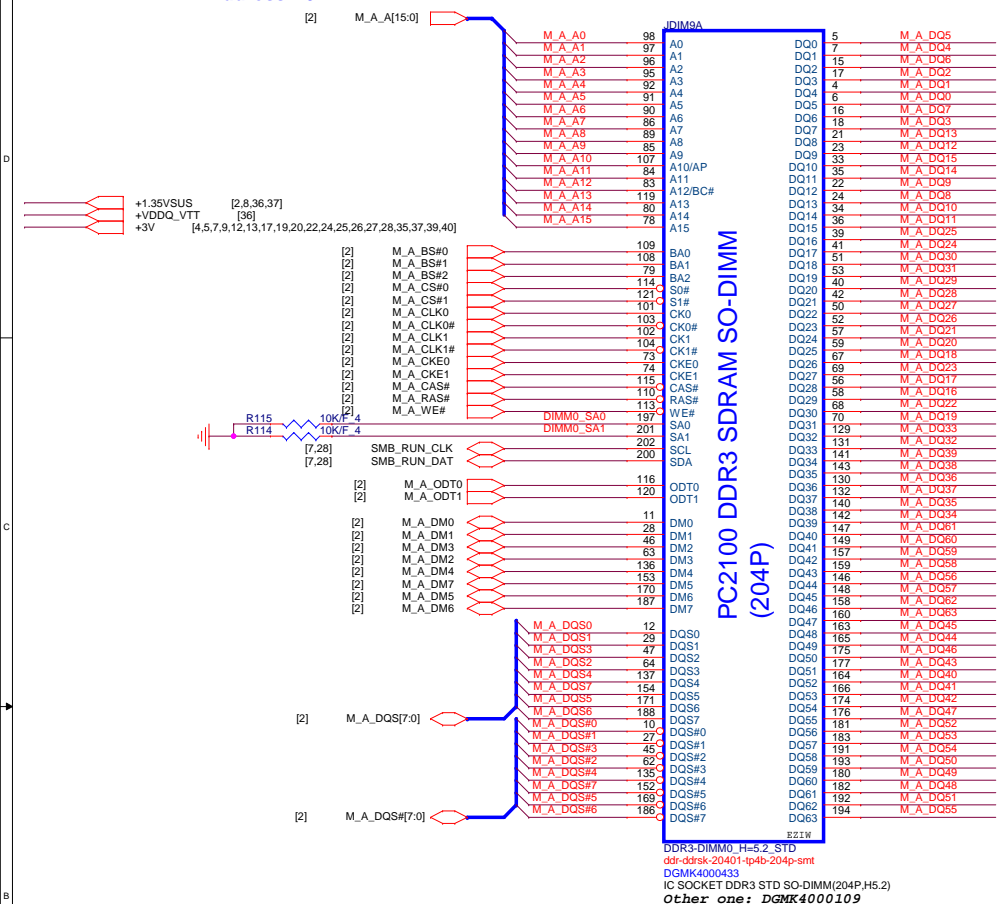
PROJECT : ZYL/ZYLA

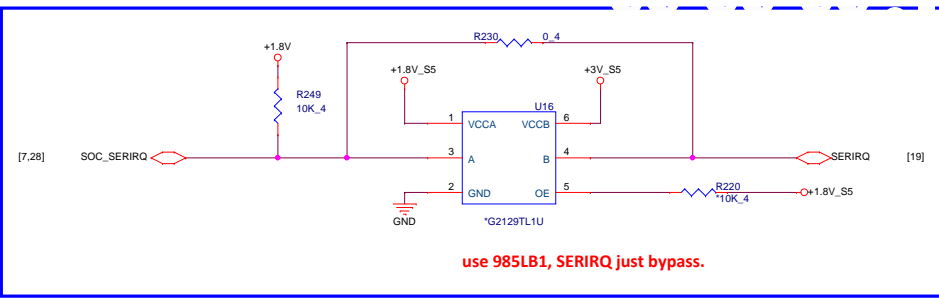
Size	Document Number	Rev
	Valley 8/9 (Power 2)	1A

Date: Thursday, July 10, 2014 Sheet 9 of 44

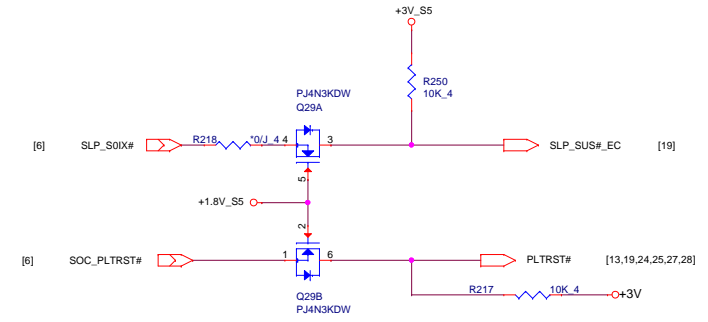
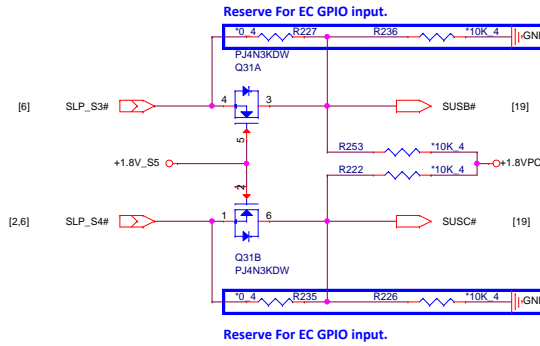
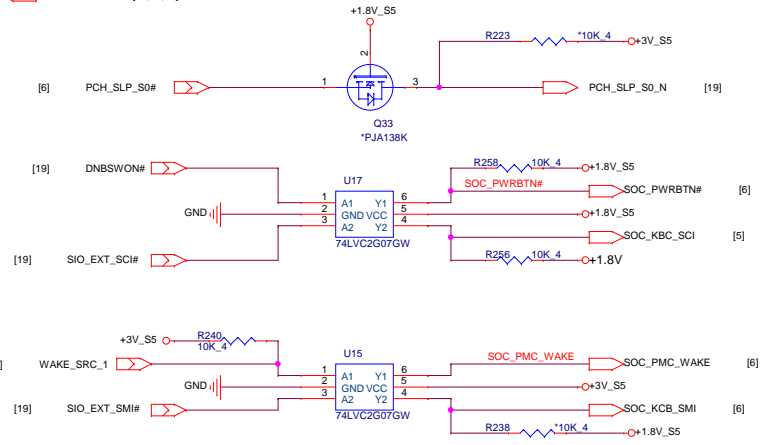
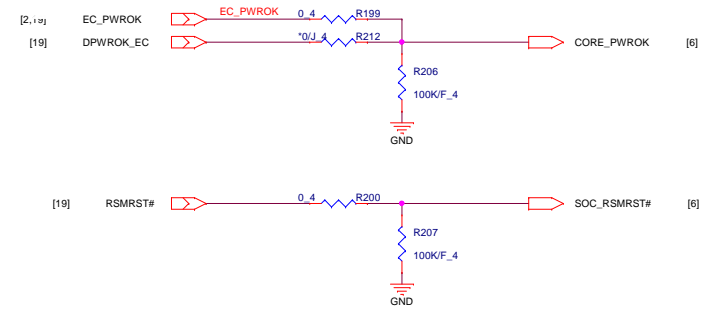


Address A0H

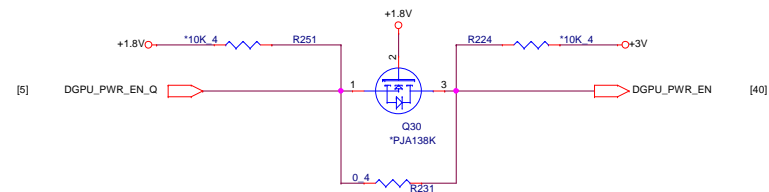
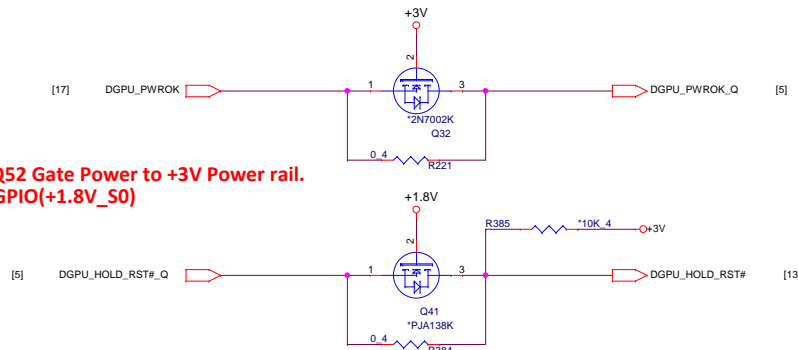


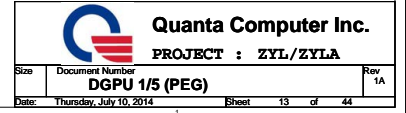


+1.8V [4,5,6,7,9,19,20,21,27,28,37]
 +3V_S5 [2,9,19,21,24,27,28,34,35,37,39,40]
 +3V [4,5,7,9,11,13,17,19,20,22,24,25,26,27,28,35,37,39,40]
 +1.8V_S5 [6,7,9,21,37]
 +1.8VPCU [19,32,37]



Check Q51 / Q52 Gate Power to +3V Power rail.
 Check which GPIO(+1.8V_S0)





<VGA>

EV@10K 4 R359 FB_CLAMP F3

N15V-GM no support GC6 function.

+1.05V_GFX [13,15,40]
+1.5V_GFX [13,18,40]

[18] FBA_CMD[30:0]

+1.5V_GFX EV@60.4/F 4 R39 FBA_DEBUG0 F22 FBA_DEBUG0
EV@60.4/F 4 R42 FBA_DEBUG1 J22 FBA_DEBUG1

[18] VMA_CLK0 D24 FBA_CLK0
[18] VMA_CLK0 D25 FBA_CLK0
[18] VMA_CLK1 M22 FBA_CLK1

+1.05V_GFX EV@HCB1608KF1A/30ohm_6 L11 C63
EV@0.1u/10V 4 C62 EV@0.1u/10V 4 C70 +FB_PLLAVDD F16 FB_PLLAVDD
EV@0.1u/10V 4 C41 +FB_PLLAVDD H22 FB_DLLAVDD GF119
C87 close ball H22 35mA

U25B

NC	GF119
FB_CLAMP	GF117

2/14 FBA

FBA_D0	E18 VMA_DQ0
FBA_D1	F18 VMA_DQ1
FBA_D2	E16 VMA_DQ2
FBA_D3	F17 VMA_DQ3
FBA_D4	D20 VMA_DQ4
FBA_D5	D21 VMA_DQ5
FBA_D6	F20 VMA_DQ6
FBA_D7	E21 VMA_DQ7
FBA_D8	E15 VMA_DQ8
FBA_D9	D15 VMA_DQ9
FBA_D10	F15 VMA_DQ10
FBA_D11	F13 VMA_DQ11
FBA_D12	C13 VMA_DQ12
FBA_D13	B13 VMA_DQ13
FBA_D14	E13 VMA_DQ14
FBA_D15	D13 VMA_DQ15
FBA_D16	B15 VMA_DQ16
FBA_D17	C16 VMA_DQ17
FBA_D18	A13 VMA_DQ18
FBA_D19	A15 VMA_DQ19
FBA_D20	B18 VMA_DQ20
FBA_D21	A18 VMA_DQ21
FBA_D22	A19 VMA_DQ22
FBA_D23	C19 VMA_DQ23
FBA_D24	B24 VMA_DQ24
FBA_D25	C23 VMA_DQ25
FBA_D26	A25 VMA_DQ26
FBA_D27	A24 VMA_DQ27
FBA_D28	A21 VMA_DQ28
FBA_D29	B21 VMA_DQ29
FBA_D30	C20 VMA_DQ30
FBA_D31	C21 VMA_DQ31
FBA_D32	R22 VMA_DQ32
FBA_D33	R24 VMA_DQ33
FBA_D34	T22 VMA_DQ34
FBA_D35	R23 VMA_DQ35
FBA_D36	N25 VMA_DQ36
FBA_D37	N26 VMA_DQ37
FBA_D38	N23 VMA_DQ38
FBA_D39	N24 VMA_DQ39
FBA_D40	V23 VMA_DQ40
FBA_D41	V22 VMA_DQ41
FBA_D42	T23 VMA_DQ42
FBA_D43	U22 VMA_DQ43
FBA_D44	Y24 VMA_DQ44
FBA_D45	A24 VMA_DQ45
FBA_D46	Y22 VMA_DQ46
FBA_D47	A23 VMA_DQ47
FBA_D48	AD27 VMA_DQ48
FBA_D49	AB25 VMA_DQ49
FBA_D50	AD26 VMA_DQ50
FBA_D51	AC25 VMA_DQ51
FBA_D52	AA27 VMA_DQ52
FBA_D53	AA26 VMA_DQ53
FBA_D54	W26 VMA_DQ54
FBA_D55	Y25 VMA_DQ55
FBA_D56	R26 VMA_DQ56
FBA_D57	T25 VMA_DQ57
FBA_D58	N27 VMA_DQ58
FBA_D59	R27 VMA_DQ59
FBA_D60	V26 VMA_DQ60
FBA_D61	V27 VMA_DQ61
FBA_D62	W27 VMA_DQ62
FBA_D63	W25 VMA_DQ63

FBA_DQM0	D19 VMA_DM0
FBA_DQM1	D14 VMA_DM1
FBA_DQM2	C17 VMA_DM2
FBA_DQM3	C22 VMA_DM3
FBA_DQM4	P24 VMA_DM4
FBA_DQM5	W24 VMA_DM5
FBA_DQM6	A25 VMA_DM6
FBA_DQM7	U25 VMA_DM7

FBA_DQS_WP0	E19 VMA_WDQS0
FBA_DQS_WP1	C15 VMA_WDQS1
FBA_DQS_WP2	B16 VMA_WDQS2
FBA_DQS_WP3	B22 VMA_WDQS3
FBA_DQS_WP4	R25 VMA_WDQS4
FBA_DQS_WP5	W23 VMA_WDQS5
FBA_DQS_WP6	AB26 VMA_WDQS6
FBA_DQS_WP7	T26 VMA_WDQS7

FBA_DQS_RN0	F19 VMA_RDQS0
FBA_DQS_RN1	C14 VMA_RDQS1
FBA_DQS_RN2	A16 VMA_RDQS2
FBA_DQS_RN3	A22 VMA_RDQS3
FBA_DQS_RN4	P25 VMA_RDQS4
FBA_DQS_RN5	W22 VMA_RDQS5
FBA_DQS_RN6	AB27 VMA_RDQS6
FBA_DQS_RN7	T27 VMA_RDQS7

For Fermi

FBA_CMD2	R36	EV@10K/F 4
FBA_CMD3	R32	EV@10K/F 4
FBA_CMD5	R41	EV@10K/F 4
FBA_CMD18	R368	EV@10K/F 4
FBA_CMD19	R53	EV@10K/F 4

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18]

VMA_DQ[63:0] VMA_DQ[63:0]

For Fermi

FBA_CMD2	R36	EV@10K/F 4
FBA_CMD3	R32	EV@10K/F 4
FBA_CMD5	R41	EV@10K/F 4
FBA_CMD18	R368	EV@10K/F 4
FBA_CMD19	R53	EV@10K/F 4

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

[18] +1.5V_GFX EV@40.2/F 4 R35 FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ
EV@42.2/F 4 R29 FB_CAL_PU_GND C24 FB_CAL_PU_GND
EV@51.1/F 4 R27 FB_CAL_TERM_GND B25 FB_CAL_TERM_GND

U25D

12/14 FBVDDQ

FBVDDQ	B26	+1.5V_GFX
FBVDDQ	C25	
FBVDDQ	E23	
FBVDDQ	E26	
FBVDDQ	F14	
FBVDDQ	P21	
FBVDDQ	G13	
FBVDDQ	G14	
FBVDDQ	P23	
FBVDDQ	G16	
FBVDDQ	G18	
FBVDDQ	G19	
FBVDDQ	G20	
FBVDDQ	G21	
FBVDDQ	H24	
FBVDDQ	H26	
FBVDDQ	J21	
FBVDDQ	K21	
FBVDDQ	L22	
FBVDDQ	L24	
FBVDDQ	U10	
FBVDDQ	M21	
FBVDDQ	N21	
FBVDDQ	R21	
FBVDDQ	T21	
FBVDDQ	V21	
FBVDDQ	W21	

+1.5V_GFX

PLACE CLOSE TO GPU BALLS

C38	EV@0.1u/10V 4
C35	EV@0.1u/10V 4
C57	EV@0.1u/10V 4
C36	EV@0.1u/10V 4
C30	EV@1u/6.3V 4
C27	EV@1u/6.3V 4
C28	EV@1u/6.3V 4
C77	EV@1u/6.3V 4

PLACE CLOSE TO GPU BALLS

C38	EV@0.1u/10V 4
C35	EV@0.1u/10V 4
C57	EV@0.1u/10V 4
C36	EV@0.1u/10V 4
C30	EV@1u/6.3V 4
C27	EV@1u/6.3V 4
C28	EV@1u/6.3V 4
C77	EV@1u/6.3V 4

PLACE CLOSE TO GPU BALLS

C38	EV@0.1u/10V 4
C35	EV@0.1u/10V 4
C57	EV@0.1u/10V 4
C36	EV@0.1u/10V 4
C30	EV@1u/6.3V 4
C27	EV@1u/6.3V 4
C28	EV@1u/6.3V 4
C77	EV@1u/6.3V 4

PLACE CLOSE TO GPU BALLS

C38	EV@0.1u/10V 4
C35	EV@0.1u/10V 4
C57	EV@0.1u/10V 4
C36	EV@0.1u/10V 4
C30	EV@1u/6.3V 4
C27	EV@1u/6.3V 4
C28	EV@1u/6.3V 4
C77	EV@1u/6.3V 4

PLACE CLOSE TO GPU BALLS

C38	EV@0.1u/10V 4
C35	EV@0.1u/10V 4
C57	EV@0.1u/10V 4
C36	EV@0.1u/10V 4
C30	EV@1u/6.3V 4
C27	EV@1u/6.3V 4
C28	EV@1u/6.3V 4
C77	EV@1u/6.3V 4

PLACE CLOSE TO GPU BALLS

C38	EV@0.1u/10V 4
C35	EV@0.1u/10V 4
C57	EV@0.1u/10V 4
C36	EV@0.1u/10V 4
C30	EV@1u/6.3V 4
C27	EV@1u/6.3V 4
C28	EV@1u/6.3V 4
C77	EV@1u/6.3V 4

PLACE CLOSE TO GPU BALLS

C38	EV@0.1u/10V 4
C35	EV@0.1u/10V 4
C57	EV@0.1u/10V 4
C36	EV@0.1u/10V 4
C30	EV@1u/6.3V 4
C27	EV@1u/6.3V 4
C28	EV@1u/6.3V 4
C77	EV@1u/6.3V 4

PLACE CLOSE TO GPU BALLS

U25F

12/14 GND

M13	GND	AB17
M15	GND	AB20
M17	GND	AB20
N10	GND	AB24
N12	GND	AC2
N14	GND	AC22
N16	GND	AC26
N18	GND	AC5
P11	GND	AC8
P13	GND	AD12
P15	GND	AD13
P17	GND	AD6
P2	GND	AD15
P23	GND	AD16
P26	GND	AD18
P5	GND	AD19
R10	GND	AD21
R12	GND	AD22
R14	GND	AE11
R16	GND	AE14
R18	GND	AE17
T11	GND	AE20
T13	GND	AE11
T15	GND	AF1
T17	GND	AF11
U10	GND	AF14
U12	GND	AF17
U14	GND	AF20
U16	GND	AF23
U18	GND	AF5
U2	GND	AF8
U23	GND	AG2
U26	GND	AG26
U5	GND	AB14
V11	GND	B1
V13	GND	B11
V15	GND	B14
V17	GND	B17
V2	GND	B20
Y23	GND	B23
Y26	GND	B27
Y5	GND	B5
	GND	B8
	GND	E11
	GND	E14
	GND	E17
	GND	E2
	GND	E20
	GND	E22
	GND	E5
	GND	E8
	GND	H2
	GND	H23
	GND	H25
	GND	H5
	GND	K11
	GND	K13
	GND	K15
	GND	K17
	GND	L10
	GND	L12
	GND	L14
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	GND	L2
	GND	L23
	GND	L25
	GND	L5
	GND	M11

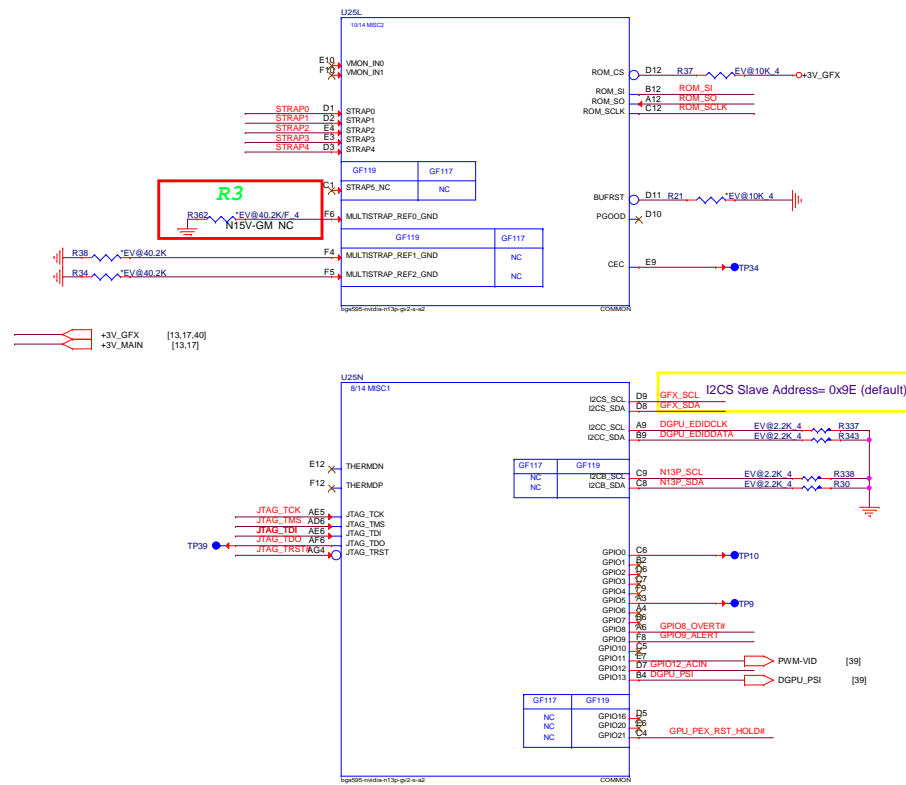
COMMON

bga595-nvda-n13p-g2-s-a2

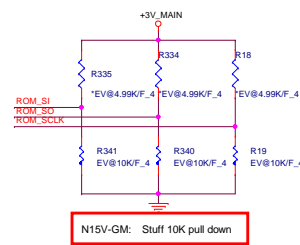


Quanta Computer Inc.
PROJECT : ZYL/ZYLA

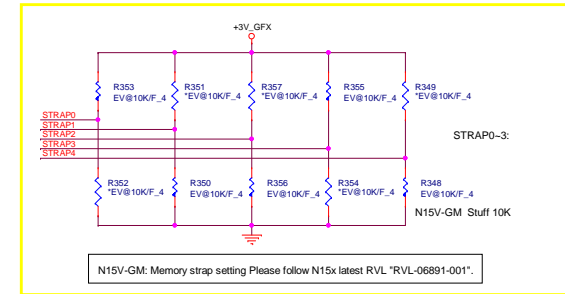
Size Document Number DGPU 2/5 (Memory) Rev 1A
Date: Thursday, July 10, 2014 Sheet 14 of 44



Binary mode setting
For N15V-GM-B-A2:
Device ID=0x1140
R3= N.C.
1.ROM_SCLK=10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory
binary mode setting.
5.Strap4=10k pull down



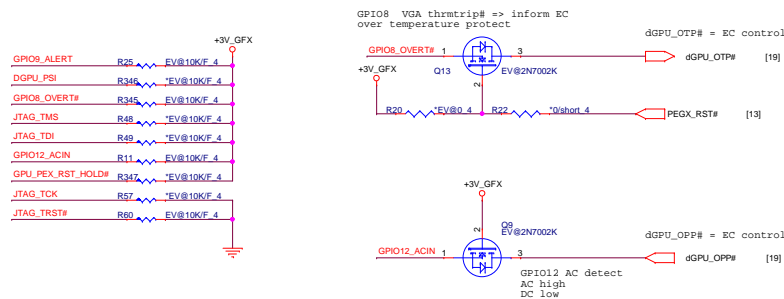
Vendor	Vendor P/N	Strap0	Strap1	Strap2	Strap3
HYNIX	HT5C4G63AFR-11C	0	0	1	0
MICRON	MT41J256M16HA-093G:E	1	0	1	1
SAMSUNG	K4W4G164D-BC1A	1	0	0	1



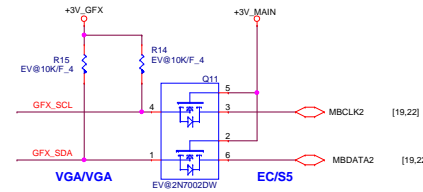
N15V-GM VRAM Configuration Table:

4Gb	Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N
	0100 (0x4)	DDR3 256MBx16, 1000MHz	HYNIX	H5TC4G63AFR-11C	
	1101 (0x5)	DDR3 256MBx16, 1000MHz	MICRON	MT41J256M16HA-093G:E	
	1001 (0x9)	DDR3 256MBx16, 1000MHz	SAMSUNG	K4W4G164D-BC1A	

STRAP3
Optimus ==> 4.99k PD
Resistor P/N
10K ==> CS31002FB26

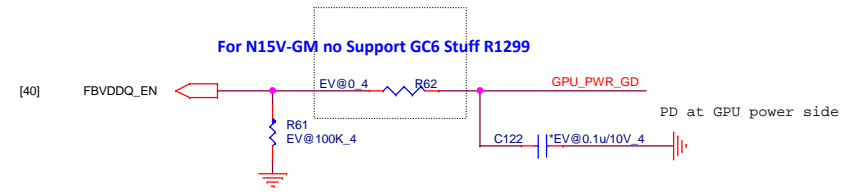
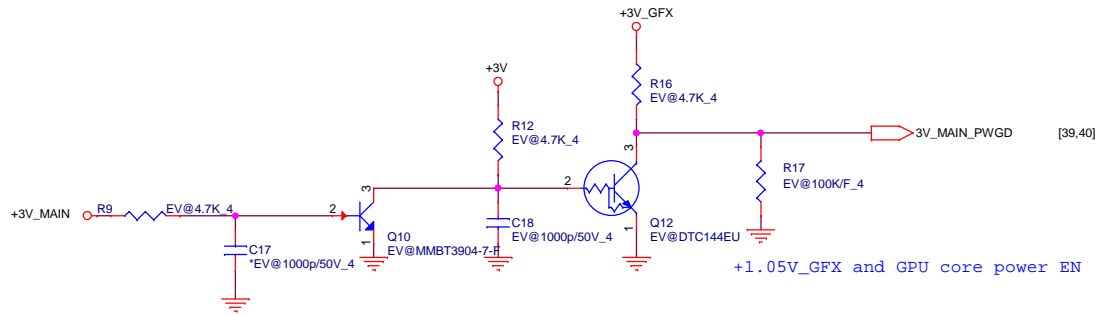
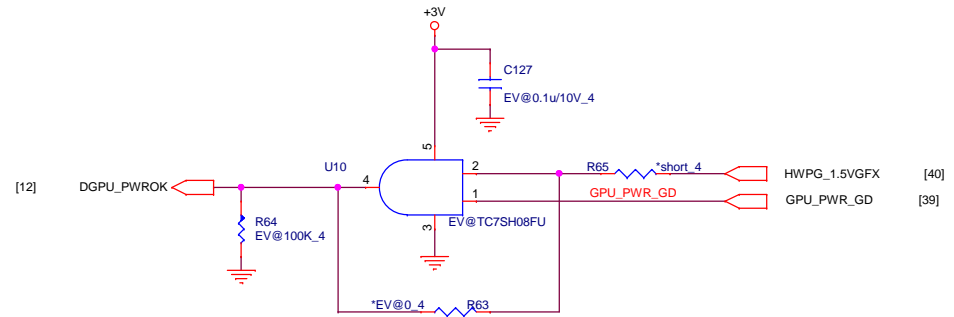
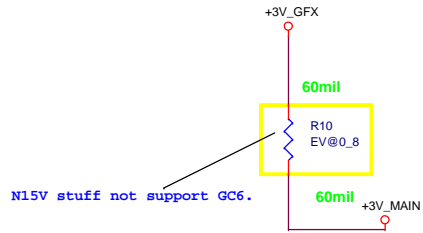


SMBus(VGA)

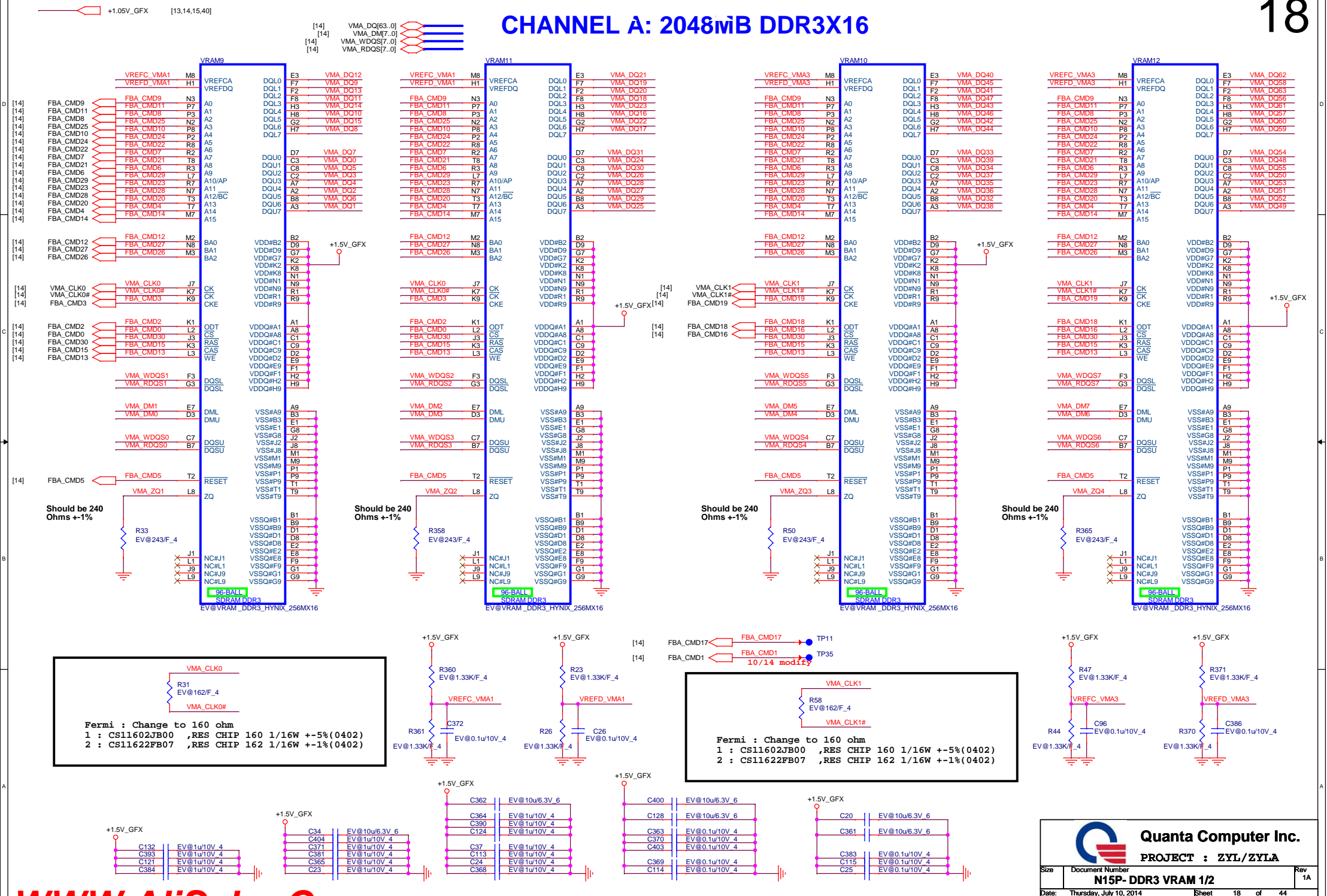


Vendor P/N	820M	QCI P/N
N15V-GM-B-A2	GeForce 820M	0x1140
		AJON15V0703

+3V_GFX [13,16,40]
 +3V_MAIN [13,16]
 +3V [4,5,7,9,11,12,13,19,20,22,24,25,26,27,28,35,37,39,40]

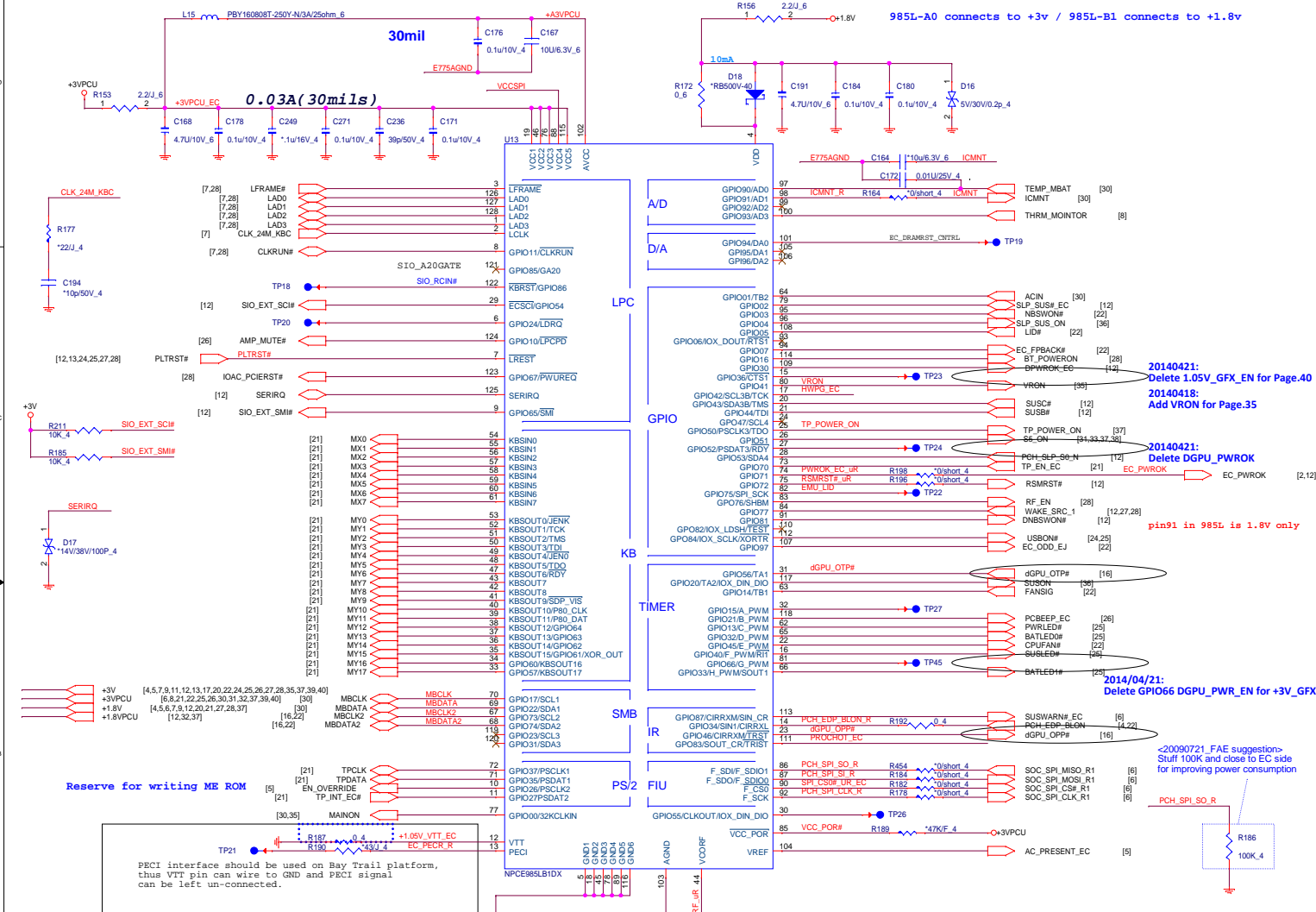


CHANNEL A: 2048MiB DDR3X16



EC 985LB1(KBC)
1.8V interface

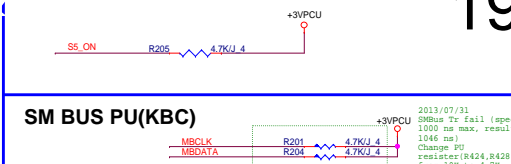
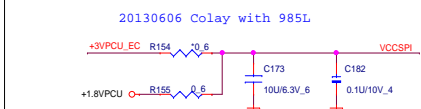
1.8V p/n: AJ9990F02
Discription: IC CONTROLLER(128P)NPCE985LB1DX(LQFP)



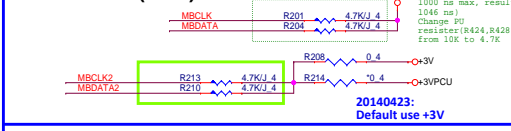
SM BUS ARRANGEMENT TABLE

SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

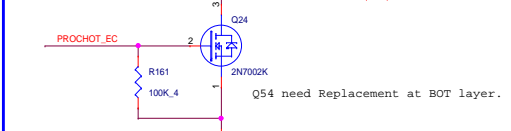
985LB1 Pin88



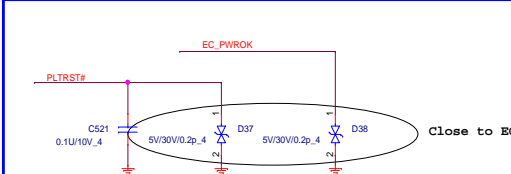
SM BUS PU(KBC)



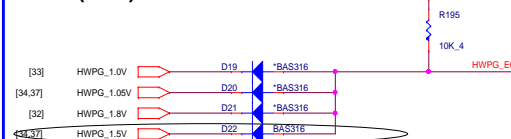
H_PROCHOT# [5.3]



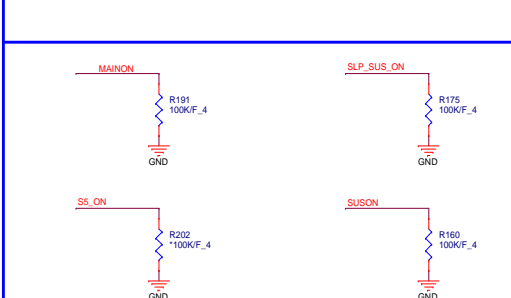
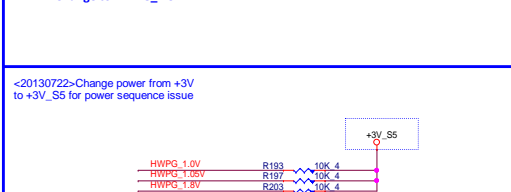
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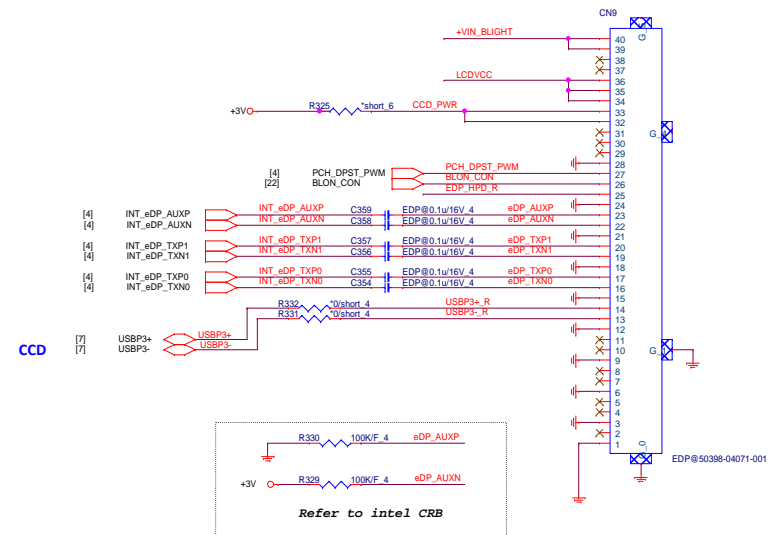


HWPG(KBC)

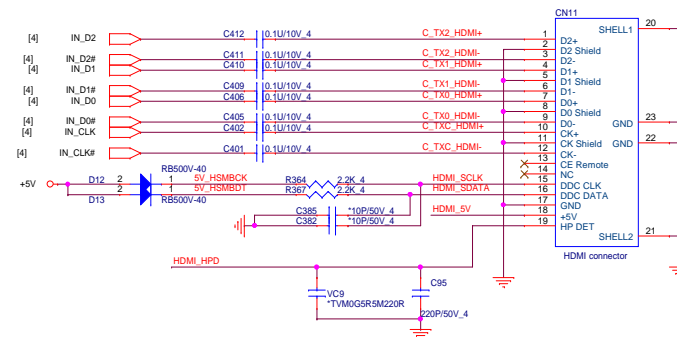
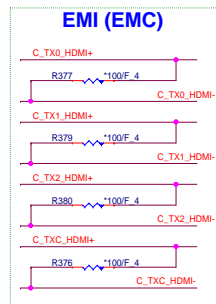


20140421:
Change to HWPG 1.5W

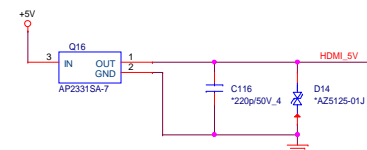
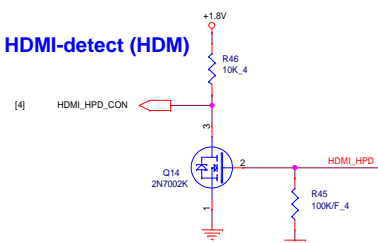


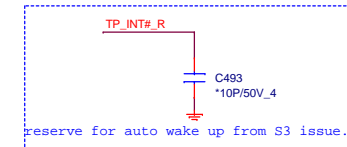
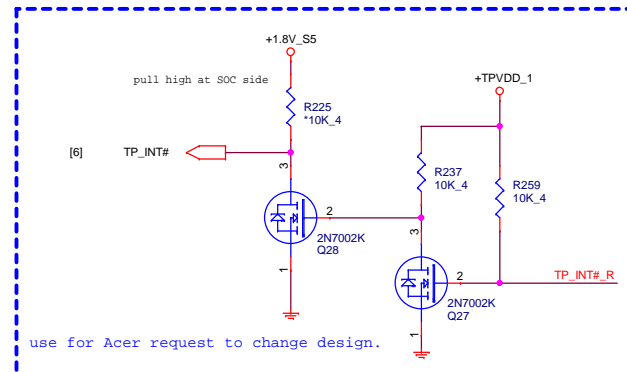
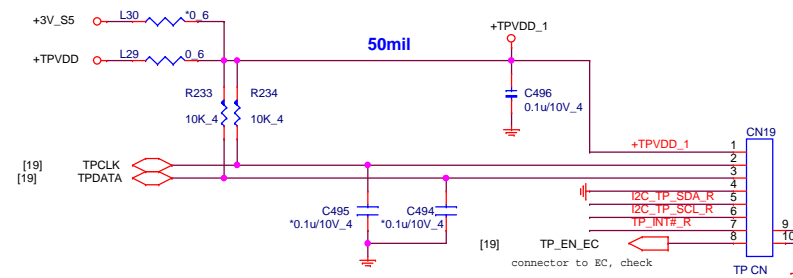


EMI (EMC)



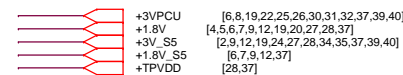
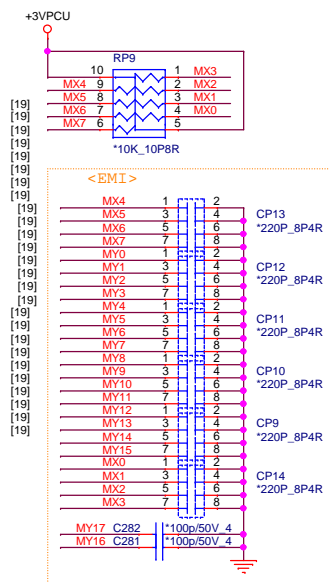
Close to HDMI connector





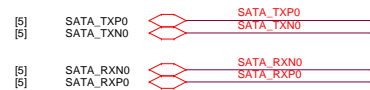
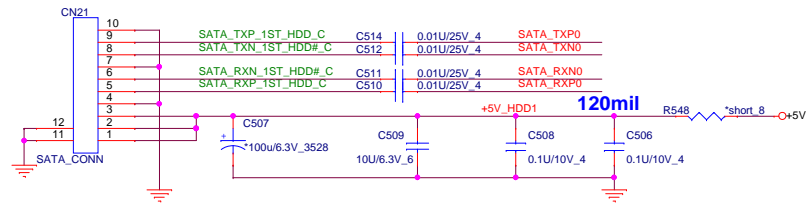
Pinout diagram for the CN20 connector:

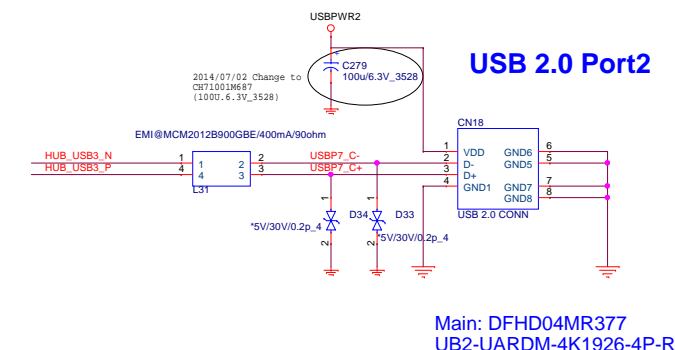
Pin	Signal
1	MX0
2	MX1
3	MX2
4	MX3
5	MX4
6	MX5
7	MX6
8	MX7
9	MY17
10	MY16
11	MY15
12	MY14
13	MY13
14	MY12
15	MY11
16	MY10
17	MY9
18	MY8
19	MY7
20	MY6
21	MY5
22	MY4
23	MY3
24	MY2
25	MY1
26	MY0
27	Ground
28	Ground



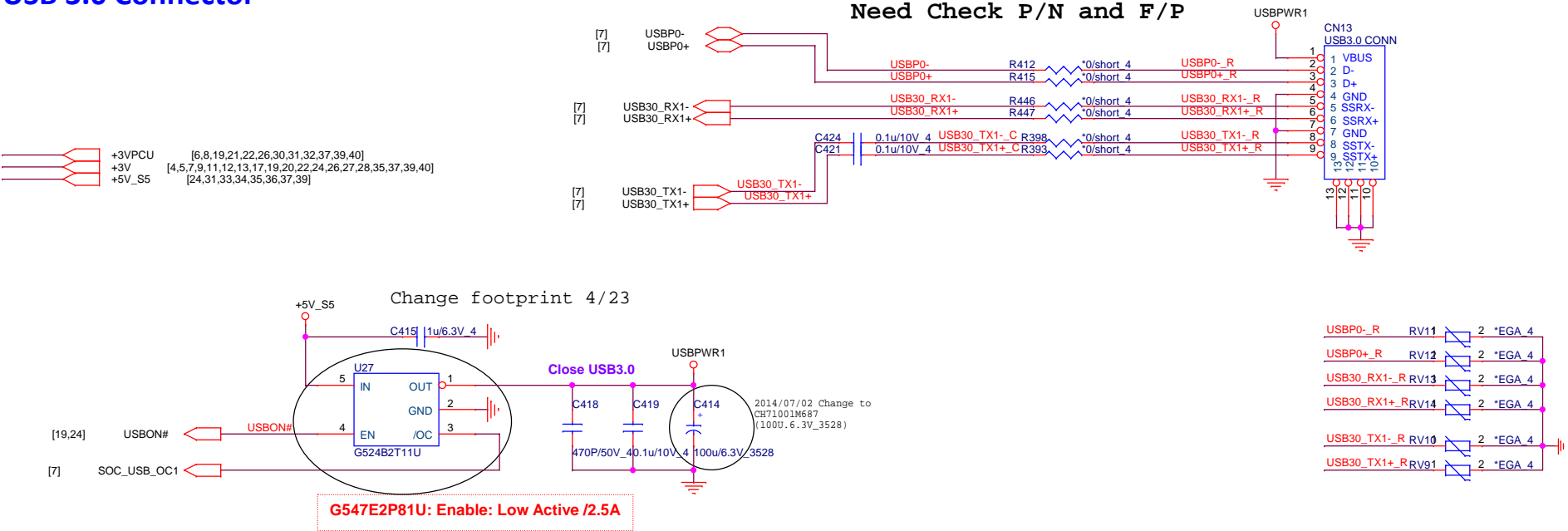
SATA HDD1

HDD1

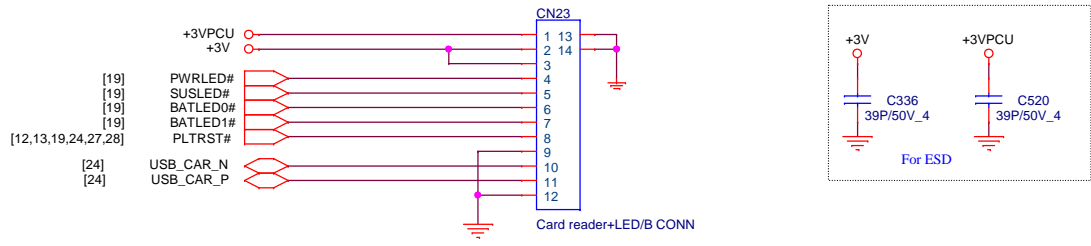




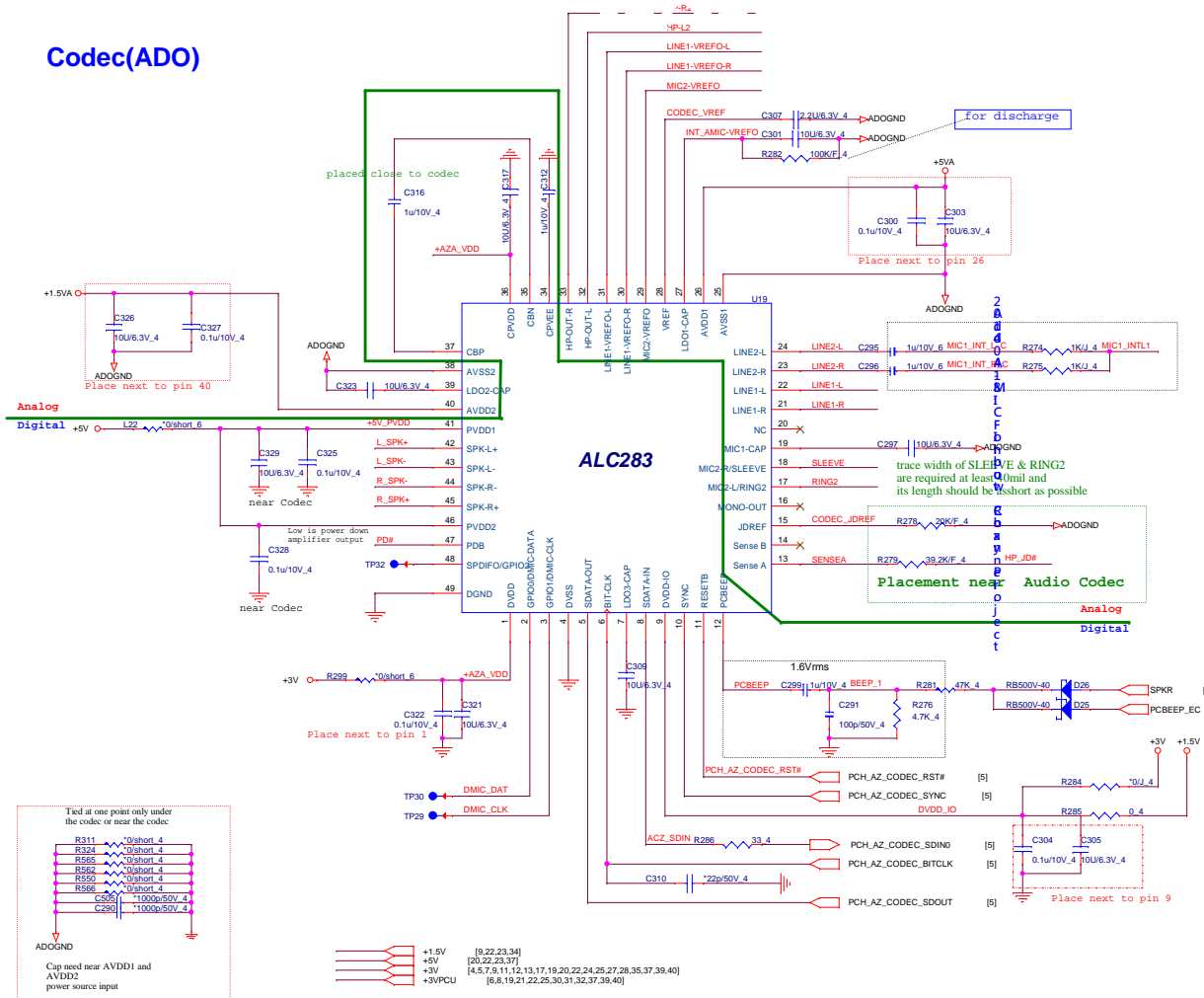
USB 3.0 Connector



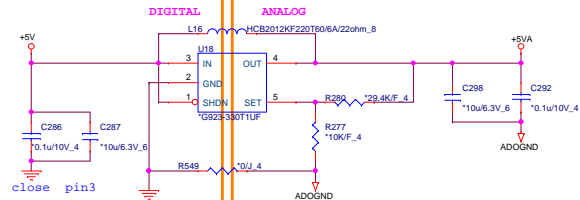
Card Reader+ LED/B Connector



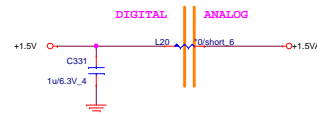
Codec(ADO)



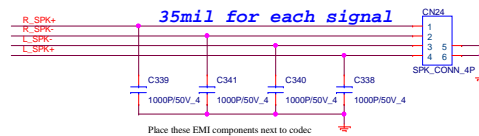
Codec PWR 5V(ADO)



Codec PWR 1.5V(ADO)

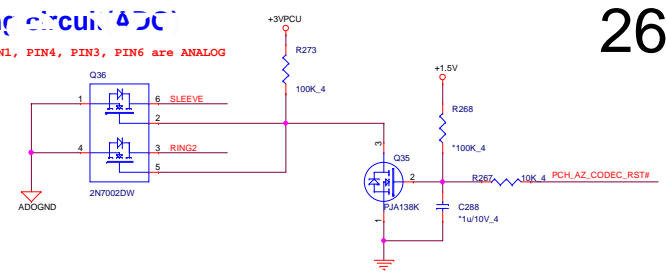


Internal Speaker

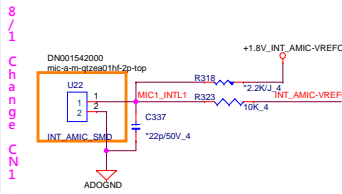


Group 4: circuit ABC

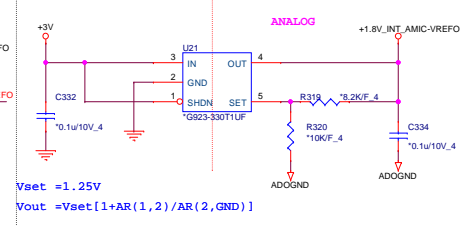
PIN1, PIN4, PIN3, PIN6 are ANALOG



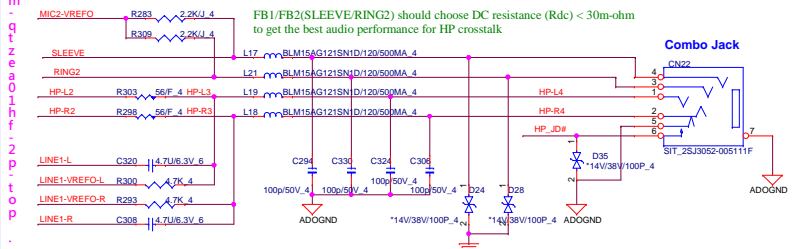
Analog-MIC



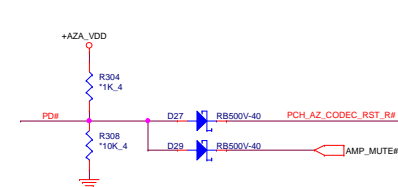
Power (ADO)



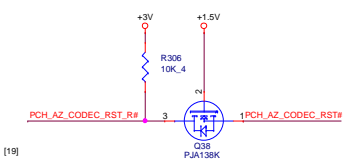
HEADPHONE/MIC/LINE combo (AMP)

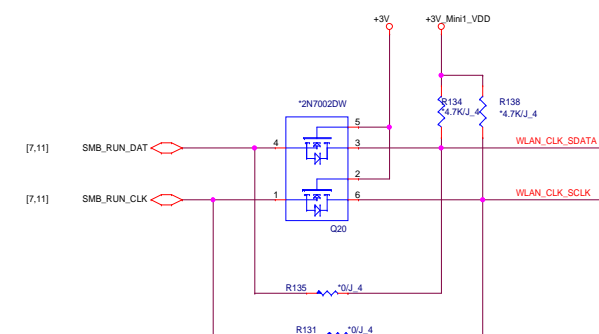
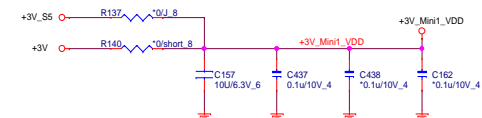


Mute(ADO)

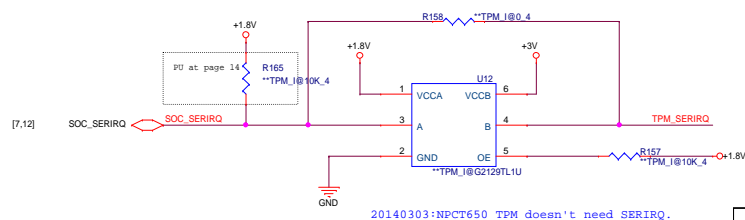



Level shift

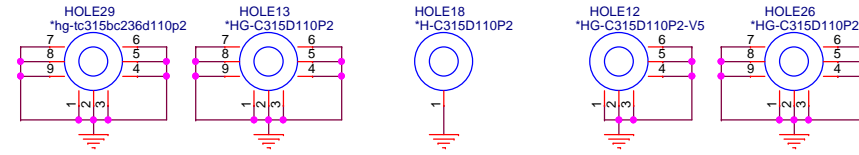
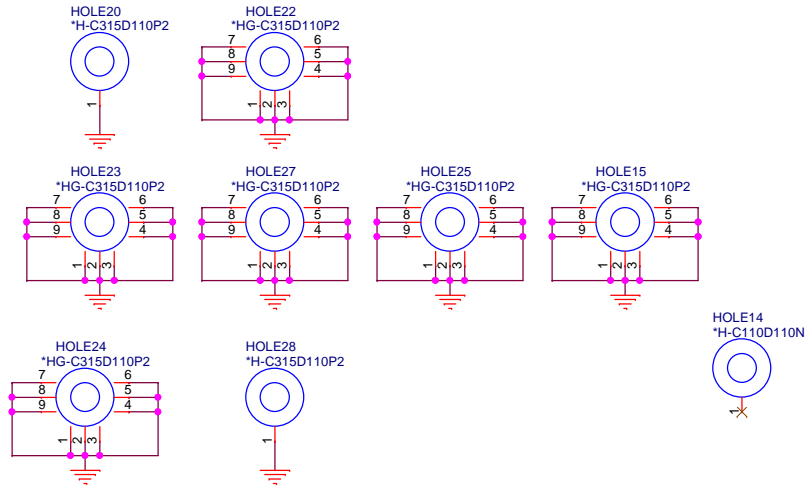




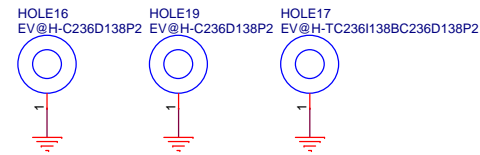
The schematic diagram illustrates the power supply for the TPM module. It features two main power rails: TPM_VDD and TPM_VSB. The TPM_VDD rail is connected to the +3V_VDD supply through a resistor R159 (100 Ohms) and a decoupling capacitor C166 (10uF/6.3V_6). It is also connected to the TPM module pins *TPM#2,2_6 and *TPM@0.1U/10V_4. The TPM_VSB rail is connected to the +TPVDD and +3V_SS supplies through resistors R05 and R06 (100 Ohms) and a decoupling capacitor C142 (10uF/6.3V_6). It is also connected to the TPM module pins *TPM_N@0_4 and *TPM_N@0.1U/10V_4. Additional decoupling capacitors C425, C420, C158, and C161 are shown on the TPM_VDD rail, and capacitor C140 is on the TPM_VSB rail.



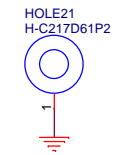
 Quanta Computer Inc. PROJECT : ZYL/ZYLA		
Size	Document Number	Rev
	WiFi & BT & TPM	1A
Date:	Thursday, July 10, 2014	Sheet 28 of 44



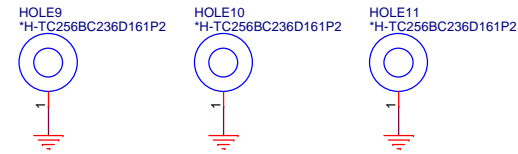
GPU nuts



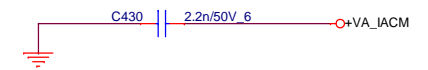
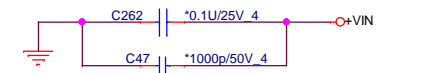
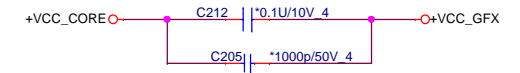
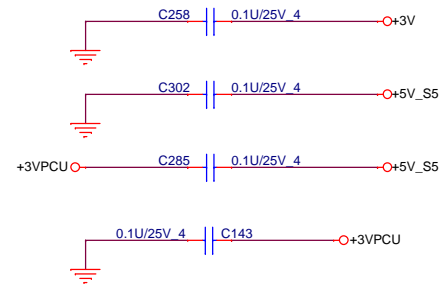
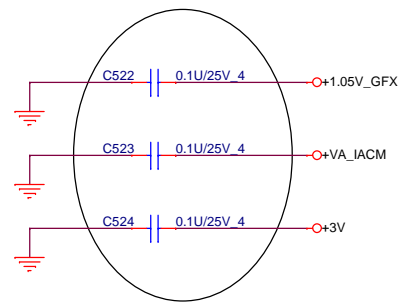
Mini card nuts



CPU nuts



reserve for ESD



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PROJECT : ZYL/ZYLA

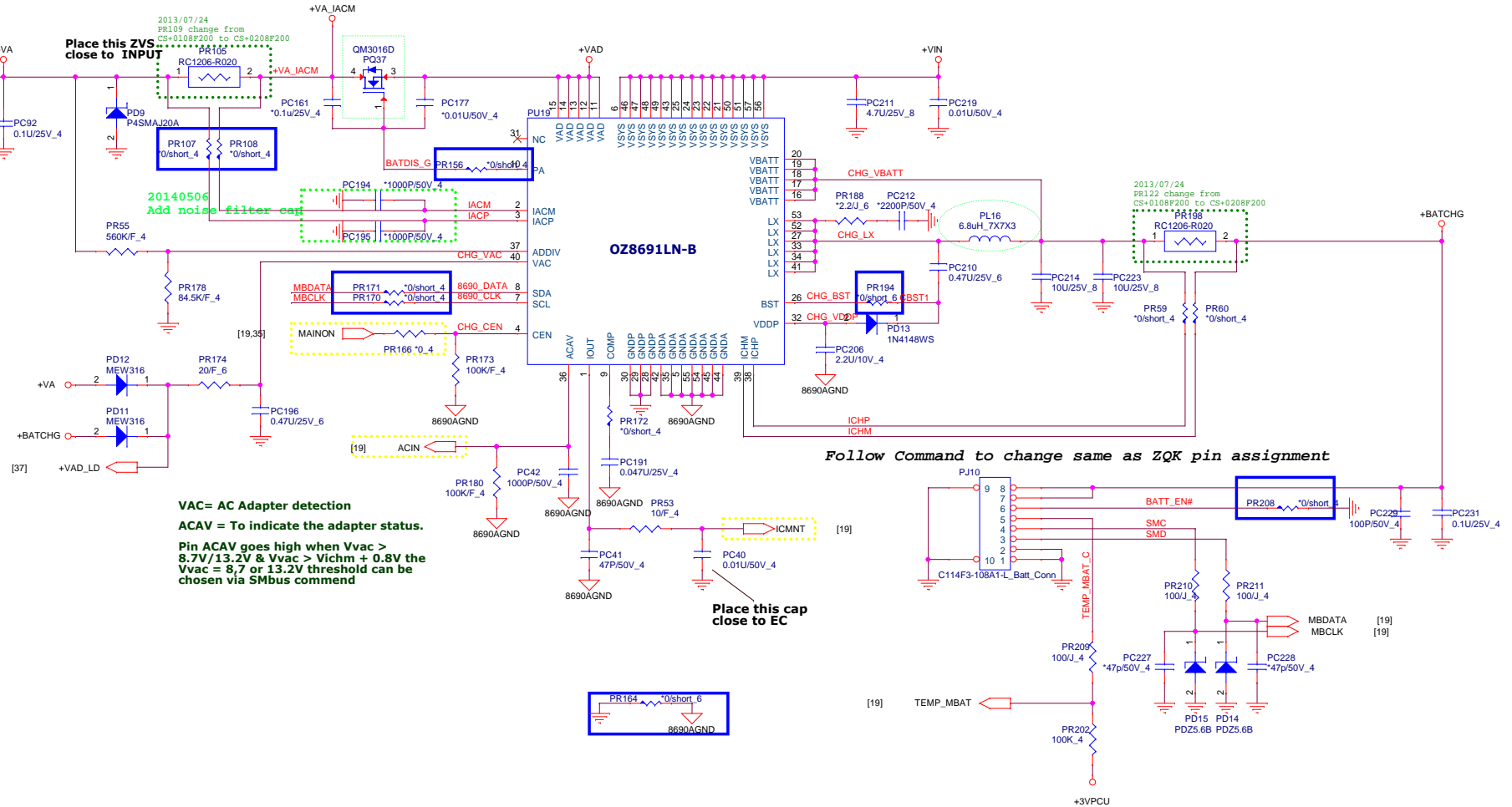
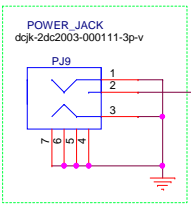
Size	Document Number	Rev
	USB BOARD CONN	1A

Date: Thursday, July 10, 2014

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DFPJ06MR013-- 95W
DFPJ06MR007--- 45W

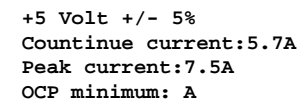
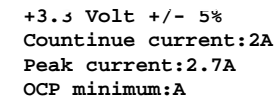
ZE7



Follow Command to change same as ZQK pin assignment

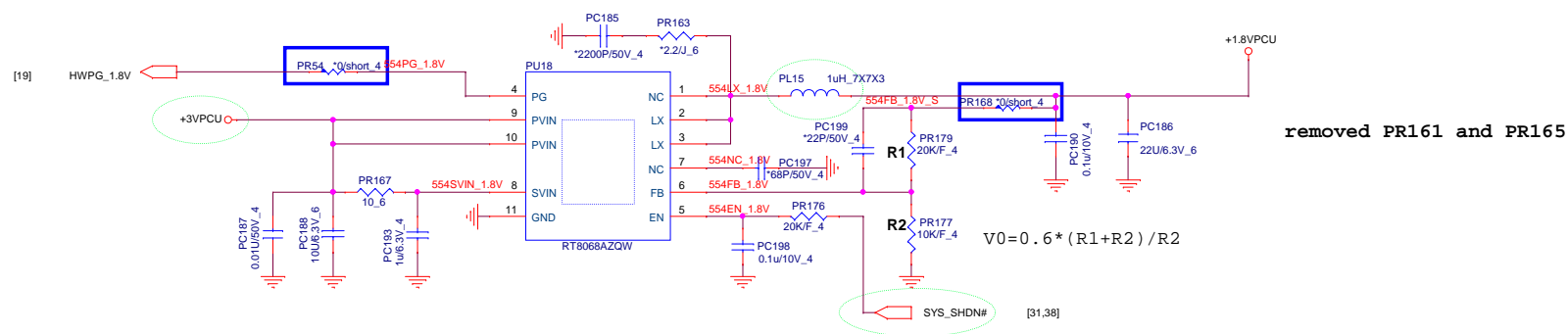
VAC= AC Adapter detection
ACAV = To indicate the adapter status.
Pin ACAV goes high when Vvac > 8.7V/13.2V & Vvac > Vichm + 0.8V the Vvac = 8.7 or 13.2V threshold can be chosen via SMBus command

Place this cap
close to EC



[12,19,37] +1.8VPCU
 [6,8,19,21,22,25,26,30,31,37,39,40] +3VPCU

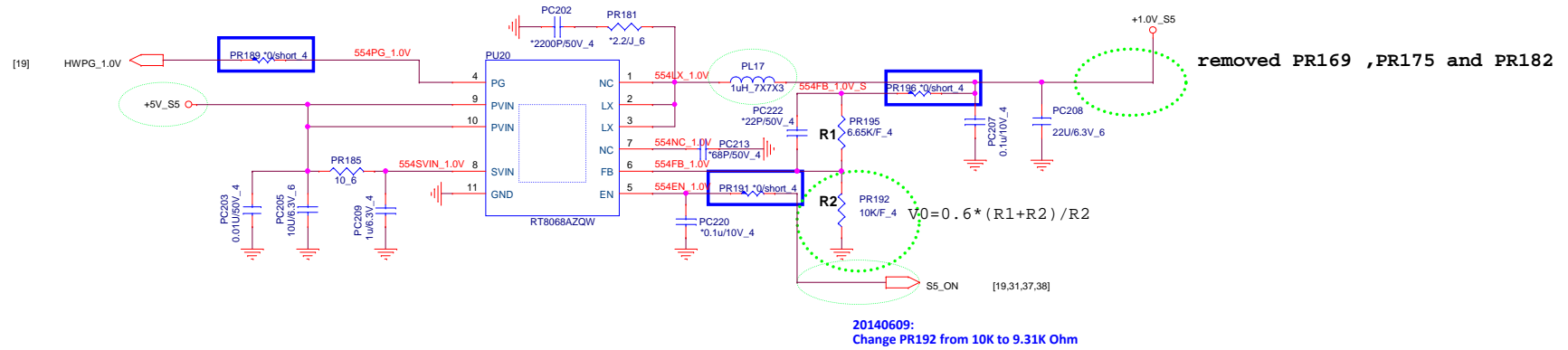
+1.8V Volt +/- 5%
 Countinue current:0.08A
 Peak current:0.11A
 OCP minimum:A



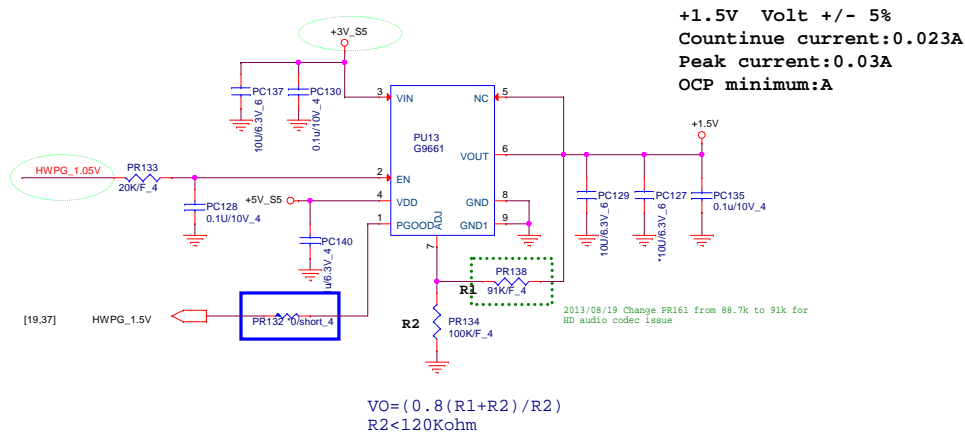
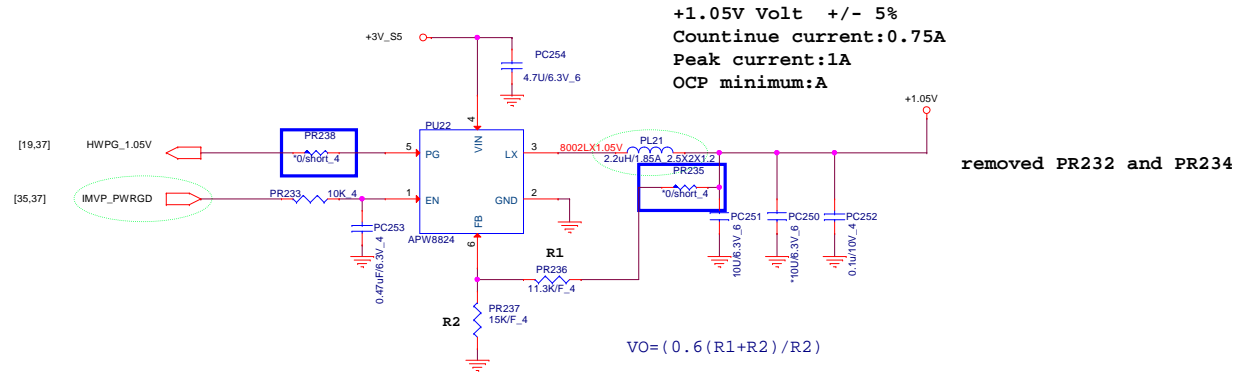
[9,37]
[24,25,31,34,35,36,37,39]
[2,9,12,19,21,24,27,28,34,35,37,39,40]

+1.0V_S5
+5V_S5
+3V_S5

+1.0V Volt +/- 5%
Countinue current:2.4A
Peak current:3.2A
OCP minimum:A



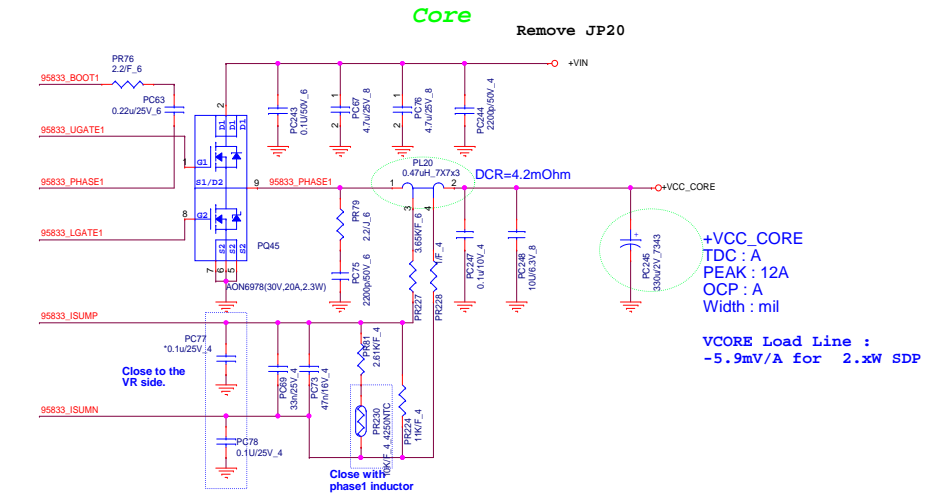
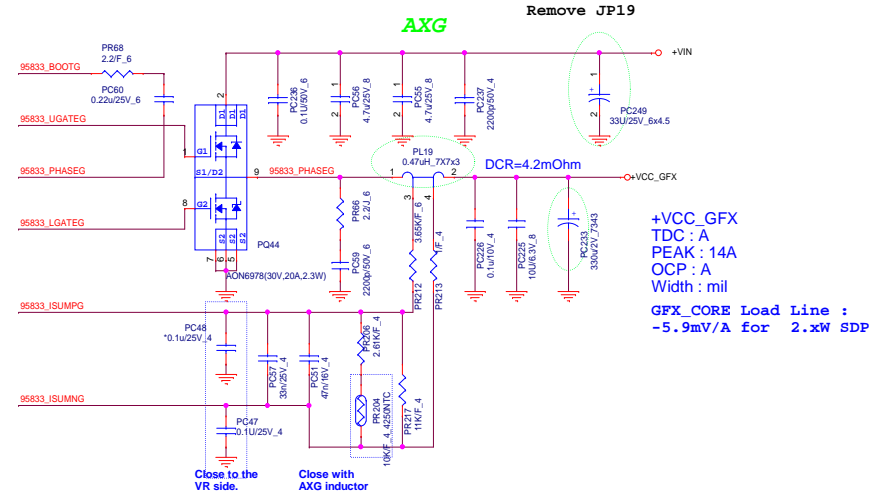
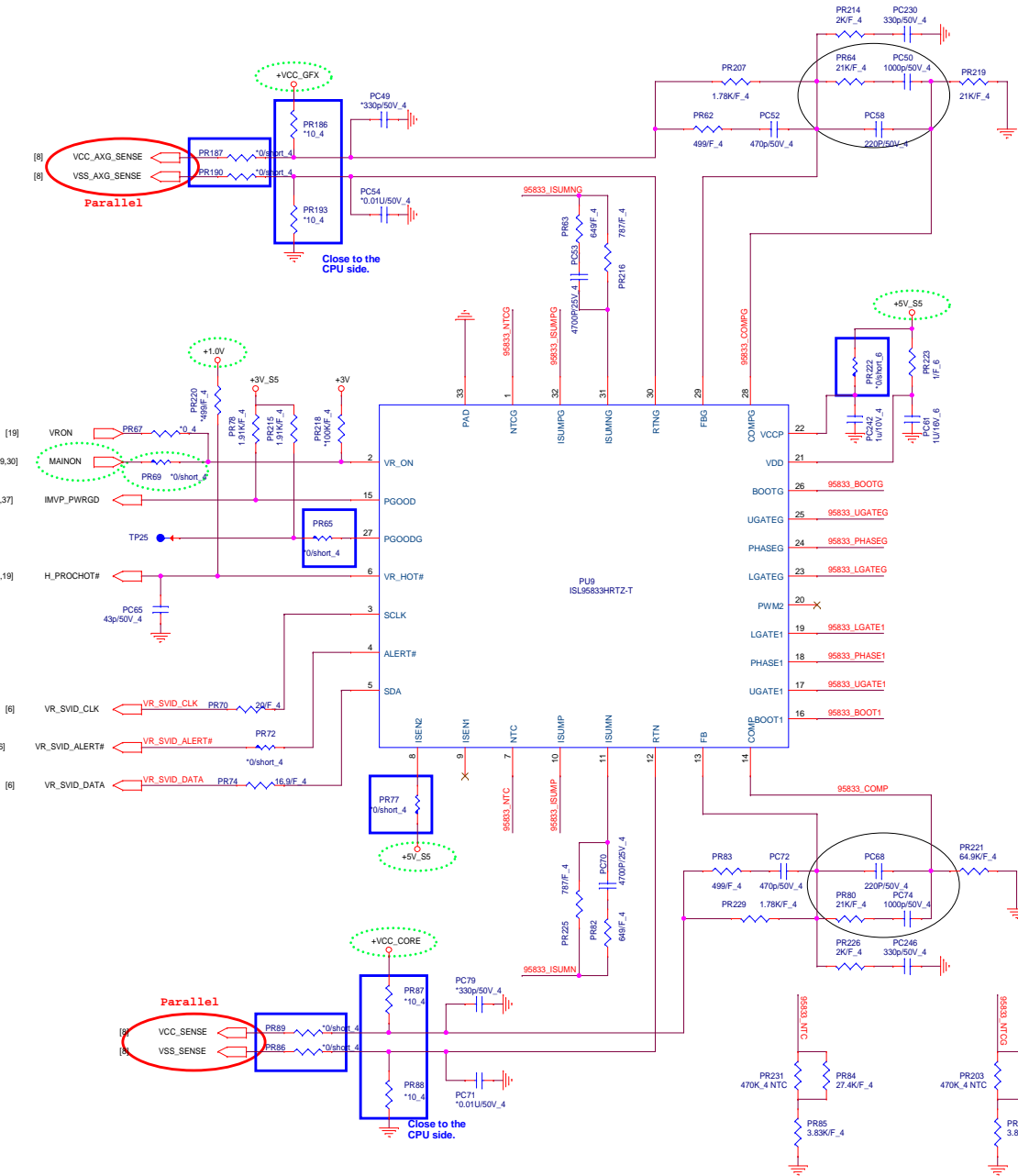
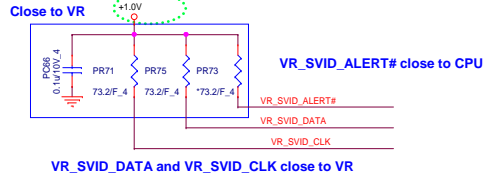
[2,9,12,19,21,24,27,28,35,37,39,40]	+3V_S5	
[5,9]	+1.05V	
[9,22,23,26]	+1.5V	

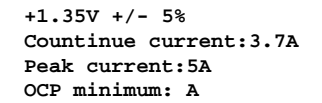


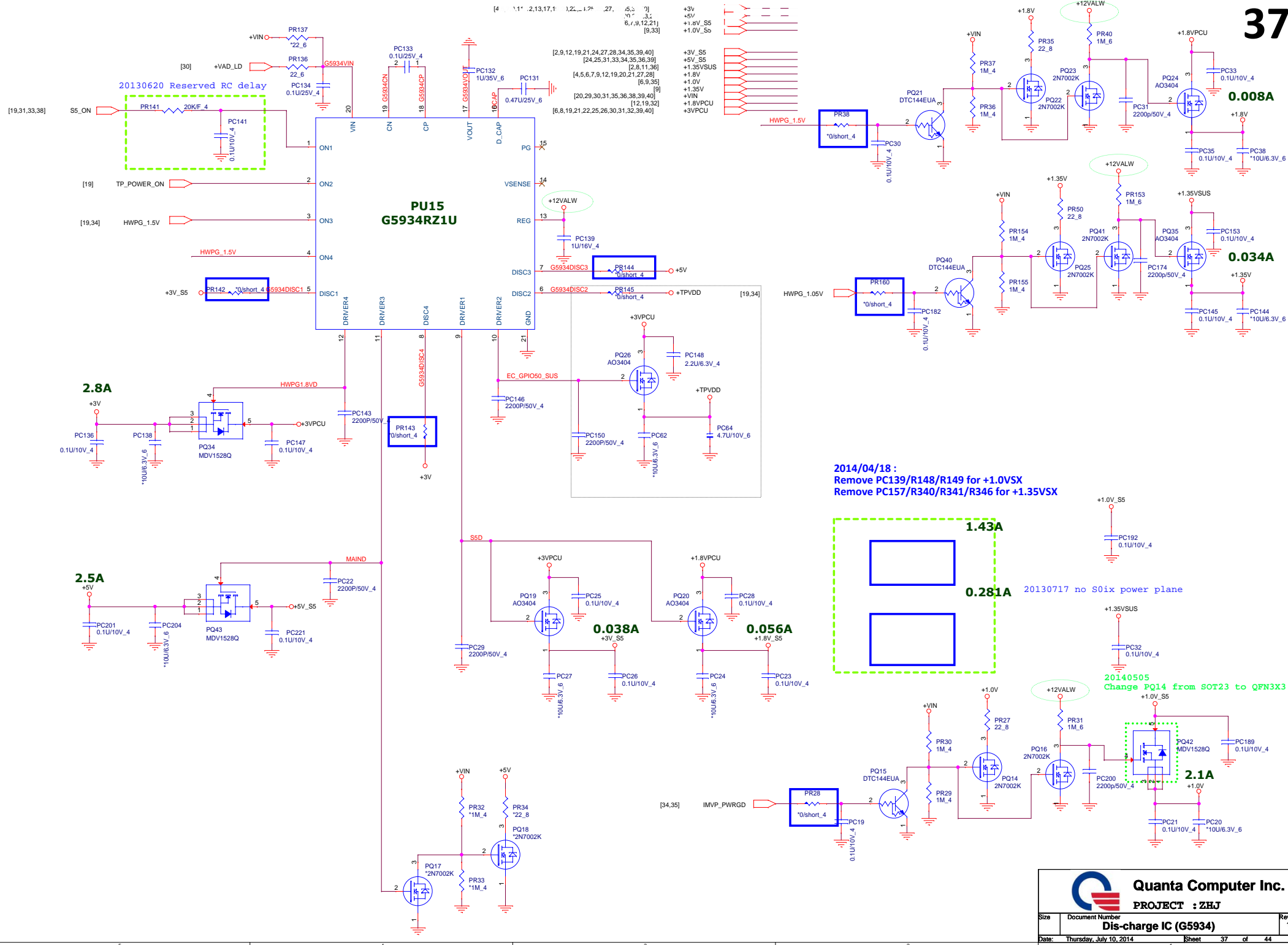
Quanta Computer Inc.
PROJECT : ZHJ

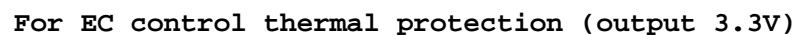
Size	Document Number	Rev
	+1.05V/1.5V	1A
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20130617 Change +1.05V to +1.0V

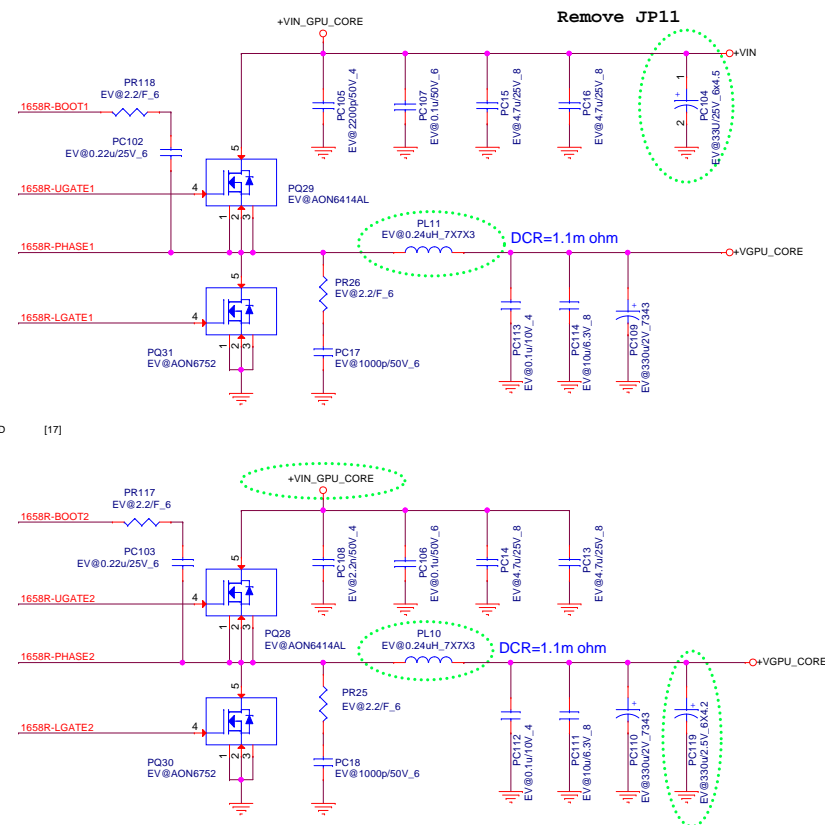








Component	Value	Config D
R1		27K
R2		7.5K
R3		0
R4		6.2K
R5		1.74K
C		5.6nF



N15V-GM

```
+VGPU_CORE
Countinue current:33.5A
Peak current:51.5A
OCP:75A
FSW:300KHz
L/L=0mV/A
```

**Quanta Computer Inc.**

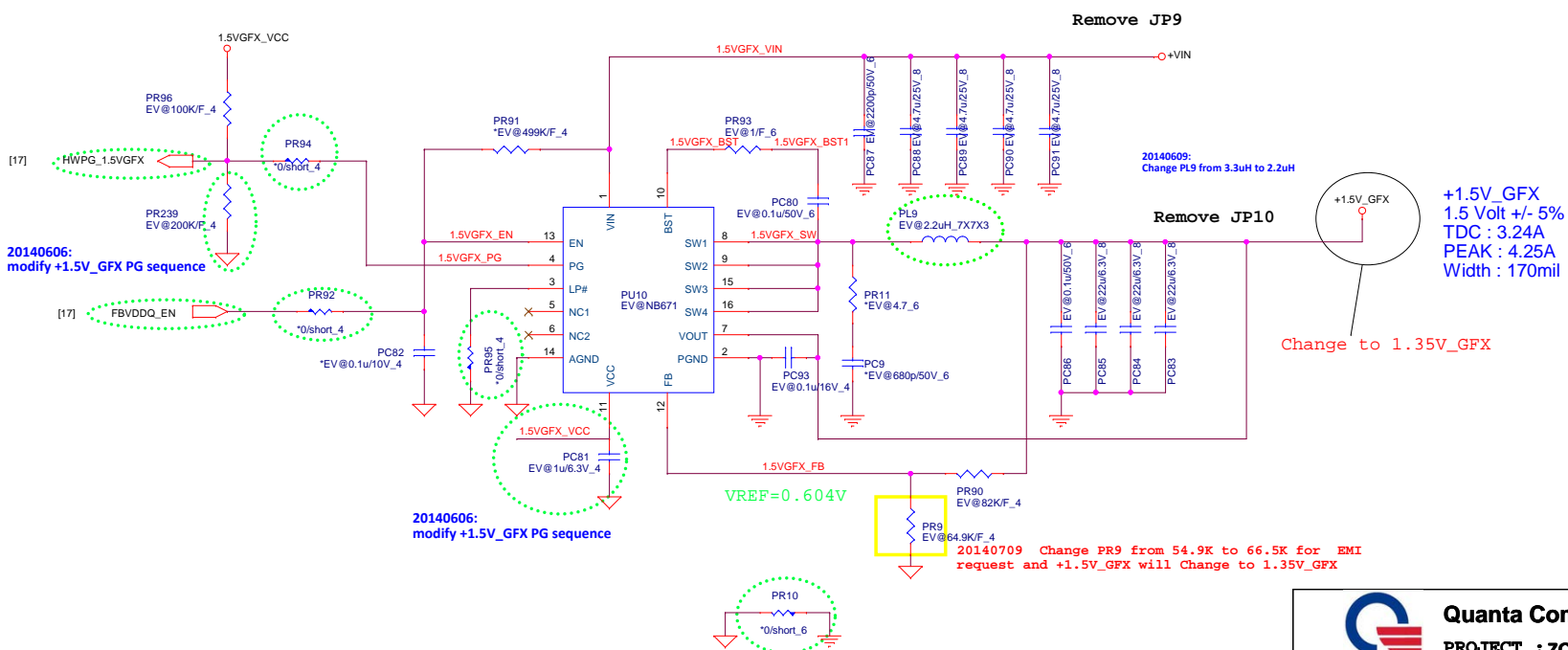
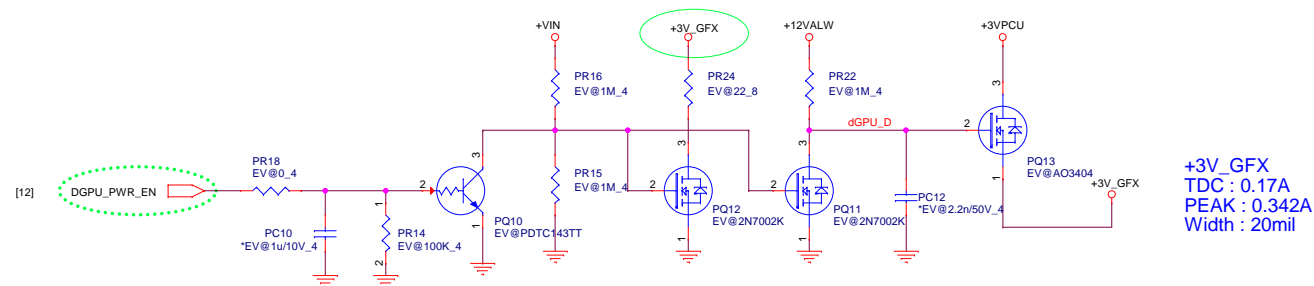
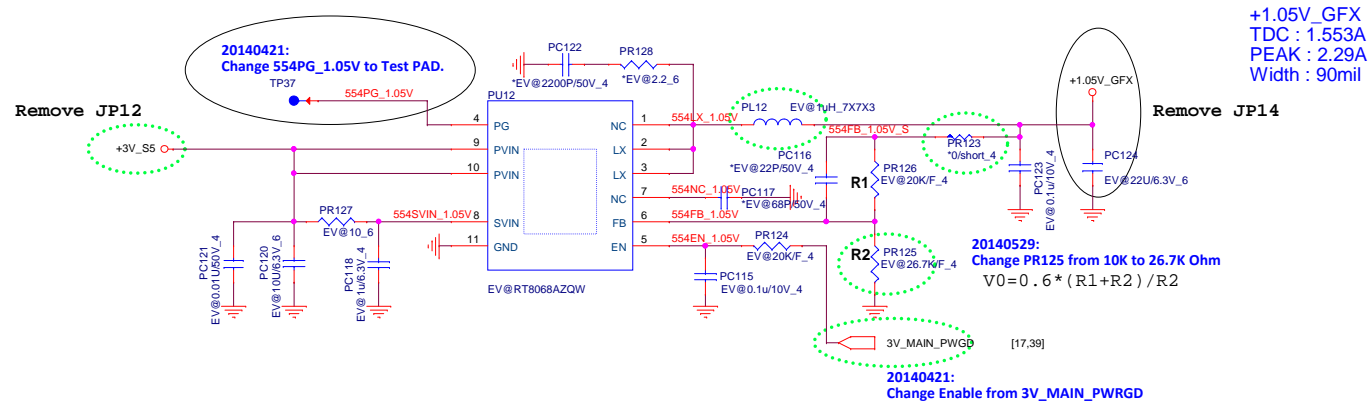
PROJECT : ZOO

+VGPU CORE (UP1658RQKF)

Size	Document Number	Rev
	+VGPU_CORE (UP1658RQKF)	1A
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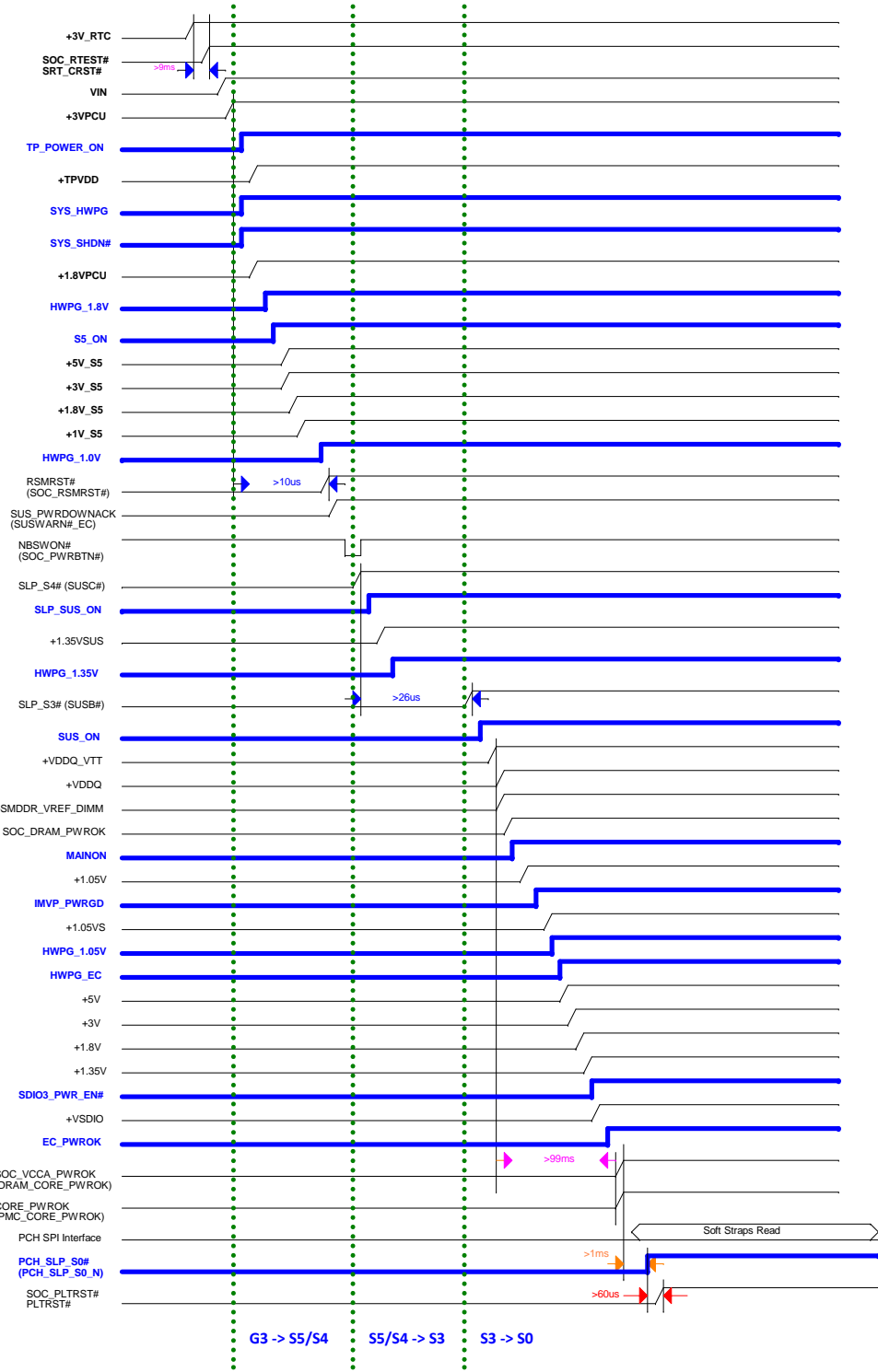
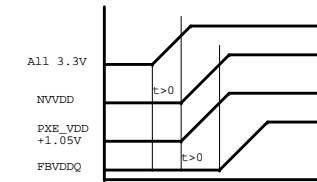
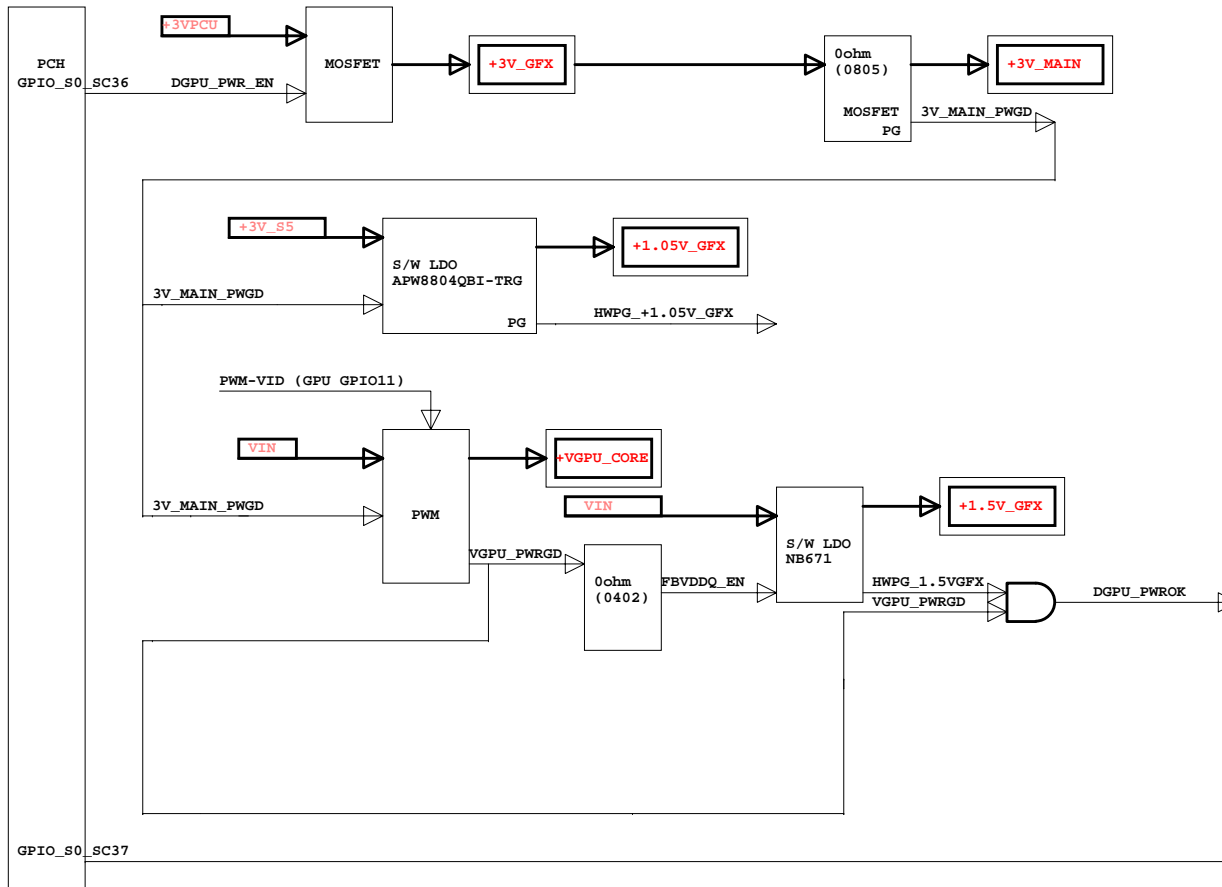


Table 37. SoC Sx-States to SLP_S*#

State	S0	S3	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle
CPU Executing	In C0	OFF	OFF	OFF	No	OFF
PMC_SLP_S3#	HIGH	LOW	LOW	LOW	HIGH	LOW
PMC_SLP_S4#	HIGH	HIGH	LOW	LOW	HIGH	LOW
S0 Power Rails	ON	OFF	OFF	OFF	ON	OFF
PMC_PLTRST#	HIGH	LOW	LOW	LOW	LOW	LOW
PMC_SUS_STAT#	HIGH	LOW	LOW	LOW	HIGH	LOW
PCIe Links	L0, L1	L3	L3	L3	L3 Ready	L3

NOTES: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S5#. PMC_SUS_STAT# is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT# also warns of upcoming reset.

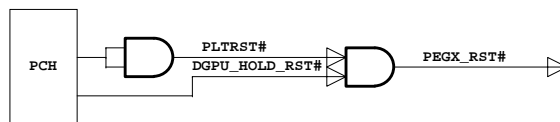
VGA power up sequence



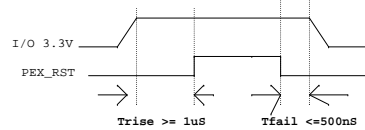
N15x Power on sequence

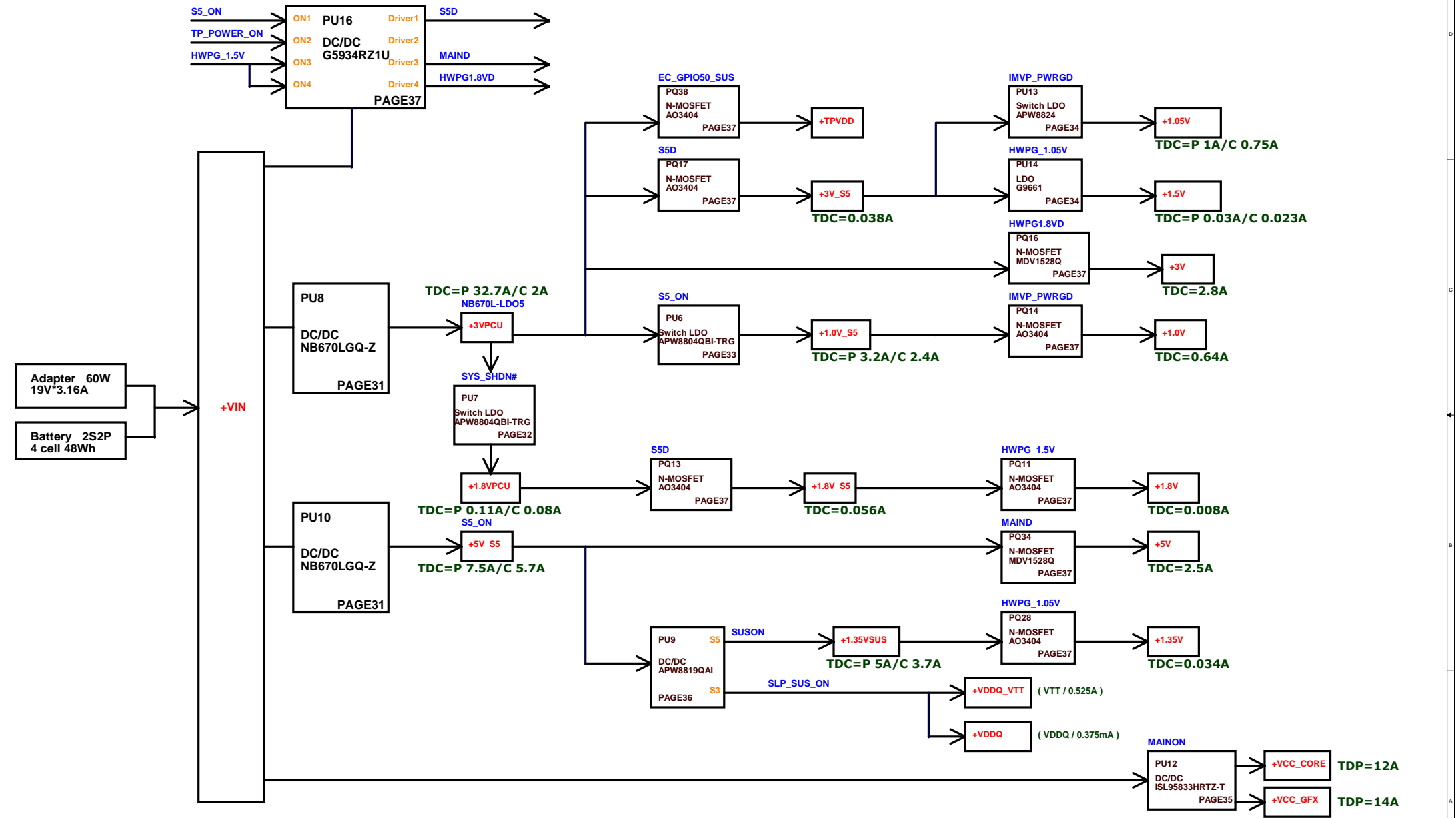
Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V includes all rails that are shared

VGA Reset



PEX_RST timing





Model	Date	CHANGE LIST
ZYL REV:A		1. FIRST RELEASED
		Check CPU of P/N. Change VRAM of P/N. Check PJ6 for UMA or Dis- GVA.
		VGA Chip (Buy and Sell) AJON15V0T07 VR4GbIII9: HYNIX Graphic DDRIII 900 4Gb H5TC4G63APR-11C AKD5PGWTW13 (B/S) MICRON Graphic DDRIII 900 4Gb MT41J256M16HA-093G:E AKD5PZSTL05 (B/S) SAMSUNG Graphic DDRIII 900 4Gb K4W4G1646D-BC1A AKD5PGWT504 (B/S) CPU (Buy and Sell) Intel BayTrail M cpu n3530 VGA Chip (Buy and Sell) AJON15V0T07 VRAM (Buy and Sell) VR2GbIII9 HYNIX Graphic DDRIII 900 2Gb H5TC2G63PFR-11C AKD5MZDTW04 ; AKD5MZDTW05 (B/S) MICRON Graphic DDRIII 900 2Gb MT41J128M16JT-093G:X AKD5MGSTL15 ; AKD5MGSTL25 (B/S)
		SAMSUNG Graphic DDRIII 900 2Gb K4W2G1646Q-BC1A AKD5MGSTL11 ; AKD5MGSTL13 (B/S)
ZYL REV:B	5/27	1.PAGE.22 , modify SW10 pin3 connect to pin1 ,pin2 connect to pin4&pin5&pin6 2.PAGE.24 , modify CN16 & CN18 footprint from "USB-TARA4-9B1323-9P-SMT" to "UB2-UARDM-4K1926-4P-R"
	5/28	1.PAGE.25 , SWAP CN23 USB_CAR_N & USB_CAR_P
	5/29	1.PAGE.40 , Change PR125 from 10K to 26.7K due to 1.05V_GFX output is incorrect
	6/6	1.PAGE.6 , Change C458、C453 from 10P/50V to 12P/50V 2.PAGE.40 , Add PR239 to modify +1.5V_GFX PG sequence
	6/9	1.PAGE.29 , change hole 18、hole20、hole28 footprint from "HG-C315D110P2" to "H-C315D110P2" 2.PAGE.19 , Add D37 D38 C521 3.PAGE.20 , change R66 R67 R69 R70 R71 R73 R74 R76 from 620ohm to 619 ohm 4.PAGE.29 , Change C430 from "CH22206K917" to "CH22206J911" 5.PAGE.22 , Change C464 C466 C468 C469 from "0.01u/16V_4" to "0.01u/25V_4"
	6/10	1.PAGE.29 , reserve & mount C522 C523 C524 for ESD 2.PAGE.40 , Change PL9 from 3.3uH to 2.2uH for modified 1.5V_GFX efficiency.
	6/11	1.PAGE.24 , delete R465 R468 R522 R530 & mount L28,L31 for EMI
	6/13	1.PAGE.7 , PAGE.26,PAGE.28 , unmount R427,C310,R452,R453 2.PAGE.19 , mount D16 and change value form 14V/38V to 5V/30V 3.PAGE.26 , mount C338,C339,C340,C341 for EMI
ZYL REV:C	6/25	1.PAGE.6 , Change G9、G10 footprint from "SOLDERJUMPER-2" to "RC0603-C" 2.PAGE.26 , Change R311、R324、R565、R562、R550、R566、L23、R13 from "0ohm" to "shortpad"
	6/27	1.PAGE.7 & 28 , Unmount R411 & Delete R147,R148,R149 2.PAGE.9 , Delete R180 for CPU +1.0V voltage
	7/1	1.PAGE.24 & 25 , Change C279,C224,C414 from 100u/6.3V_3216 to 100U/6.3V_3528
	7/2	1.PAGE.38 , Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request
	7/9	1.PAGE.40 , Change PR9 from 54.9K to 64.9K for EMI request and +1.5V_GFX will Change to 1.35V_GFX

 Quanta Computer Inc.		DOC NO.	PROJECT MODEL :	ZYL/ZYLA	APPROVED BY:		DATE:
PROJECT : ZYL/ZYLA			PART NUMBER		DRAWING BY:		REVISION:

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