

PCB STACK UP 8L

- LAYER 1 : TOP
- LAYER 2 : SGND
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : SVCC
- LAYER 6 : IN3
- LAYER 7 : SGND1
- LAYER 8 : BOT

D/M Note Block Diagram -- Intel Huron River ULV

POWER		
DC/DC	3V_PCU, 5V_PCU, +15V	Page 31
REGULATOR (DDR3)	1.5V_SUS, 0.75V_DDR_VTT	Page 32
REGULATOR	1.05V&1.8V	Page 33
REGULATOR	VCCSA	Page 34
CPU Core		Page 35
Charger		Page 36
RUN POWER SW/Discharge	5V_SUS, 3V_SS, 5V_SS +3V, +5V	Page 37

DDR3 SO-DIMM 1
(STD)
Page 13

DDR3 SO-DIMM 2
(RVS)
Page 14

Intel Huron River
Sandy Bridge

31mmX24mm, BGA
2 Core 18Watt

Page 3, 4, 5, 6

Environment temperature
Thermal Sensor
Page 26

Charger temperature
Thermal Sensor
Page 26

DDR
Thermal Sensor
Page 13

FDI X4 DMI

Cougar Point
HM65
25mmX25mm, BGA
PCH 3.9Watt

Page 7, 8, 9, 10, 11, 12

HP/Mic
Audio Jack
Page 18

HDA CODEC
CX20671-21Z
Page 18

Internal MIC
Page 18

Internal SPK
Page 18

HD Audio

SPI Flash (4MB)
Page 8

SPI Flash (512K)
Page 28

32.768KHz

LPC BUS

IT8518
Page 28

TPM
(for M-note)
Page 25

Accelerometer
(APS)
Page 25

Int. KB
Page 24

T/P
Page 24

Battery
Page 36

Charger
Page 36

USB Card Reader Realtek RTS5209
Page 21

4 in 1 Socket
SD/SDHC/SDXC/MMC
Page 21

PCI-e/USB Mini PCIe Slot
Page 22

WLAN Module
Page 22

PCI-e/USB Mini PCIe Slot
Page 23

WWAN Module
Page 23

SIM Card
Page 23

PCI-e 10/100/1G Ethernet
AR8151-BL1A-R++
Page 17

RJ-45
Page 17

SATA 2.5" HDD /SSD Module
(Option)
Page 19

LVDS 11.6" HD (1366x768) LCD
Page 15

RGB CRT
Page 16

HDMI HDMI
Page 16

USB Camera Conn
Page 15

Camera Module
Page 15

USB Bluetooth
Page 25

USB USB PORT X 3
Page 20

USB Fingerprint (for M-note)
Page 24

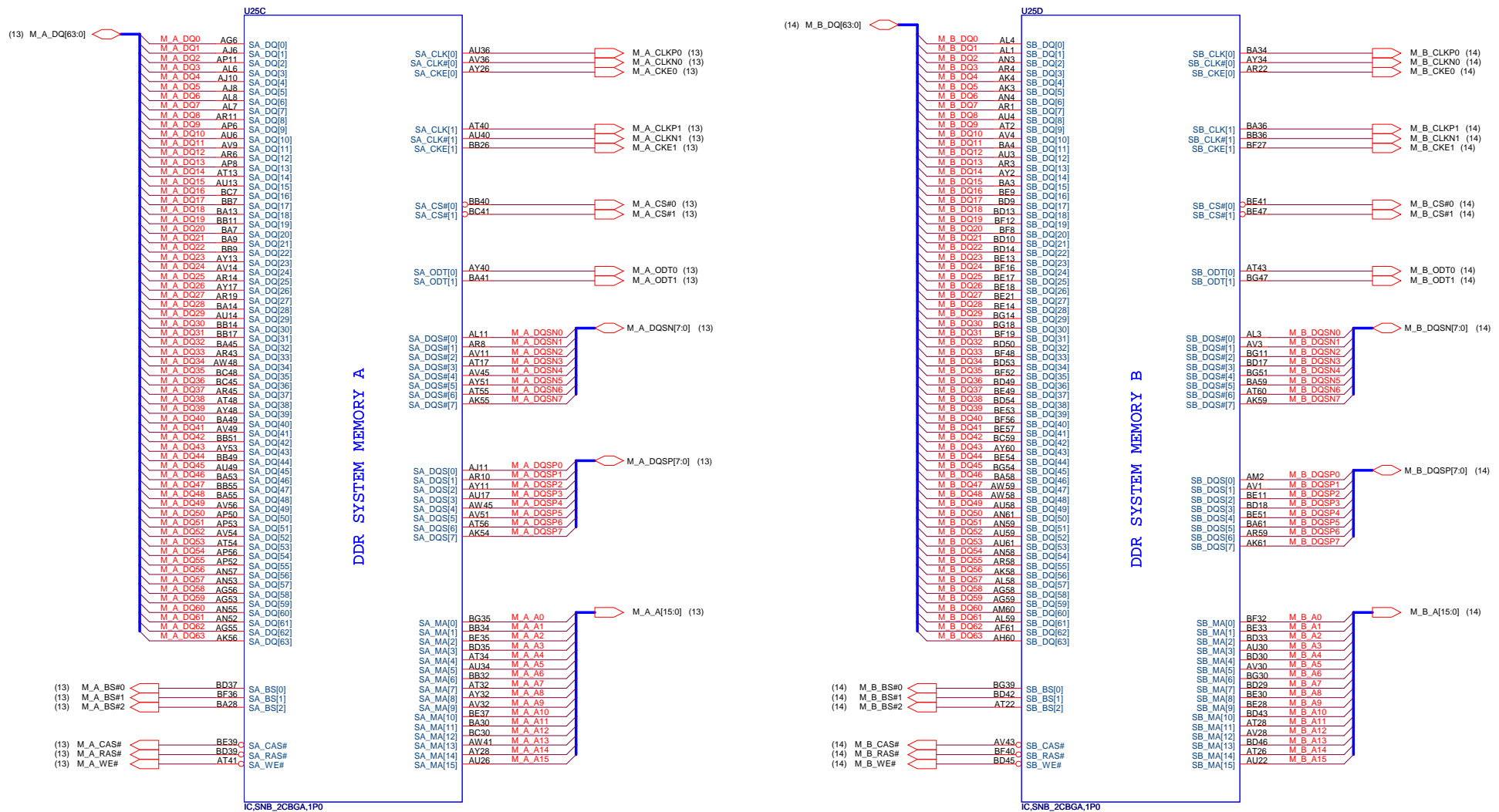
Table of Contents

PAGE	DESCRIPTION
01	LOCK DIAGRAM(UMA)
02	FRONT PAGE
03-06	Sandy Bridge
07-12	Cougar Point-PCH
13-14	DDRIII SO-DIMM
15	LCD/CAMERA
16	CRT/HDMI CONN
17	LAN-RTL8111E-VB-GR
18	AUDIO (CX20671-21Z, SPK)
19	SATA
20	USB X 3
21	Card Reader-RTS5209
22	WLAN
23	WWAN
24	KB/TP/FP
25	BT/G-SENSOR/TPM
26	FAN/Thermal
27	SW/LED/RFID_EEPROM
28	KBC IT8518/19
29	Screw Hole/EMI
30	Power Block Diagram
31	POWER_3V/5V (RT8206MGQW)
32	POWER_DDR3 (TPS51116)
33	POWER_1.05V&1.8V (OZ8117)
34	POWER_+VCCSA (OZ8117)
35	POWER_+VCC_CORE(ISL95831)
36	POWER_Charger (ISL88731A)
37	POWER_Discharge
38	Power On Sequence
39	BOM Matrix Table
40	Schematic Value Descript
41	EC RECORD DV
42	Power EC RECORD DV
43	
44	
45	
46	
47	

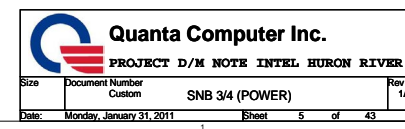
Power States

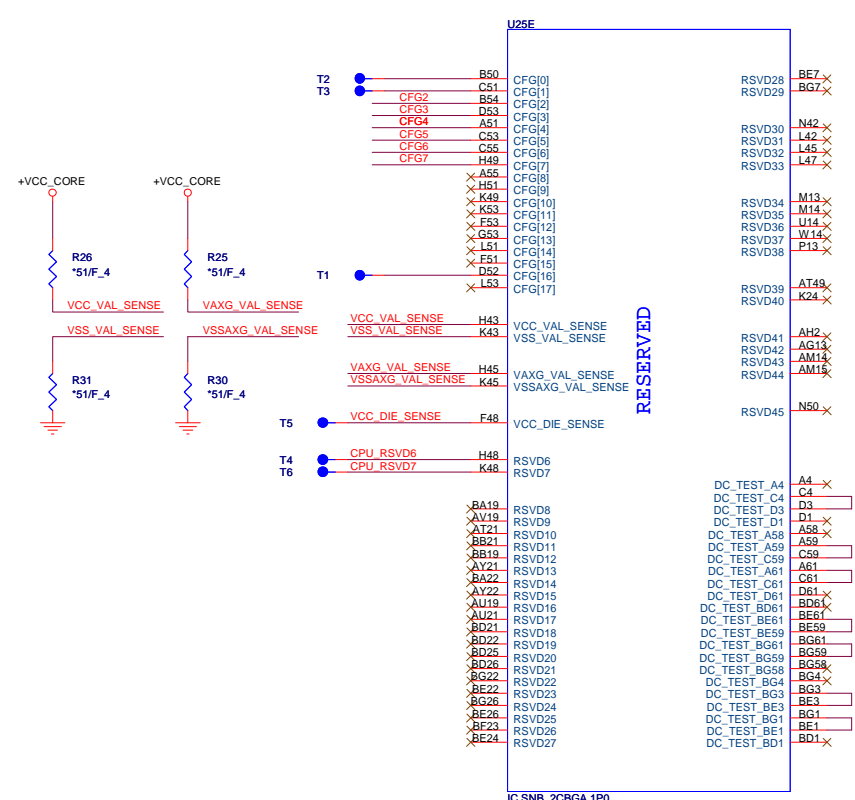
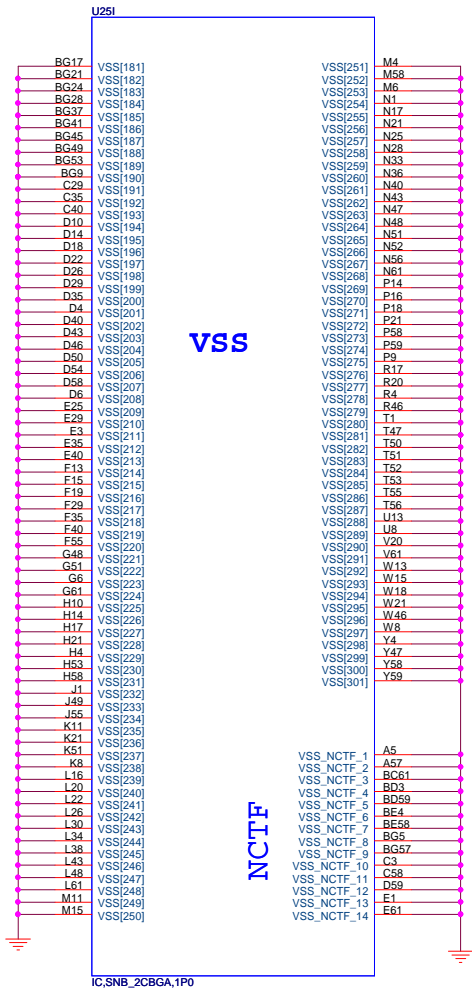
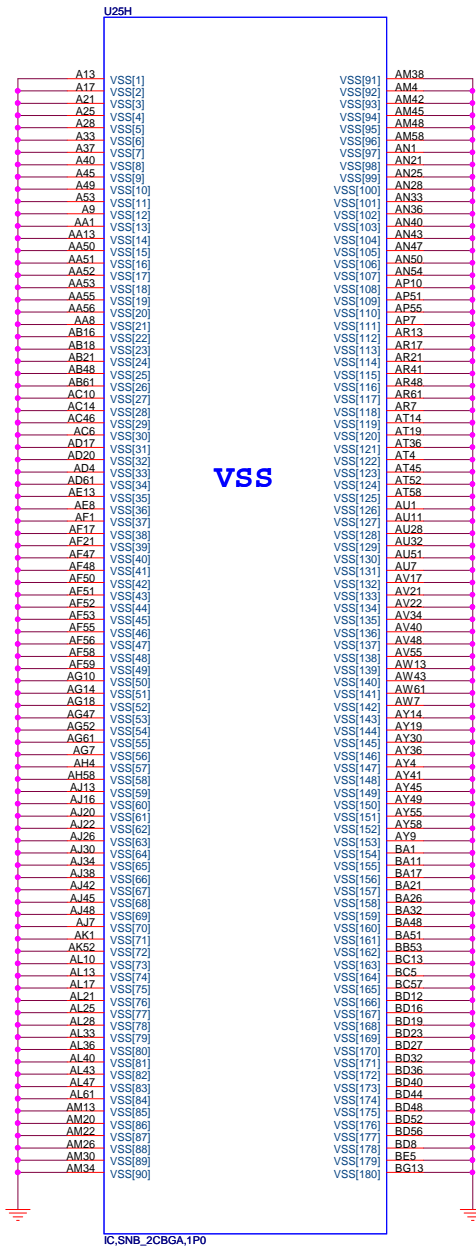
POWER PLANE	VOLTAGE	PAGE	DESCRIPTION	CONTROL SIGNAL	ACTIVE IN
VIN	10V~+20V	15,31,32,33,34,35,36,37	MAIN POWER		S0~S5
+3V_RTC	+3.0V~+3.3V	7,8,11,28	RTC		S0~S5
3VPCU	+3.3V	8,15,16,17,20,27,28,31,33,36,37	IT8518/19 POWER	3V5V_EN	S0~S5
5VPCU	+5V	15,29,31,32,33,34,36,37	DC/DC POWER IC SOURCE	3V5V_EN	S0~S5
+15V	+15V	15,25,31,32,37	LARGE POWER	3V5V_EN	S0~S5
LANVCC	+3.3V	17,37	LAN POWER	LAN_ON	
5V_S5	+5V	11,20,37	PCH SUS POWER	S5_ON	S0~S3
3V_S5	+3.3V	3,7,8,9,10,11,22,25,27,28,37	Sys Management,PCH Resume Well, USB,WLAN,WiMAX POWER	S5_ON	S0~S3
5VSUS	+5V	15,27,35,37	SLP_S4# CTRLD POWER	SUSON	S0~S3
3VSUS	+3.3V	32,37	SLP_S4# CTRLD POWER	SUSON	S0~S3
+1.5VSUS	+1.5V	3,11,13,14,32,37	DDR3 SODIMM POWER	SUSON	S0~S3
+0.75V_DDR_VTT	+0.75V	13,14,32,37	DDR3 SODIMM REFERENCE POWER	MAINON	S0
+5V	+5V	7,8,11,15,16,18,19,24,26,28,29,37	SLP_S3# CTRLD POWER	MAINON	S0
+3V	+3.3V	3,7,8,9,10,11,13,14,15,16,17,18,19,21,22,23, 24, 25,26,27,28,29	SLP_S3# CTRLD POWER	MAINON	S0
+VCC_GFX		5,35,37	VGA CORE POWER	MAINON	S0
+VCCSA	+0.8V~+0.9V	5,34,37	Sandy Bridge Power	MAINON	S0
+1.8V	+1.8V	5,8,11,33,37	LVDS,NVM POWER	MAINON	S0
+1.05V	+1.05V	3,5,7,8,9,11,33,37	Sandy Bridge VTT POWER/PCH CORE POWER	MAINON	S0
+VCC_CORE		5,6,35,37	CPU CORE POWER	VRON	S0
+LCDVCC	+3.3V	15	LCD Power	ENVDD	S0
+3V_HDD	+3V	19	ODD Power	ODD_5V_ON	S0
+5V_HDD	+5V	19	HDD Power	MAINON#	S0
BAT-V	+10V~+17V	36	MAIN BATTERY	CHG_PBATT	S0~S5
+1.5V_CPU	+1.5V	3,5,32,37	DDR3 1.5V Rails	PS_S3CNTRL	S0

Sandy Bridge Processor (DDR3)



05





Processor Strapping

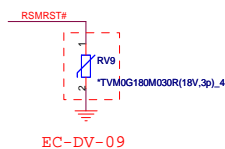
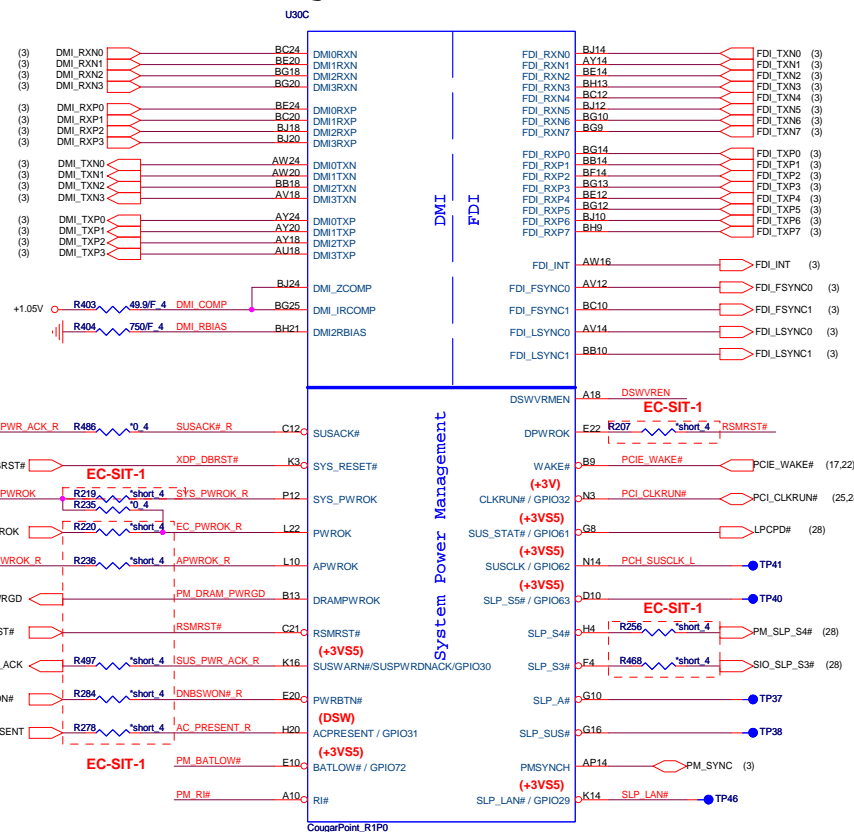
The CFG signals have a default value of '1' if not terminated on the board.

	1	0
CFG2 (PCI-E Static x16 Lane Reversal)	Normal Operation	Lane Reversed
CFG3 (PCI-E Static x4 Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP

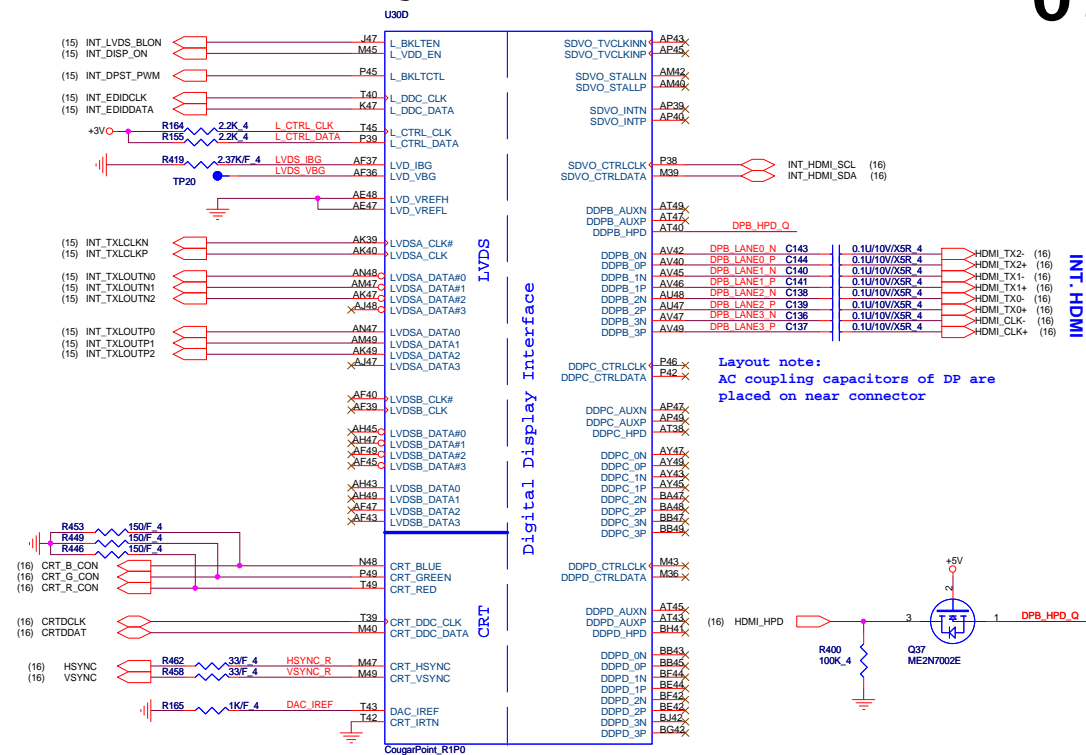
CFG[6:5] (PCIe Port Bifurcation Straps)

11: (Default) x16 - Device 1 functions 1 and 2 disabled
10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

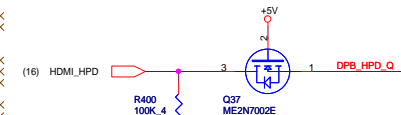
Cougar Point (DMI,FDI,PM)



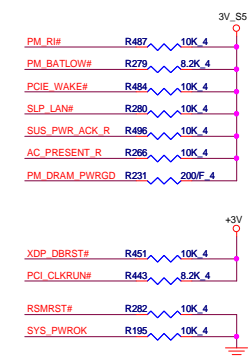
Cougar Point (LVDS,DDI)



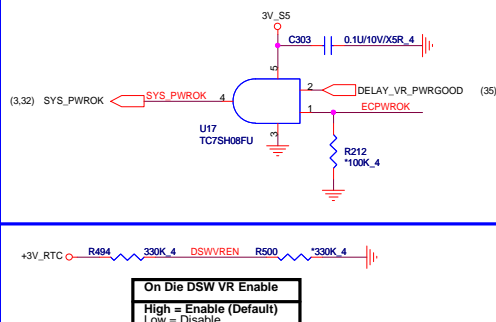
Layout note:
AC coupling capacitors of DP are
placed on near connector




PCH Pull-high/low(CLG)



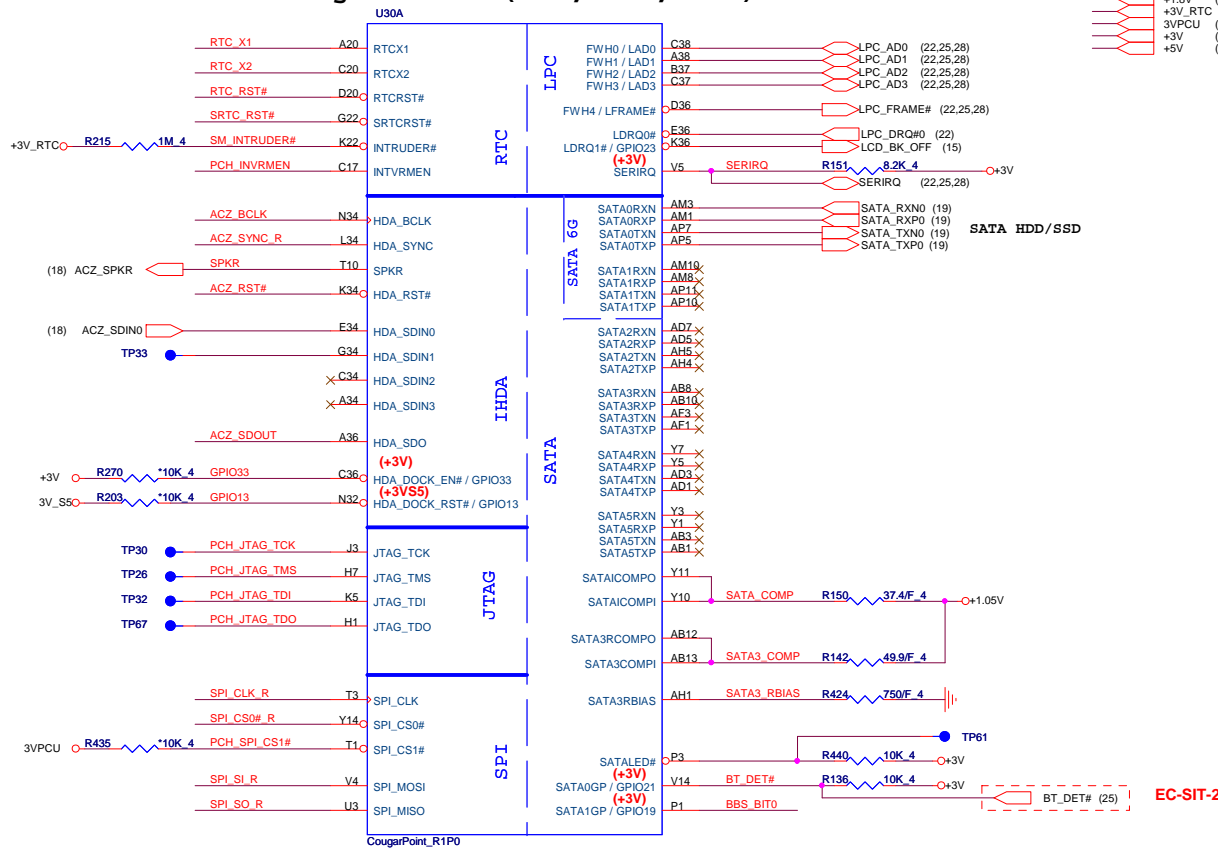
System PWR_OK(CLG)





Signal	Pin Numbers
+1.05V	(3,5,8,9,11,29,33,37)
+3V_RTC	(8,11,28)
3V_S5	(3,8,9,10,11,22,25,28,37)
+3V	(3,8,9,10,11,13,14,15,16,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)
+5V	(11,15,16,18,19,24,26,29,37)

Cougar Point (HDA,JTAG,SATA)



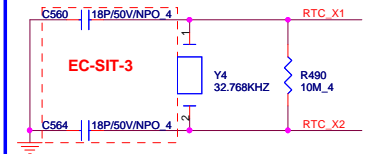
if default boot destination is SPI,
no external pull-up/-down resistors on the board are
necessary

PCH Strap Table

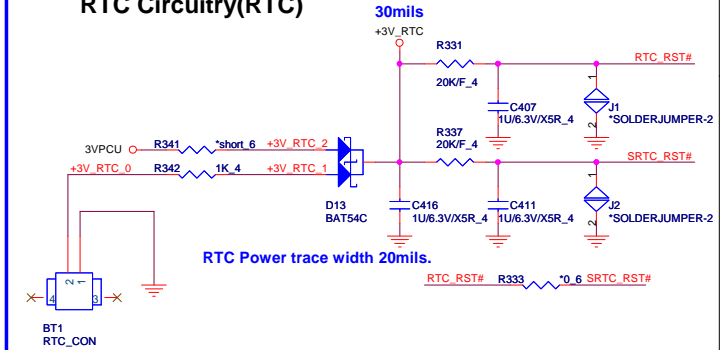
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	Different from Calpella	No reboot mode setting	PWROK 0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	SPKR R172 *1K_4 +3V
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R482 *1K_4 R477 *10K_4 +3V PCH_INTRUDER# R488 330K_4 +3V_RTC
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	PCH_INVRMEN R488 330K_4 +3V_RTC
HDA_SDO	Flash Descriptor Security Only for Interposer	PWROK	0 = effective(Default: weak pull down) 1 = Override	ACZ_SDOUT R224 *1K_4 3V_S5
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK		[Need external pull-down for LPC BIOS]
GPIO19	Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK	R442 *1K_4 R481 *1K_4 BBS_BIT0 BBS_BIT1 (9)
GNT2# / GPIO53	ESI strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN
DF_TVS	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V R416 2.2K_4 (3) PROC_SELECT# R418 1K_4 DF_TVS (10)
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 R201 1K_4 ACZ_SYNC_R
GPIO15				(10) GPIO15 R466 1K_4 3V_S5
GPIO28	Different from Calpella	On-die PLL Voltage Regulator	RSMRST# 0 = Disable 1 = Enable (Default)	R192 *1K_4 PLL_ODRV_EN (10)
DSWVREN		0: disable 1: enable		

RTC Clock 32.768KHz

08



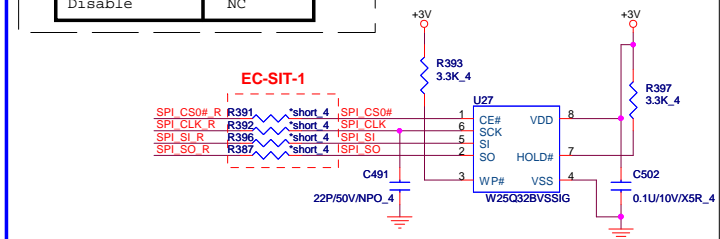
RTC Circuitry(RTC)



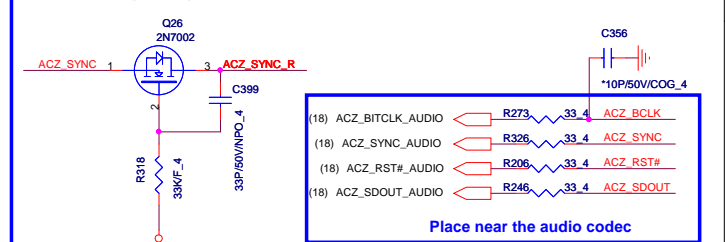
iTPM ENABLE/DISABLE

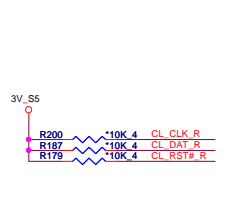
iTPM Function	R366
Enable	1K
Disable	NC

For PCH
32Mbit (4M Byte), SPI

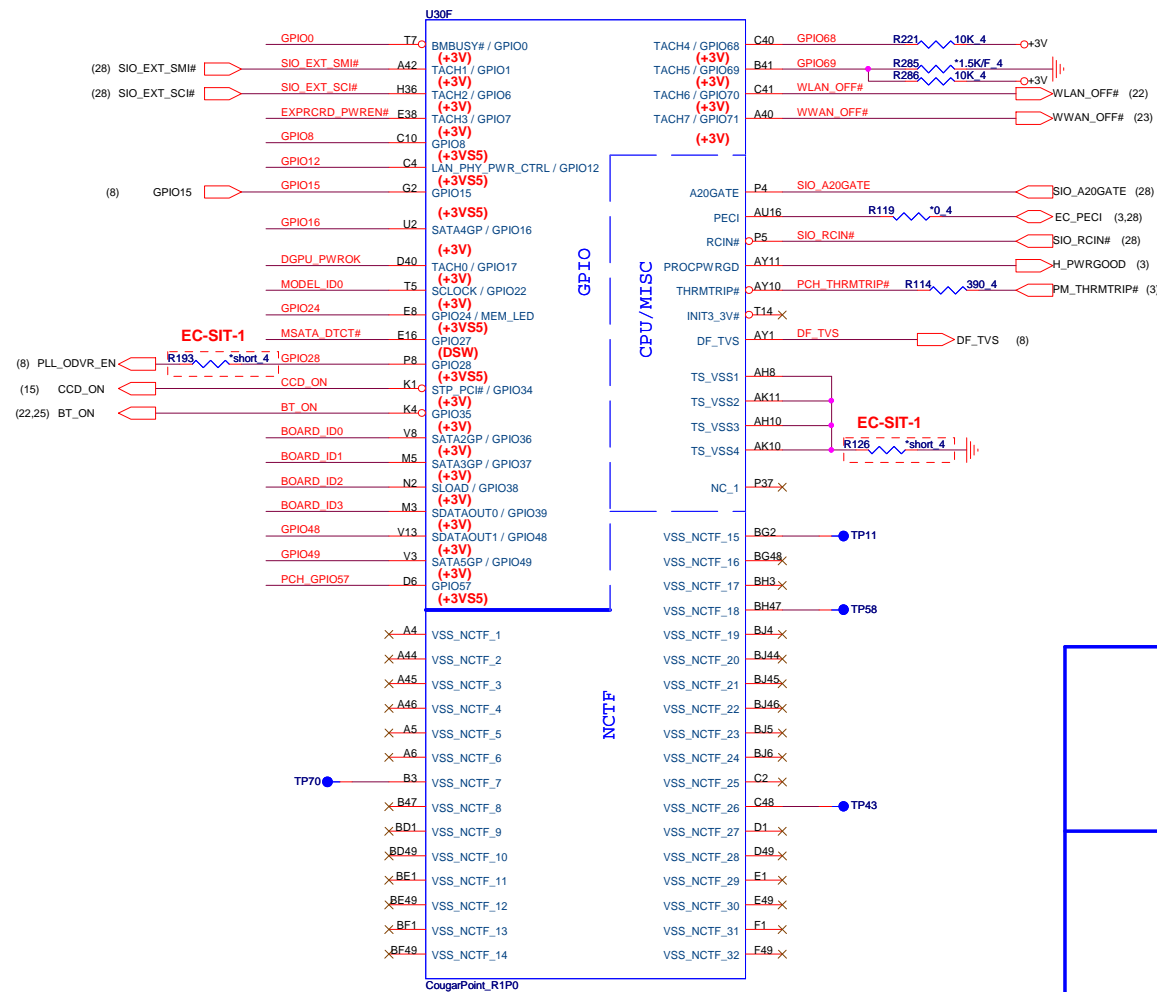


HDA Bus(CLG)

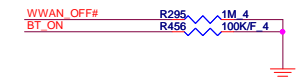
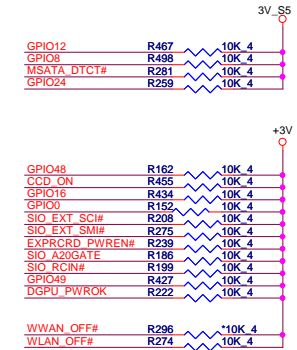




Cougar Point (GPIO,VSS_NCTF,RSVD)



GPIO Pull-up/Pull-down(CLG)

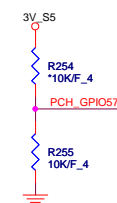
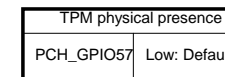
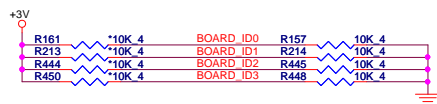
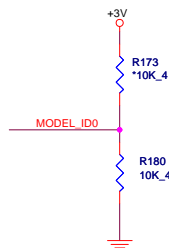



 3V_S5 (3,7,8,9,11,22,25,28,37)
 +3V (3,7,8,9,11,13,14,15,16,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)

BOARD ID SETTING

Board ID For Function	ID3 GPIO39	ID2 GPIO38	ID1 GPIO37	ID0 GPIO36
SDV	0	0	0	0
SIV	0	0	0	1
SIT	0	0	1	0
SVT	0	0	1	1
SOVP	0	1	0	0

Model ID	MODEL_ID0
INTEL	0
AMD	1

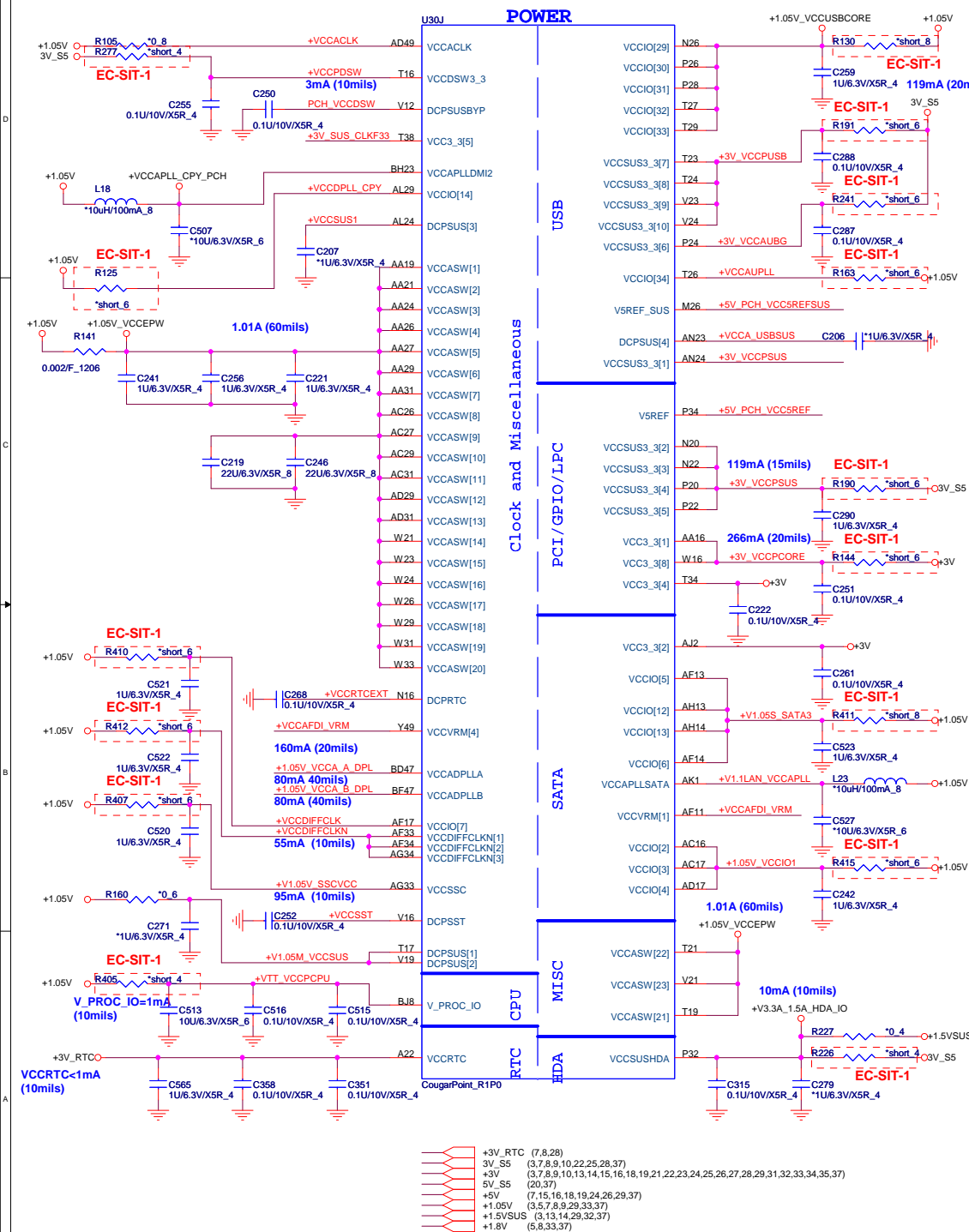


Quanta Computer Inc.

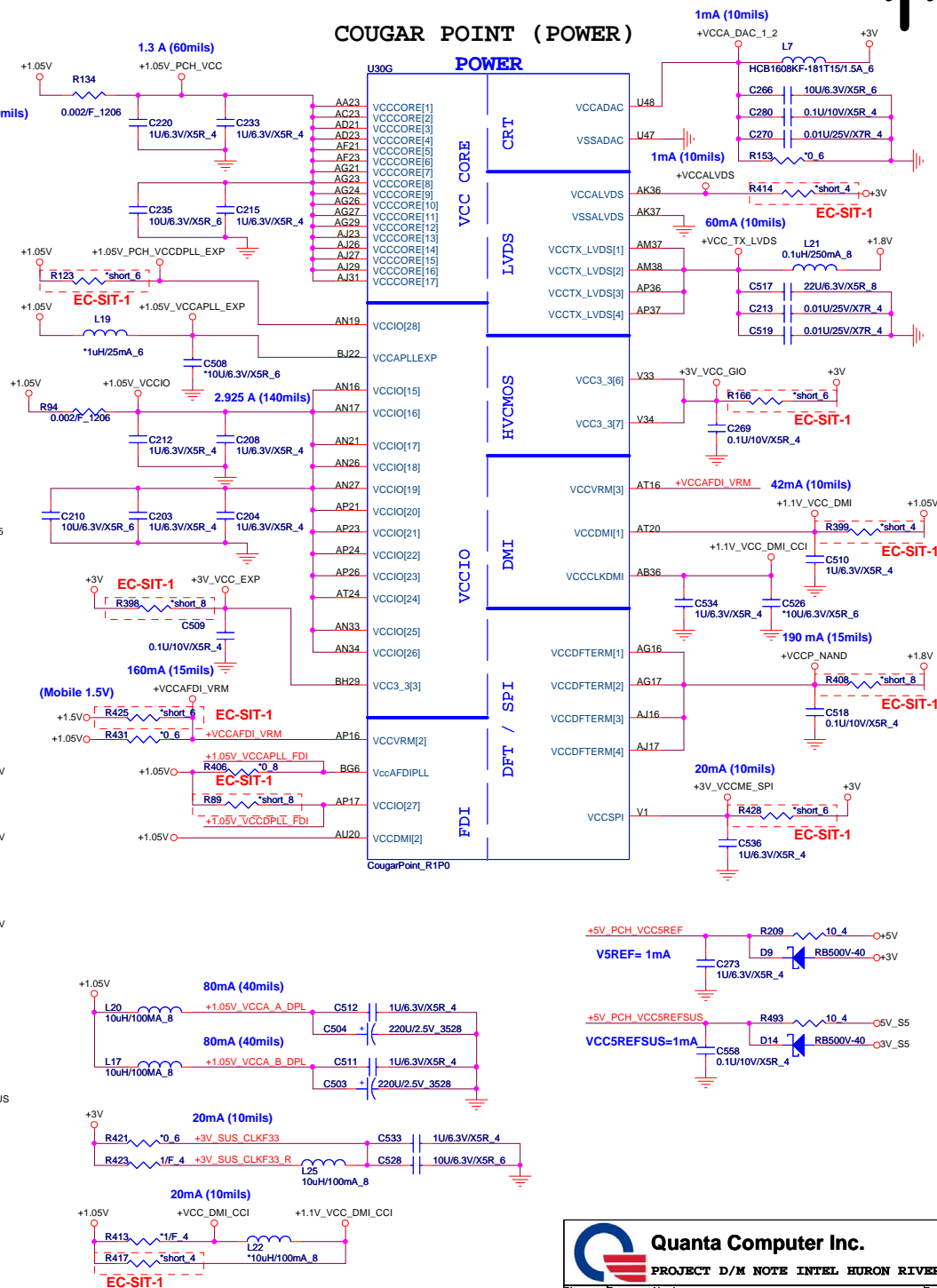
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	PCH 4/6 (GPIO/MISC)	1A
Date:	Monday, January 31, 2011	Sheet 10 of 43

Cougar Point-M (POWER)



COUGAR POINT (POWER)



IBEX PEAK-M (GND)

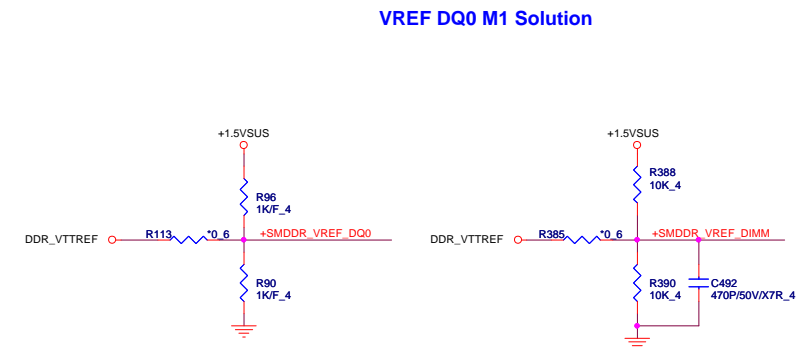
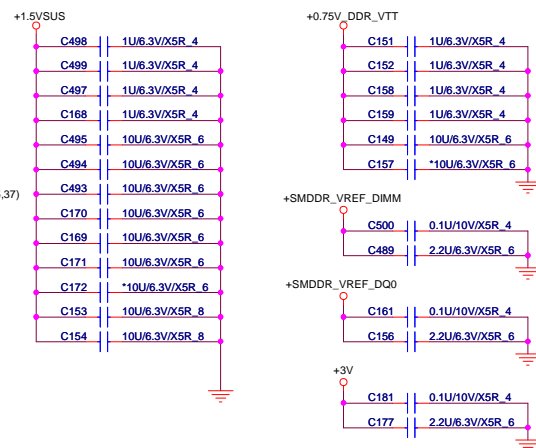
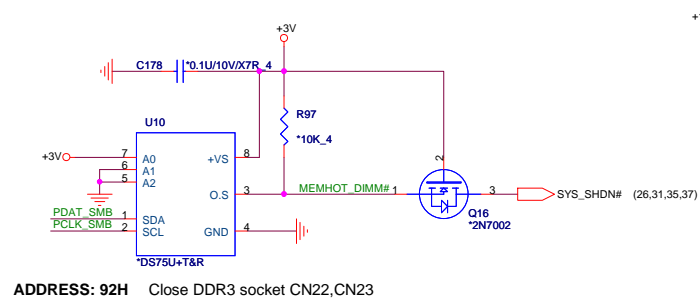
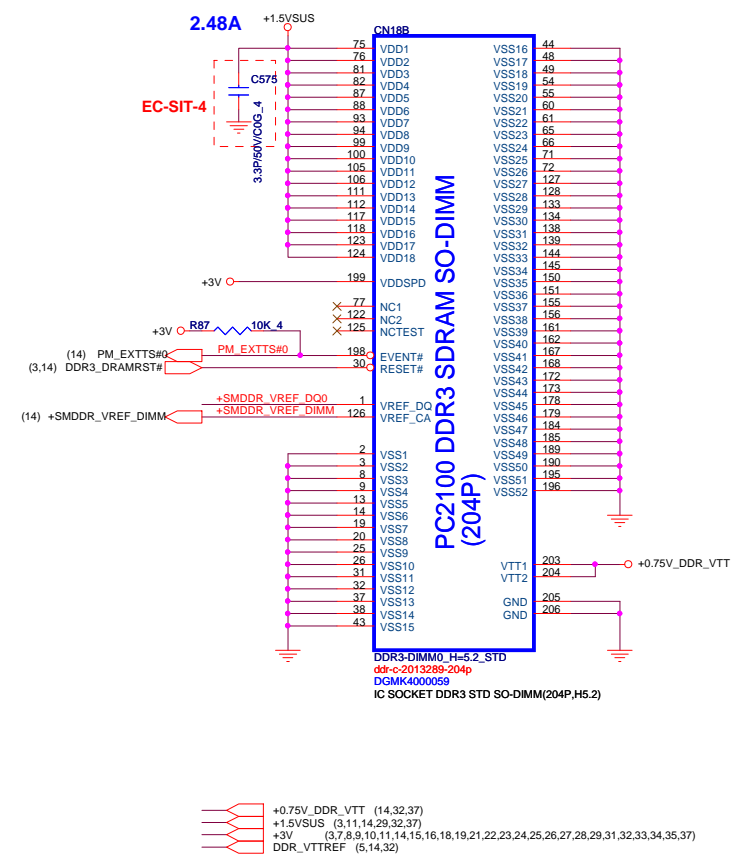
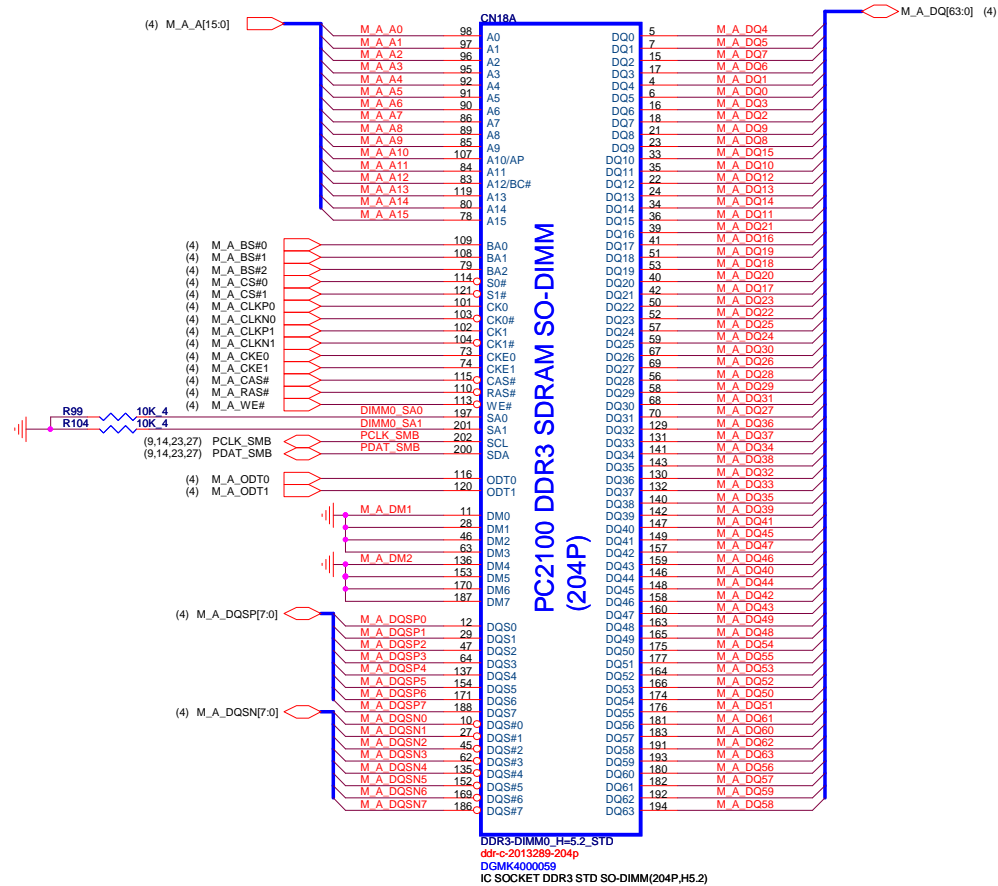
U30I		
AY4	VSS[159]	VSS[259] H46
AY42	VSS[160]	VSS[260] K18
AY46	VSS[161]	VSS[261] K26
AY8	VSS[162]	VSS[262] K39
B11	VSS[163]	VSS[263] K46
B15	VSS[164]	VSS[264] K7
B19	VSS[165]	VSS[265] L18
B23	VSS[166]	VSS[266] L2
B27	VSS[167]	VSS[267] L20
B31	VSS[168]	VSS[268] L26
B35	VSS[169]	VSS[269] L28
B39	VSS[170]	VSS[270] L36
B7	VSS[171]	VSS[271] L48
F45	VSS[172]	VSS[272] M12
BB12	VSS[173]	VSS[273] P16
BB16	VSS[174]	VSS[274] M18
BB20	VSS[175]	VSS[275] M22
BB22	VSS[176]	VSS[276] M24
BB24	VSS[177]	VSS[277] M30
BB28	VSS[178]	VSS[278] M32
BB30	VSS[179]	VSS[279] M34
BB38	VSS[180]	VSS[280] M38
BB4	VSS[181]	VSS[281] M4
BB46	VSS[182]	VSS[282] M42
BC14	VSS[183]	VSS[283] M46
BC18	VSS[184]	VSS[284] M8
BC2	VSS[185]	VSS[285] N18
BC22	VSS[186]	VSS[286] P30
BC32	VSS[187]	VSS[287] N47
BC34	VSS[188]	VSS[288] P11
BC36	VSS[189]	VSS[289] P18
BC40	VSS[190]	VSS[290] T33
BC42	VSS[191]	VSS[291] P40
BC48	VSS[192]	VSS[292] P43
BD46	VSS[193]	VSS[293] P47
BD5	VSS[194]	VSS[294] P7
BE22	VSS[195]	VSS[295] R2
BE26	VSS[196]	VSS[296] R48
BE40	VSS[197]	VSS[297] T12
BE10	VSS[198]	VSS[298] T31
BE12	VSS[199]	VSS[299] T37
BE16	VSS[200]	VSS[300] T4
BE20	VSS[201]	VSS[301] W34
BF20	VSS[202]	VSS[302] T46
BF22	VSS[203]	VSS[303] T47
BF24	VSS[204]	VSS[304] T8
BF26	VSS[205]	VSS[305] V11
BF28	VSS[206]	VSS[306] V17
BD3	VSS[207]	VSS[307] V26
BF40	VSS[208]	VSS[308] V27
BF38	VSS[209]	VSS[309] V29
BF40	VSS[210]	VSS[310] V31
BF8	VSS[211]	VSS[311] V36
BG17	VSS[212]	VSS[312] V39
BG21	VSS[213]	VSS[313] V43
BG33	VSS[214]	VSS[314] V7
BG44	VSS[215]	VSS[315] W17
BG8	VSS[216]	VSS[316] W19
BH11	VSS[217]	VSS[317] W2
BH15	VSS[218]	VSS[318] W27
BH17	VSS[219]	VSS[319] W48
BH19	VSS[220]	VSS[320] Y12
H10	VSS[221]	VSS[321] Y38
BH27	VSS[222]	VSS[322] Y4
BH31	VSS[223]	VSS[323] Y42
BH33	VSS[224]	VSS[324] Y46
BH35	VSS[225]	VSS[325] Y8
BH39	VSS[226]	VSS[326] BG29
BH43	VSS[227]	VSS[327] A3
BH7	VSS[228]	VSS[328] AD47
D3	VSS[229]	VSS[329] AH11
D12	VSS[230]	VSS[330] AH3
D16	VSS[231]	VSS[331] AH36
D18	VSS[232]	VSS[332] B43
D22	VSS[233]	VSS[333] BE10
D24	VSS[234]	VSS[334] BH40
D26	VSS[235]	VSS[335] BH42
D30	VSS[236]	VSS[336] BH46
D32	VSS[237]	VSS[337] AH7
D34	VSS[238]	VSS[338] AJ19
D38	VSS[239]	VSS[339] T36
D42	VSS[240]	VSS[340] BG22
D8	VSS[241]	VSS[341] BG24
E18	VSS[242]	VSS[342] C22
E26	VSS[243]	VSS[343] AP13
G18	VSS[244]	VSS[344] M14
G20	VSS[245]	VSS[345] AP3
G26	VSS[246]	VSS[346] AP1
G28	VSS[247]	VSS[347] BE16
G36	VSS[248]	VSS[348] BC16
G48	VSS[249]	VSS[349] BG28
H12	VSS[250]	VSS[350] BJ28
H18	VSS[251]	VSS[351]
H22	VSS[252]	VSS[352]
H24	VSS[253]	
H26	VSS[254]	
H30	VSS[255]	
H32	VSS[256]	
H34	VSS[257]	
F3	VSS[258]	

CougarPoint_R1P0


IBEX PEAK-M (GND)

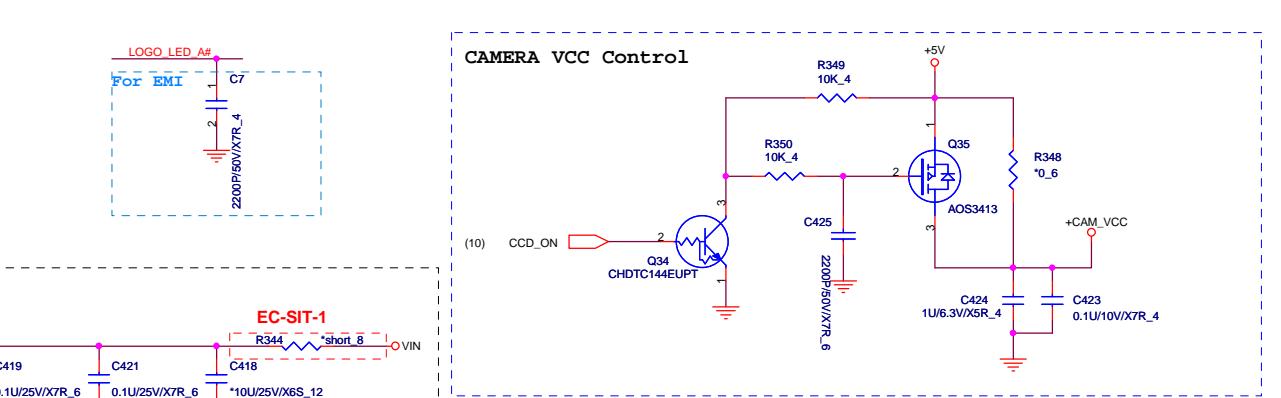
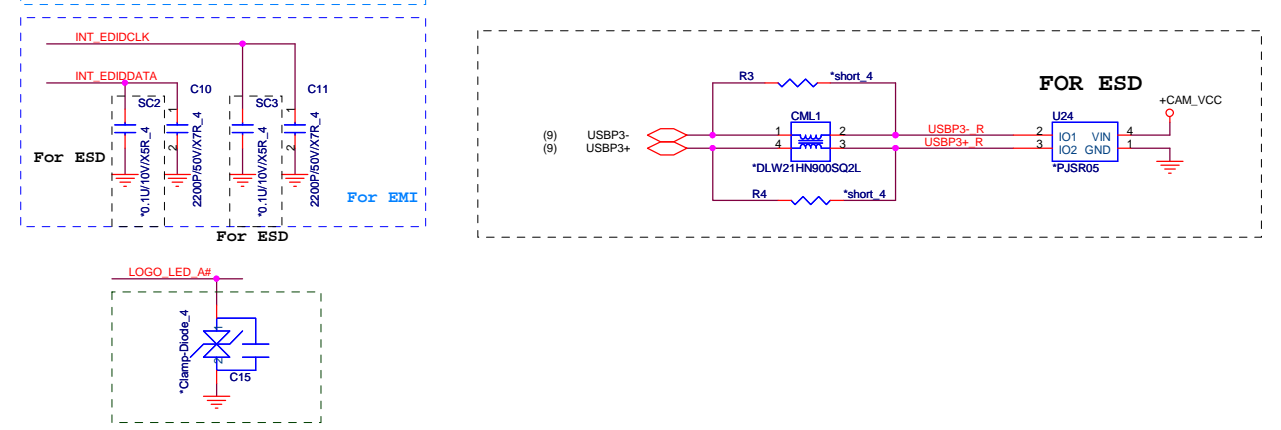
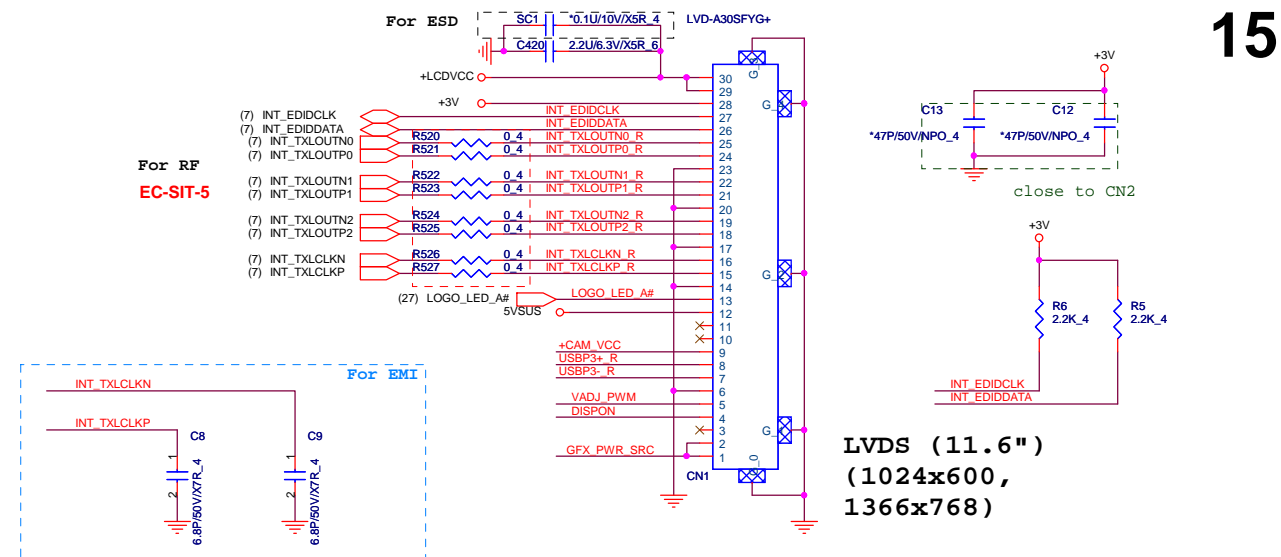
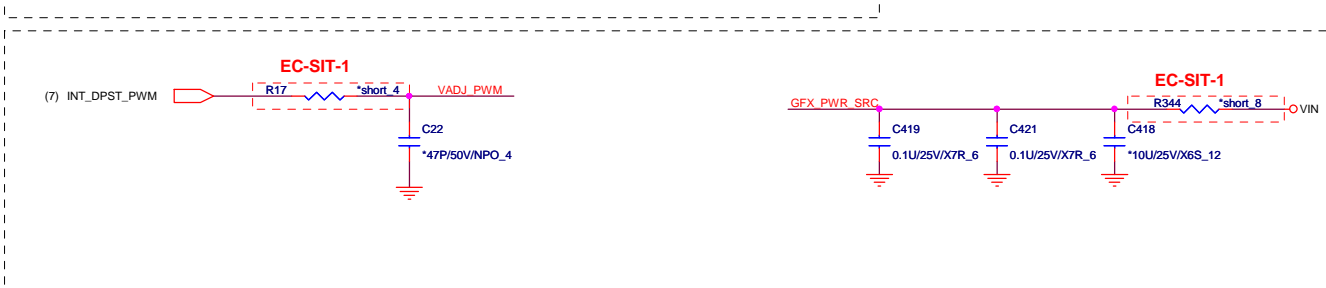
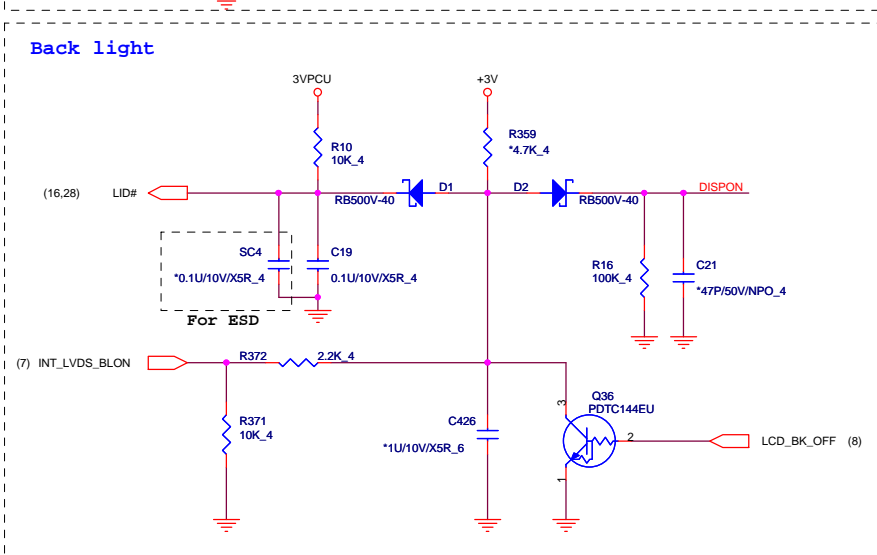
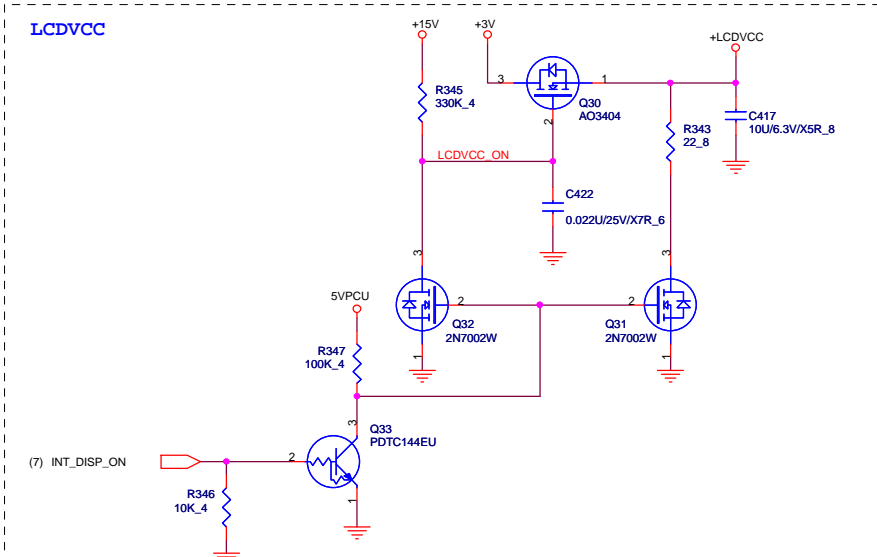
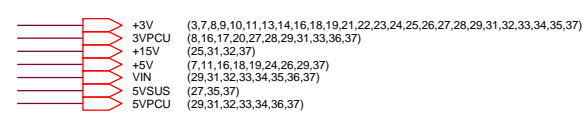
U30H		
H5	VSS[0]	
AA17	VSS[1]	VSS[80] AK38
AA2	VSS[2]	VSS[81] AK4
AA3	VSS[3]	VSS[82] AK42
AA33	VSS[4]	VSS[83] AK46
AA34	VSS[5]	VSS[84] AK8
AB11	VSS[6]	VSS[85] AL16
AB14	VSS[7]	VSS[86] AL17
AB39	VSS[8]	VSS[87] AL19
AB4	VSS[9]	VSS[88] AL2
AB43	VSS[10]	VSS[89] AL21
AB5	VSS[11]	VSS[90] AL23
AB7	VSS[12]	VSS[91] AL26
AC19	VSS[13]	VSS[92] AL27
AC2	VSS[14]	VSS[93] AL31
AC21	VSS[15]	VSS[94] AL33
AC24	VSS[16]	VSS[95] AL34
AC33	VSS[17]	VSS[96] AL48
AC34	VSS[18]	VSS[97] AM11
AC48	VSS[19]	VSS[98] AM14
AD10	VSS[20]	VSS[99] AM36
AD11	VSS[21]	VSS[100] AM39
AD12	VSS[22]	VSS[101] AM43
AD13	VSS[23]	VSS[102] AM45
AD19	VSS[24]	VSS[103] AM46
AD24	VSS[25]	VSS[104] AM7
AD26	VSS[26]	VSS[105] AN2
AD27	VSS[27]	VSS[106] AN29
AD33	VSS[28]	VSS[107] AN3
AD34	VSS[29]	VSS[108] AN31
AD36	VSS[30]	VSS[109] AP12
AD37	VSS[31]	VSS[110] AP19
AD38	VSS[32]	VSS[111] AP28
AD39	VSS[33]	VSS[112] AP30
AD4	VSS[34]	VSS[113] AP32
AD40	VSS[35]	VSS[114] AP38
AD42	VSS[36]	VSS[115] AP4
AD43	VSS[37]	VSS[116] AP42
AD45	VSS[38]	VSS[117] AP46
AD46	VSS[39]	VSS[118] AP8
AD8	VSS[40]	VSS[119] AR2
AE2	VSS[41]	VSS[120] AR48
AE3	VSS[42]	VSS[121] AT11
AF10	VSS[43]	VSS[122] AT13
AF12	VSS[44]	VSS[123] AT18
AD14	VSS[45]	VSS[124] AT22
AD16	VSS[46]	VSS[125] AT26
AF18	VSS[47]	VSS[126] AT28
AF19	VSS[48]	VSS[127] AT30
AF24	VSS[49]	VSS[128] AT32
AF26	VSS[50]	VSS[129] AT34
AF27	VSS[51]	VSS[130] AT39
AF28	VSS[52]	VSS[131] AT42
AF31	VSS[53]	VSS[132] AT46
AF38	VSS[54]	VSS[133] AT7
AF4	VSS[55]	VSS[134] AU24
AF42	VSS[56]	VSS[135] AU30
AF46	VSS[57]	VSS[136] AV16
AF5	VSS[58]	VSS[137] AV20
AF7	VSS[59]	VSS[138] AV24
AF8	VSS[60]	VSS[139] AV30
AG19	VSS[61]	VSS[140] AV38
AG2	VSS[62]	VSS[141] AV4
AG31	VSS[63]	VSS[142] AV43
AG48	VSS[64]	VSS[143] AV8
AH11	VSS[65]	VSS[144] AW14
AH3	VSS[66]	VSS[145] AW18
AH36	VSS[67]	VSS[146] AW2
B43	VSS[68]	VSS[147] AW22
BE10	VSS[69]	VSS[148] AW26
BH40	VSS[70]	VSS[149] AW28
BH42	VSS[71]	VSS[150] AW32
AH46	VSS[72]	VSS[151] AW34
AH7	VSS[73]	VSS[152] AW36
AJ19	VSS[74]	VSS[153] AW40
AJ21	VSS[75]	VSS[154] AW48
AJ24	VSS[76]	VSS[155] AV11
AJ33	VSS[77]	VSS[156] AV12
AJ34	VSS[78]	VSS[157] AY22
AK12	VSS[79]	VSS[158] AY28
AK3		

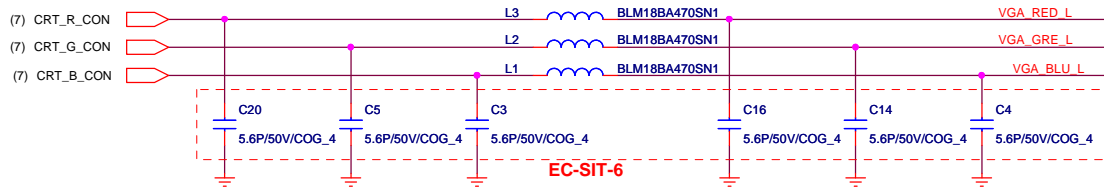
CougarPoint_R1P0





	Quanta Computer Inc. PROJECT D/M NOTE INTEL HURON RIVER	Rev 1A
Size	Document Number Custom	
	DDR3 DIMM1-RVS (4.0H)	
Date:	Monday, January 31, 2011	Sheet 14 of 43

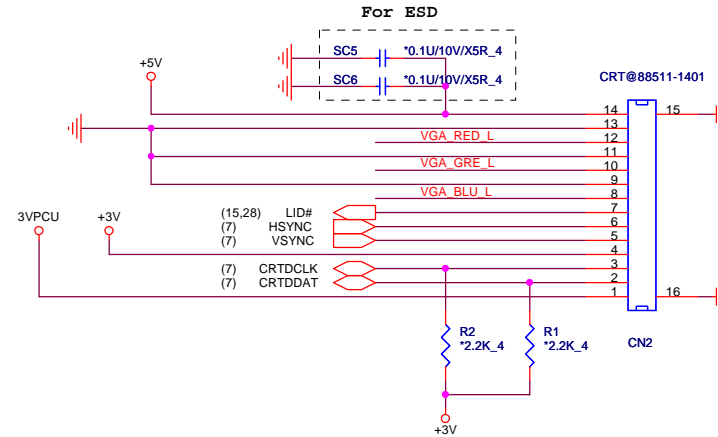




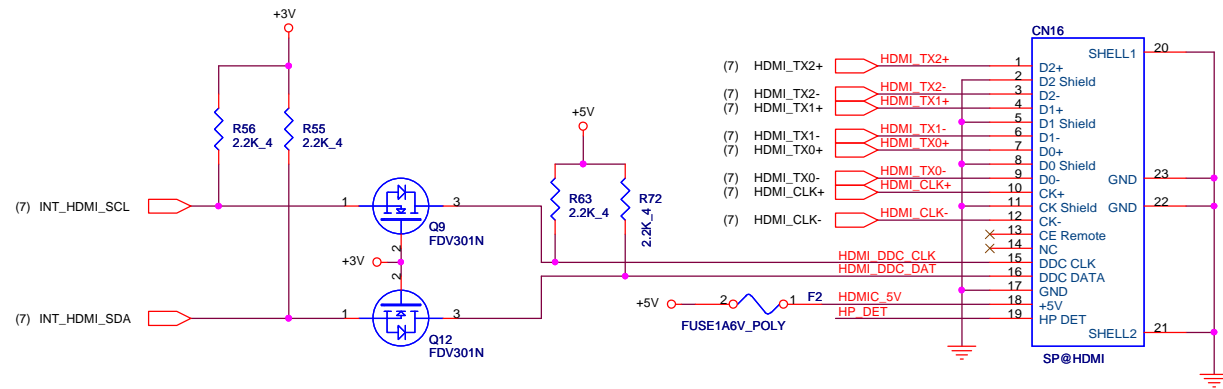
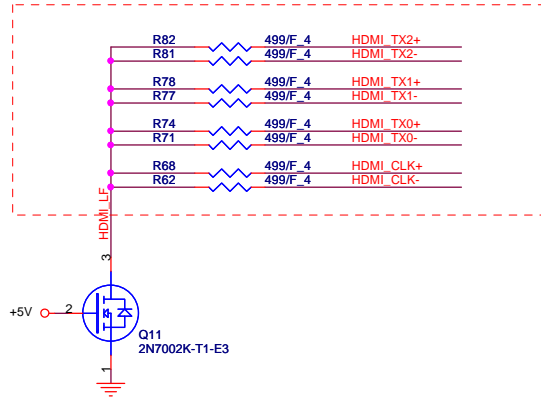
(8,15,17,20,27,28,29,31,33,36,37) 3VPCU

(3,7,8,9,10,11,13,14,15,18,19,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37) +3V

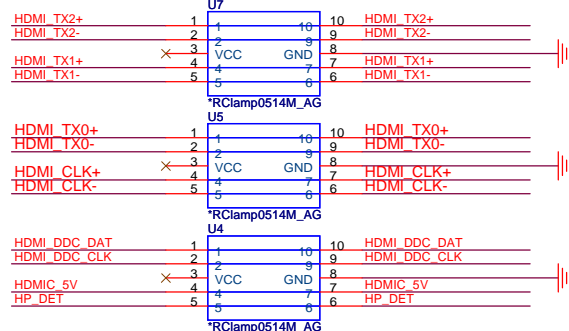
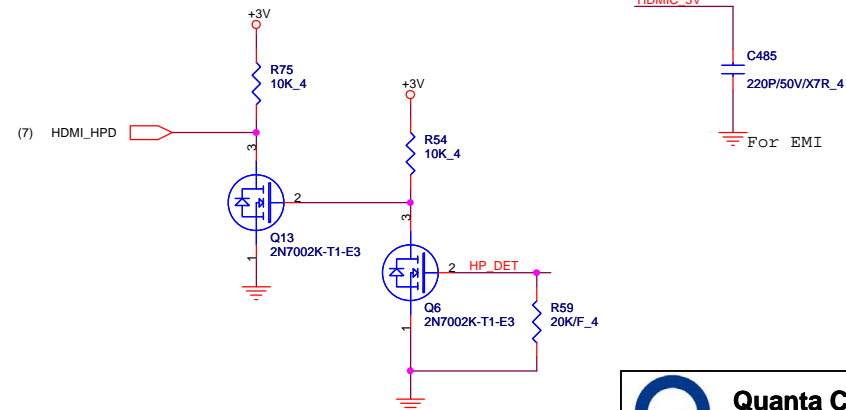
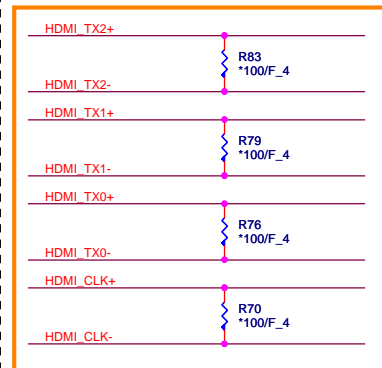
(7,11,15,18,19,24,26,29,37) +5V



EC-DV-01



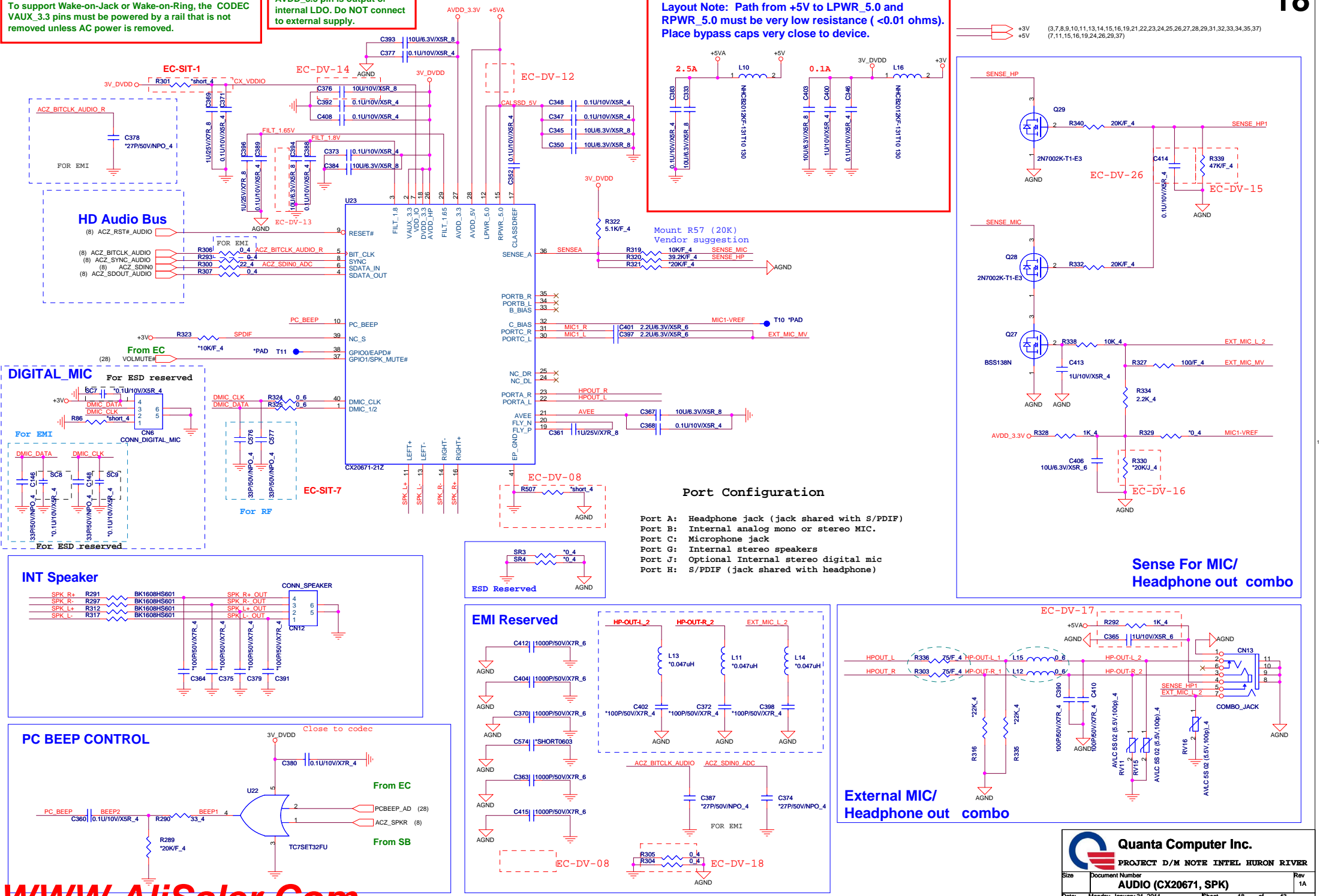
EMI reserve for HDMI

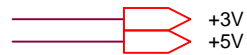


Note:
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

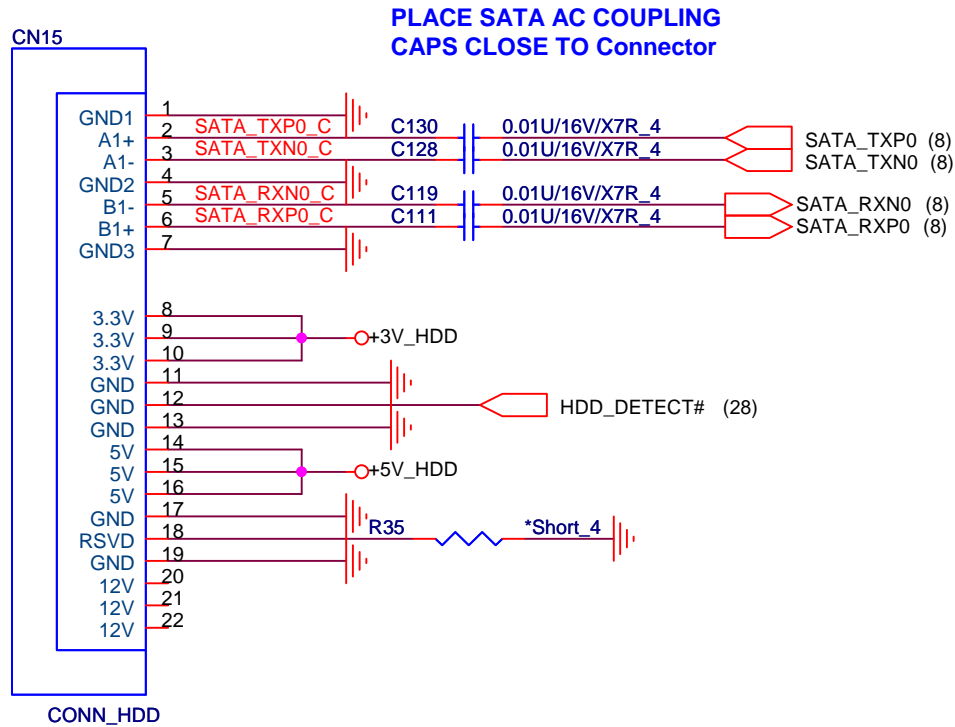
AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.

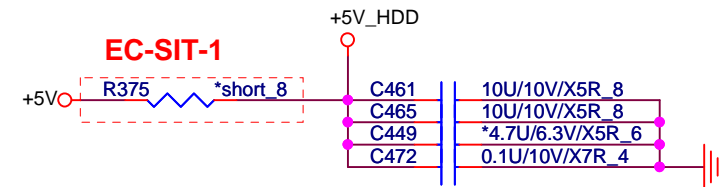




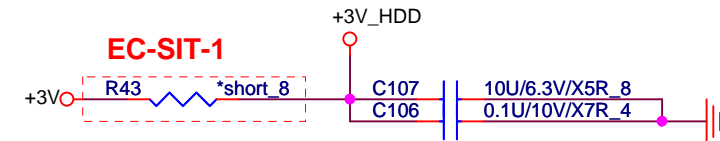
(3,7,8,9,10,11,13,14,15,16,18,21,22,23,24,25,26,27,28,29,31,32,33,34,35,37)
(7,11,15,16,18,24,26,29,37)



DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



Quanta Computer Inc.

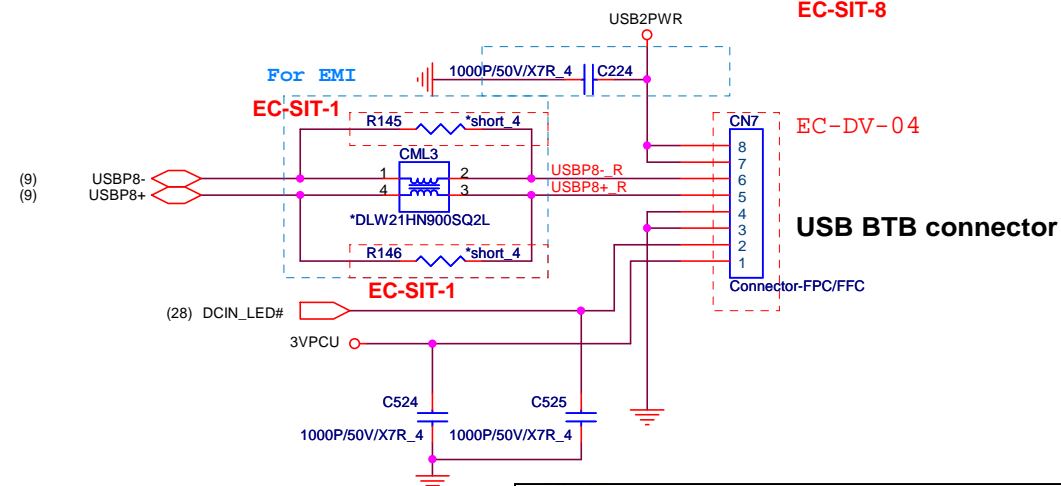
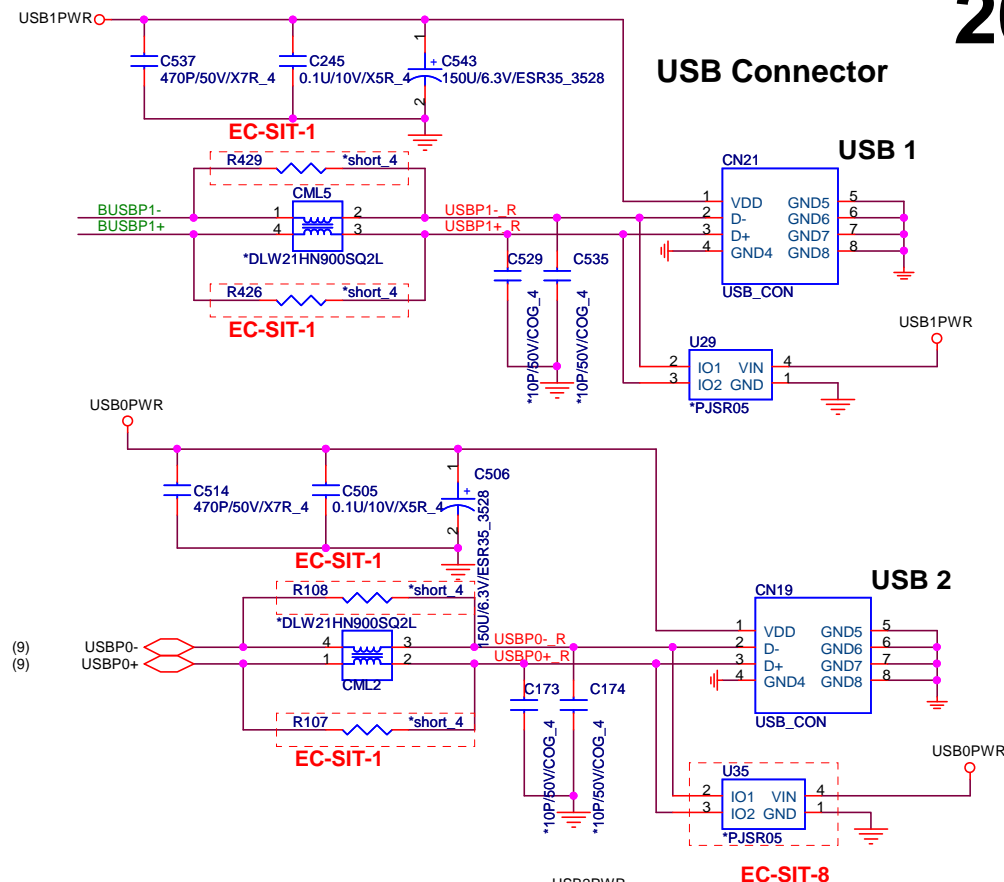
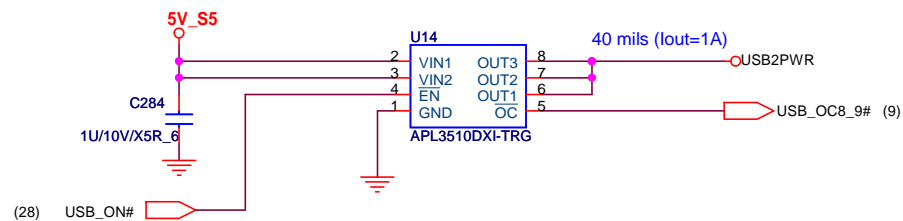
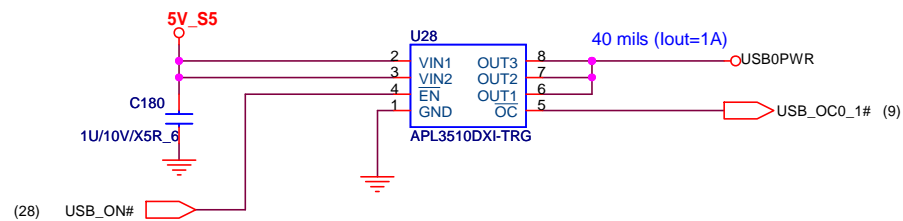
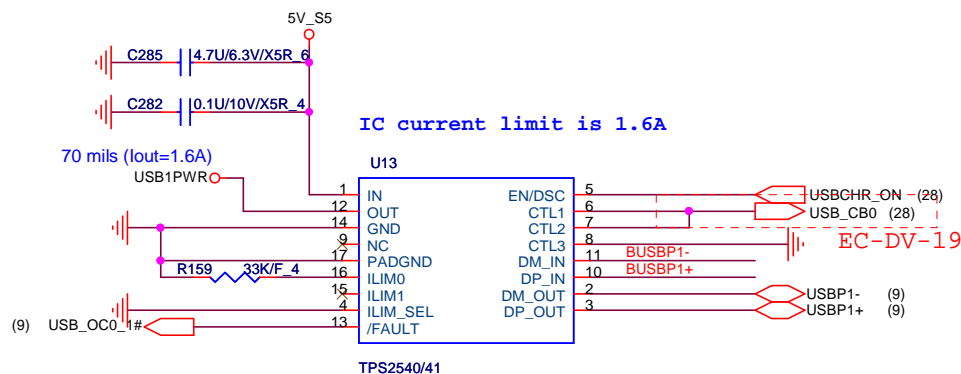
PROJECT D/M NOTE INTEL HURON RIVER

Size	Document Number	Rev
	SATA	1A
Date:	Monday, January 31, 2011	Sheet 19 of 43

TPS2541 table

CTL1	CTL2	CTL3	Mode
0	0	X	Dedicated Charging Port, Auto-detect
0	1	X	Dedicated Charging Port, BC Specification 1.1 Only
1	0	X	Dedicated Charging Port, Apple Only
1	1	0	Standard Downstream Port, USB 2.0 Mode
1	1	1	Charging Downstream Port, BC Specification 1.1

Table 3 – TPS2541 Control Truth Table



5V_S5 (11,37)
3VPCU (8,15,16,17,27,28,29,31,33,36,37)



Quanta Computer Inc.

PROJECT D/M NOTE INTEL HURON RIVER

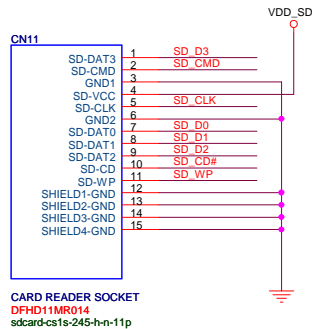
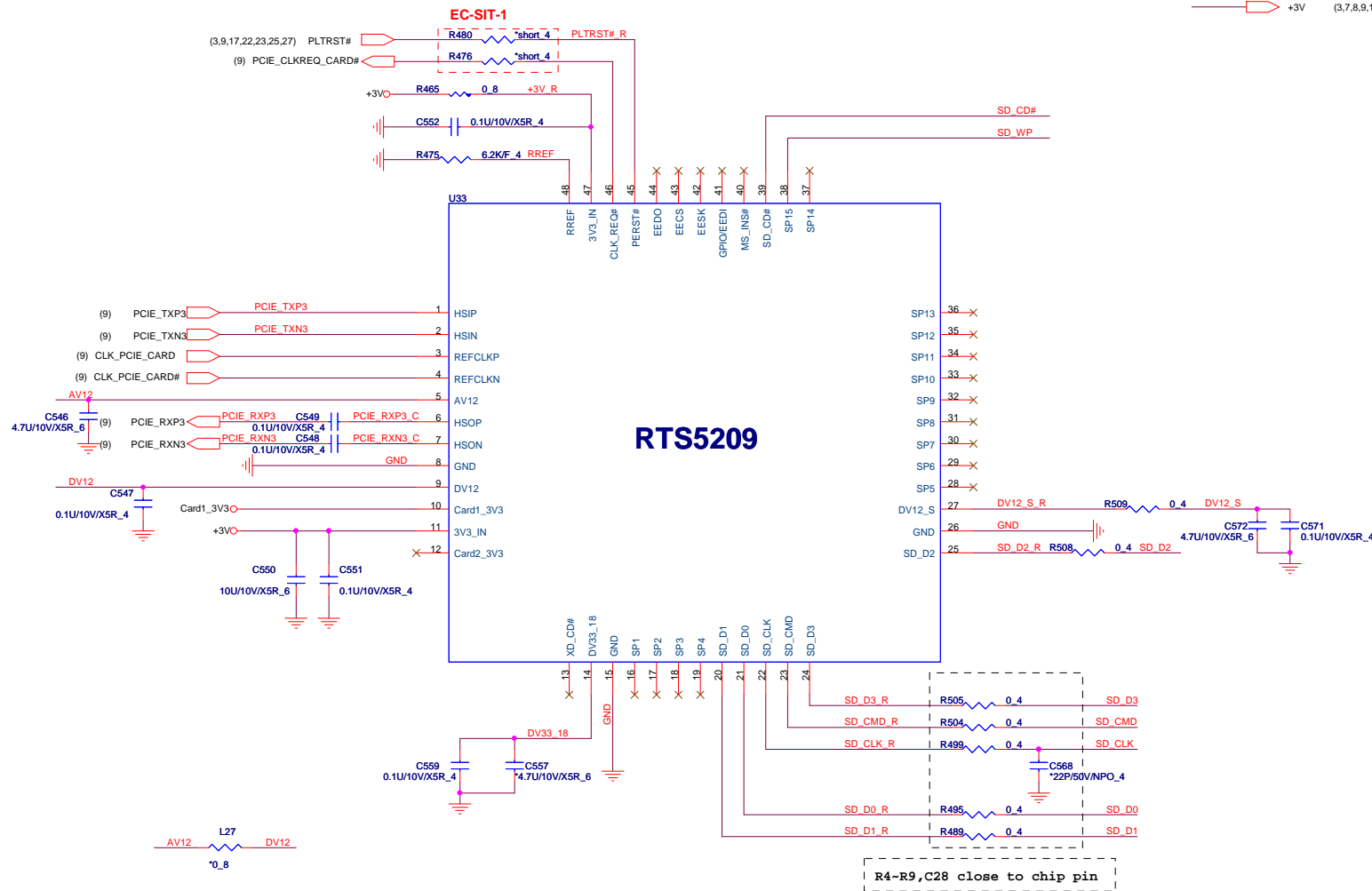
Size	Document Number	Rev
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	USB x 3	1A
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Date:	Monday, January 24, 2011	Sheet	20	of	42
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Note:

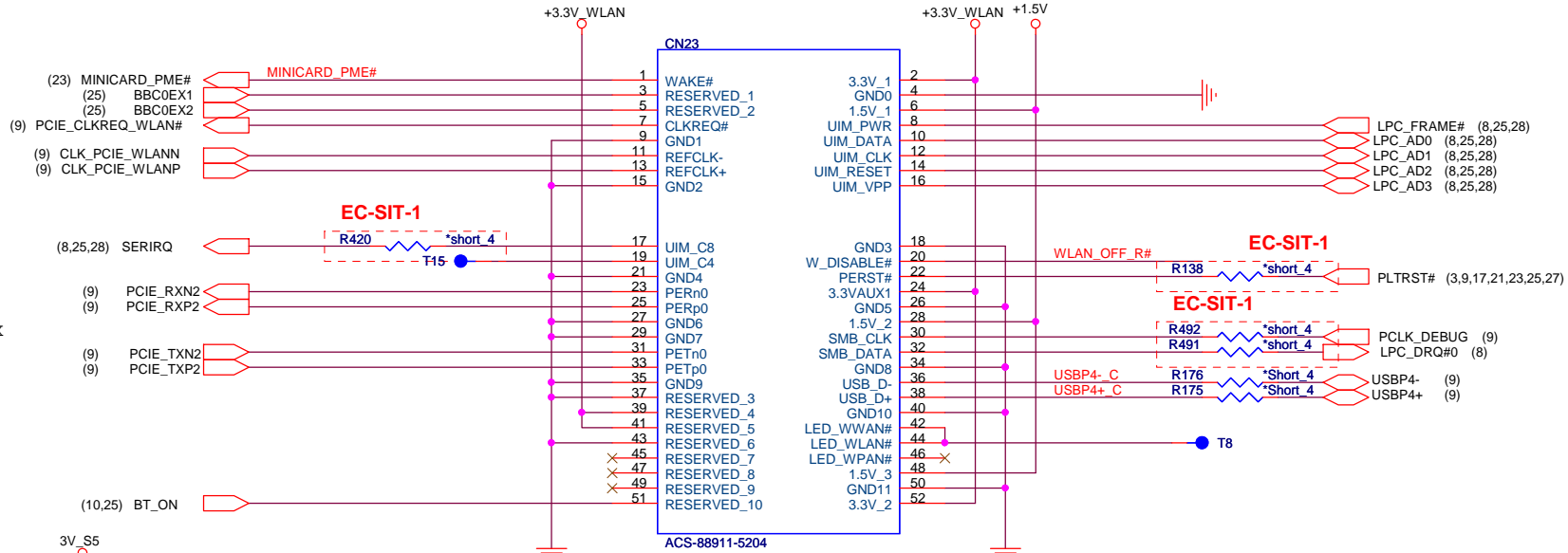
SD/MMC	MS
SP1	SD D7
SP2	SD D6
SP3	SD D5
SP4	SD D4
SP5	MS BS
SP6	
SP7	MS D1
SP8	
SP9	MS D0
SP10	MS D2
SP11	
SP12	MS D3
SP13	
SP14	MS CLK
SP15	SD_WP



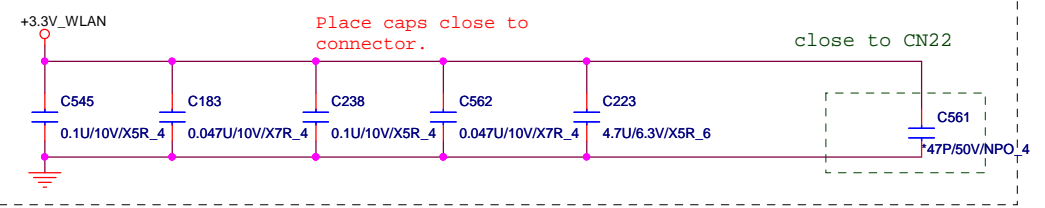
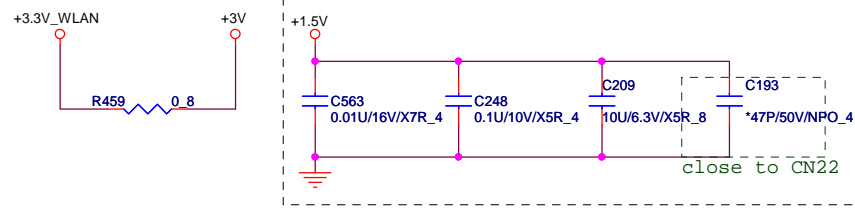
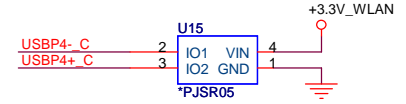
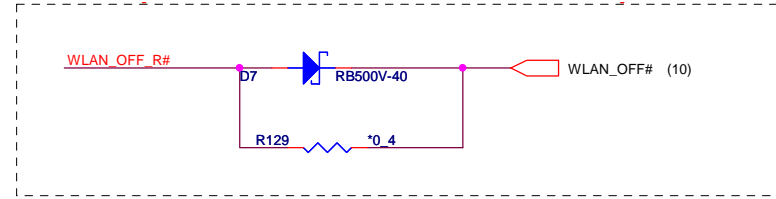
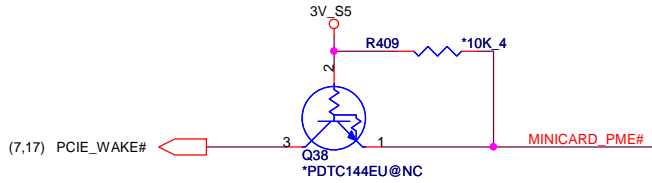
MiniCard WLAN connector

+3V	(3,7,8,9,10,11,13,14,15,16,18,19,21,23,24,25,26,27,28,29,31,32,33,34,35,37)
+1.5V	(11,23,32)
3V_S5	(3,7,8,9,10,11,25,28,37)

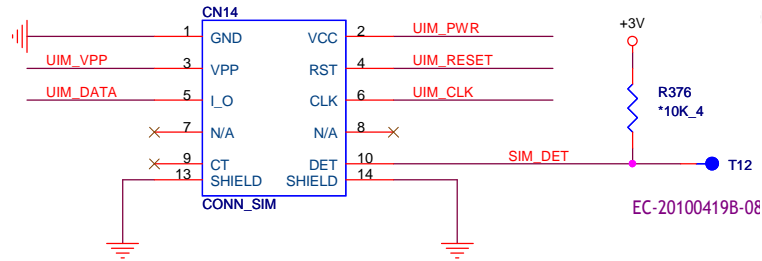
22



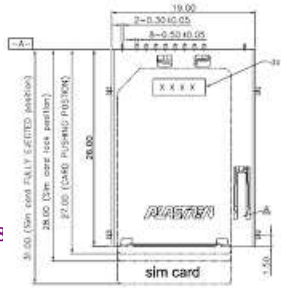
PCI-Express TX and RX direct to connector



SIM Card CONN

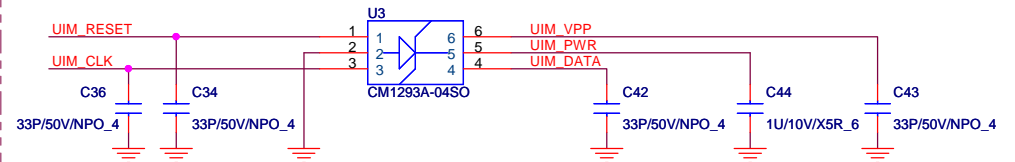


Layout Note:
UIM_RESET, UIM_CLK, UIM_DATA routing as short as possible

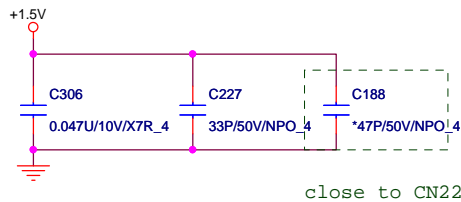
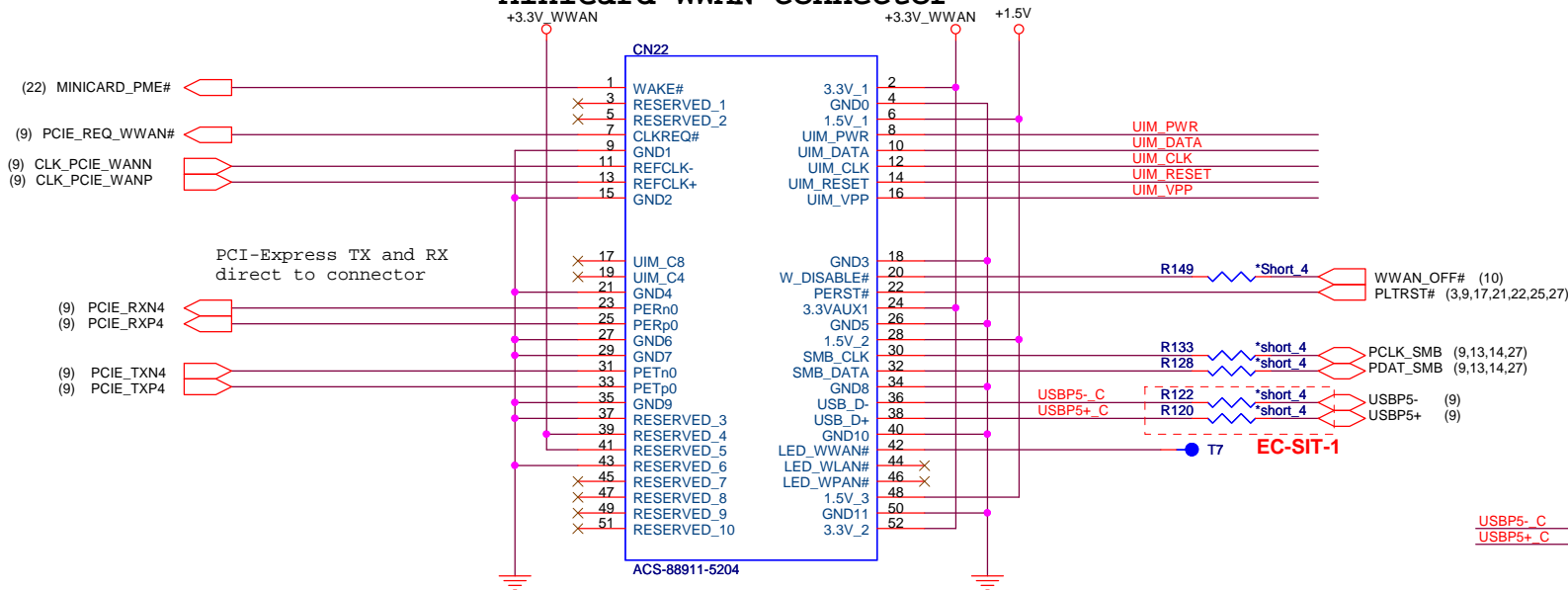


+3V (3,7,8,9,10,11,13,14,15,16,18,19,21,22,24,25,26,27,28,29,31,32,33,34,35,37)
+1.5V (11,22,32)

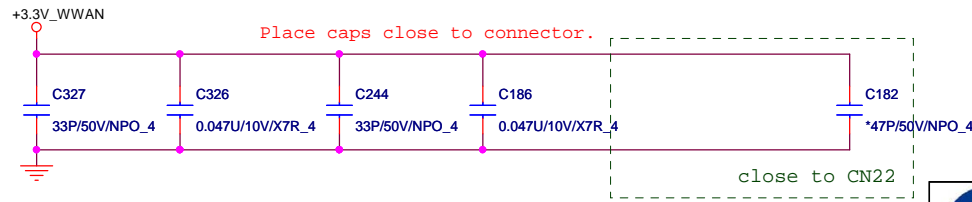
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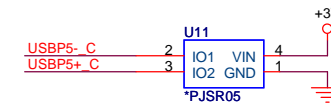
MiniCard WWAN connector



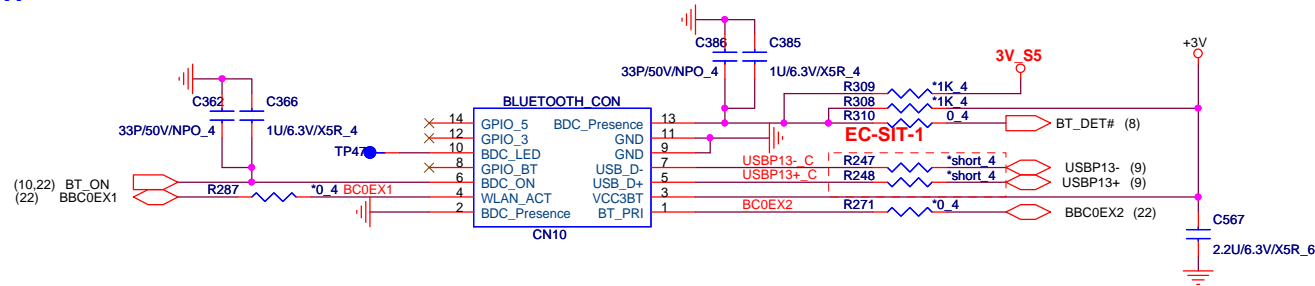
close to CN22



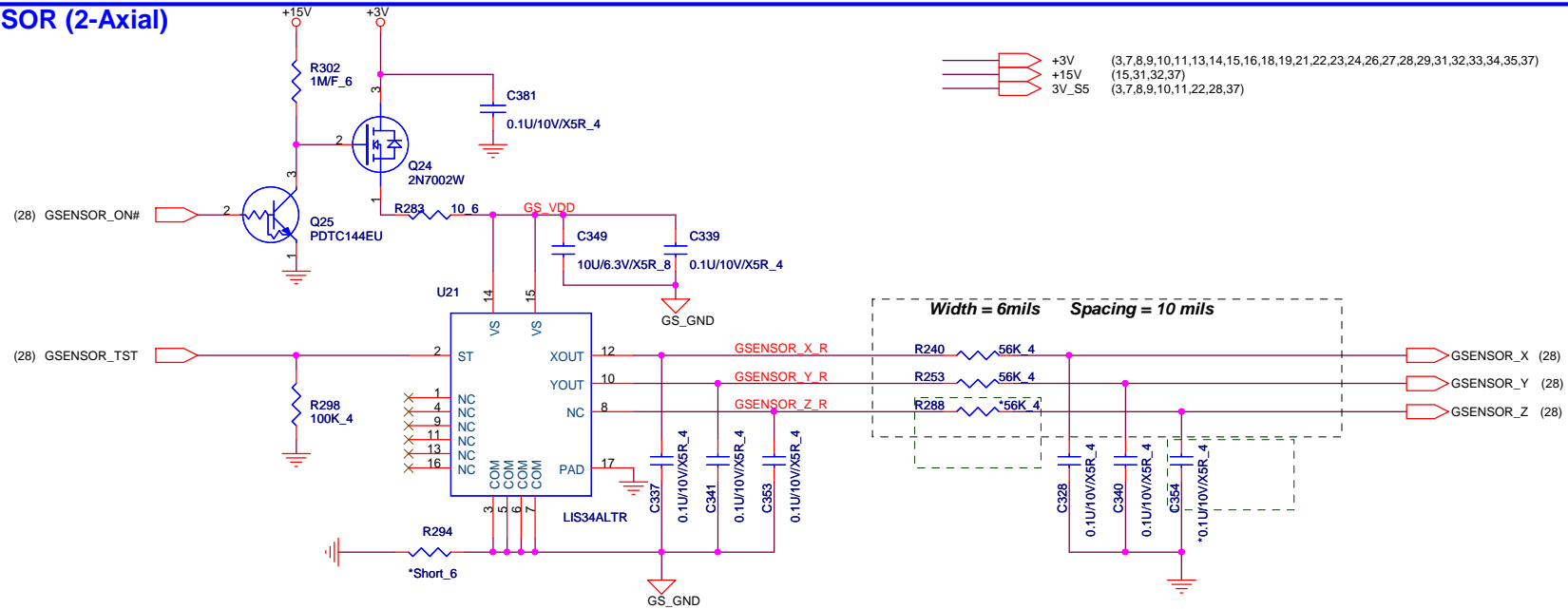
close to CN22



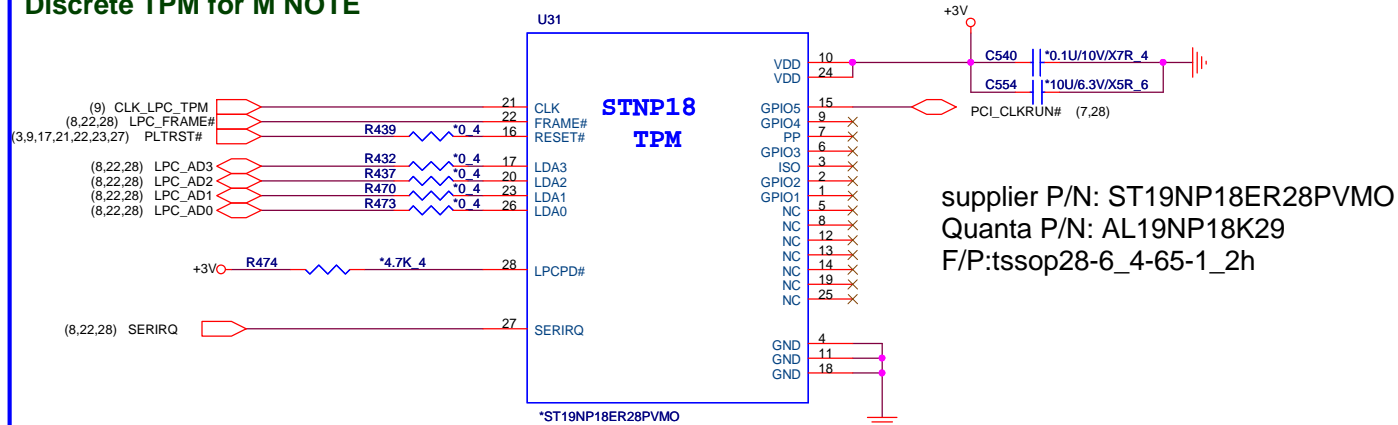
BLUETOOTH



G-SENSOR (2-Axial)



Discrete TPM for M NOTE



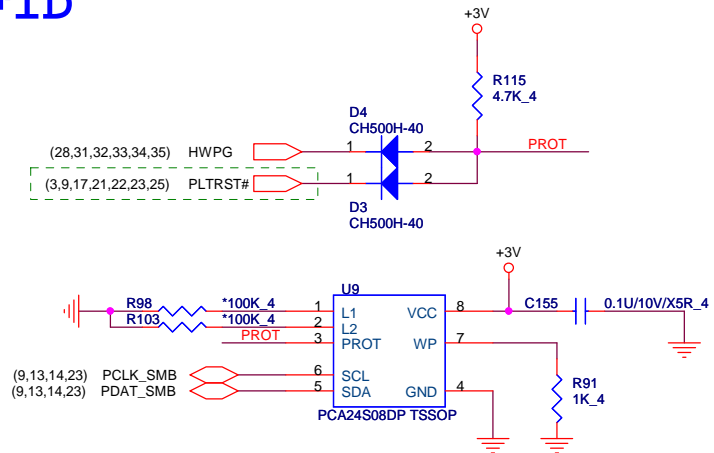
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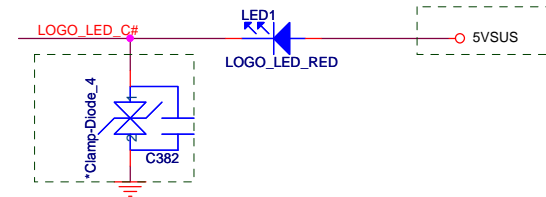
for Charger

1	0	0	1	A2	A1	A0	0
MSB				LSB			

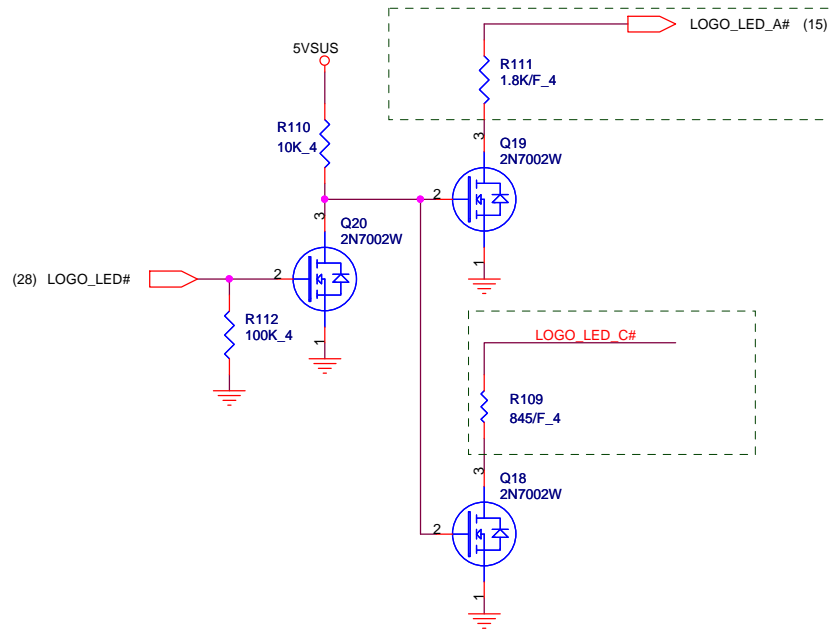
RFID



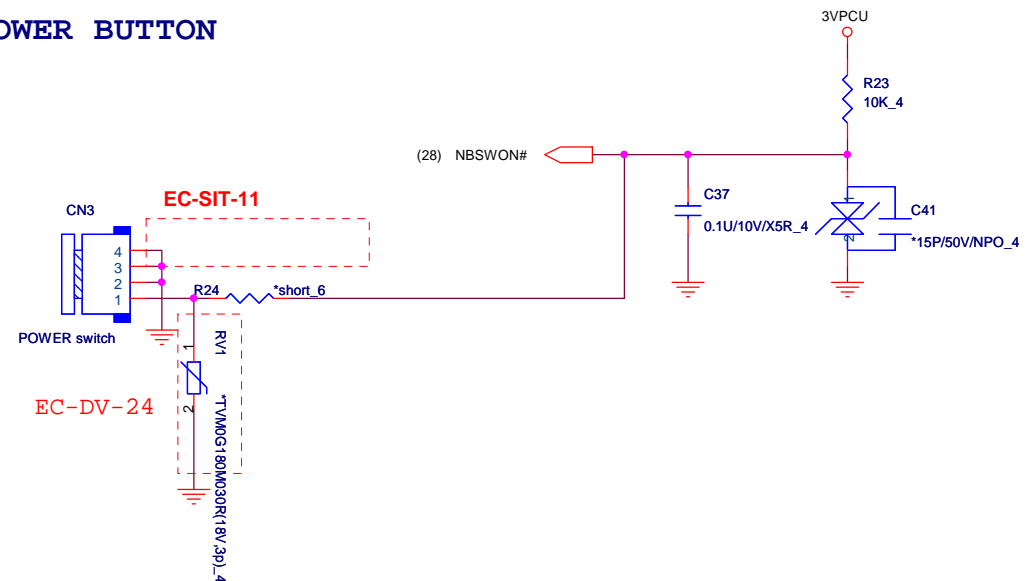
EC-SIT-10



LED Driver

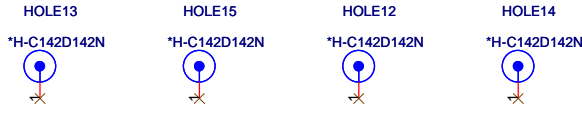


POWER BUTTON

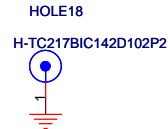




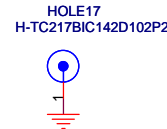
Hole for CPU support



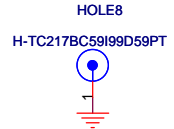
MiniCard WWAN



MiniCard WLAN



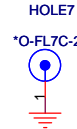
BLUETOOTH



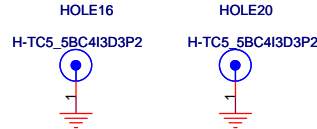
CRT



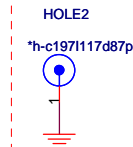
Keyboard



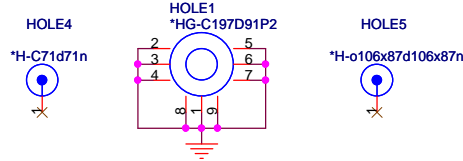
SB



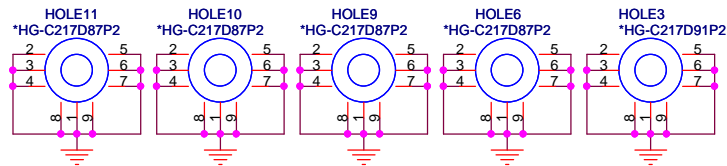
EC-DV-03



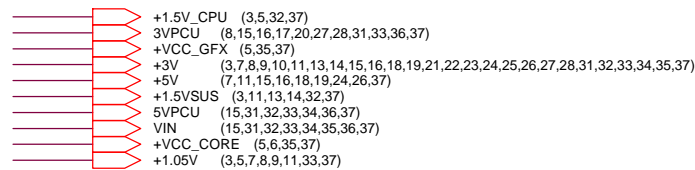
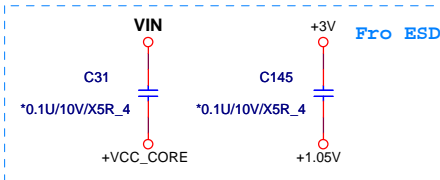
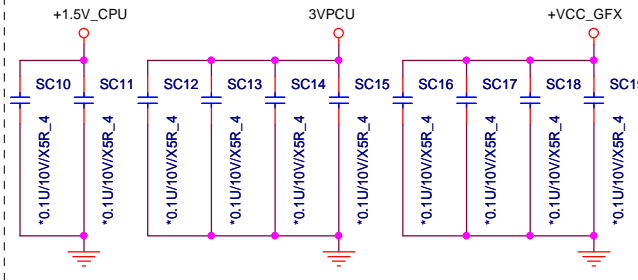
Boundary Hole



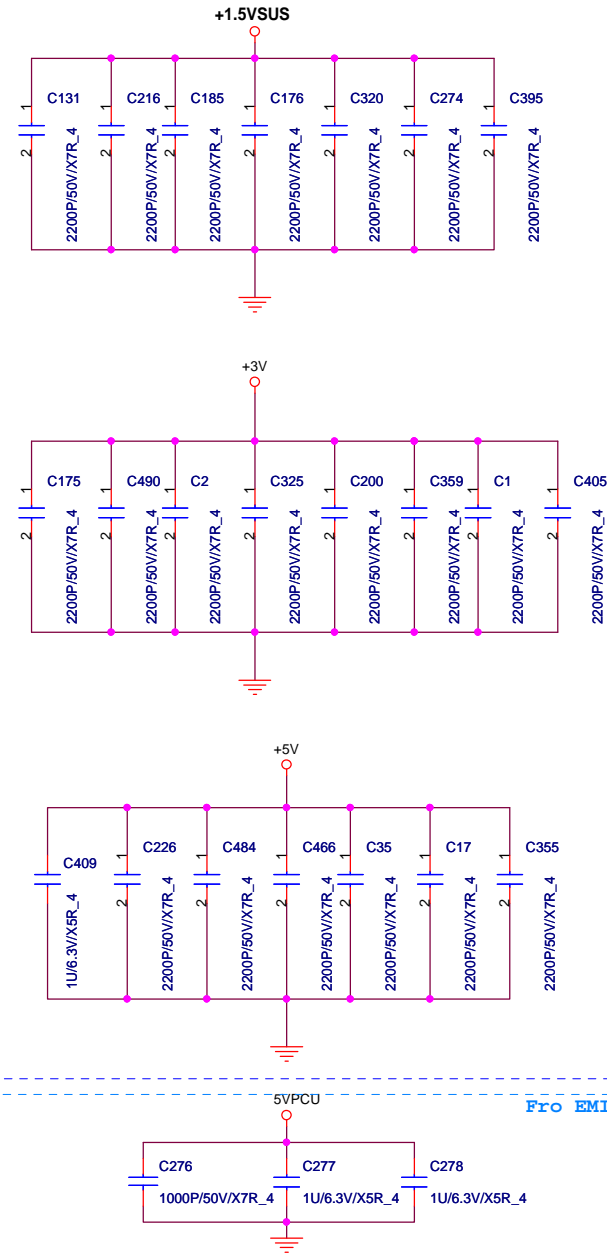
Boundary Hole

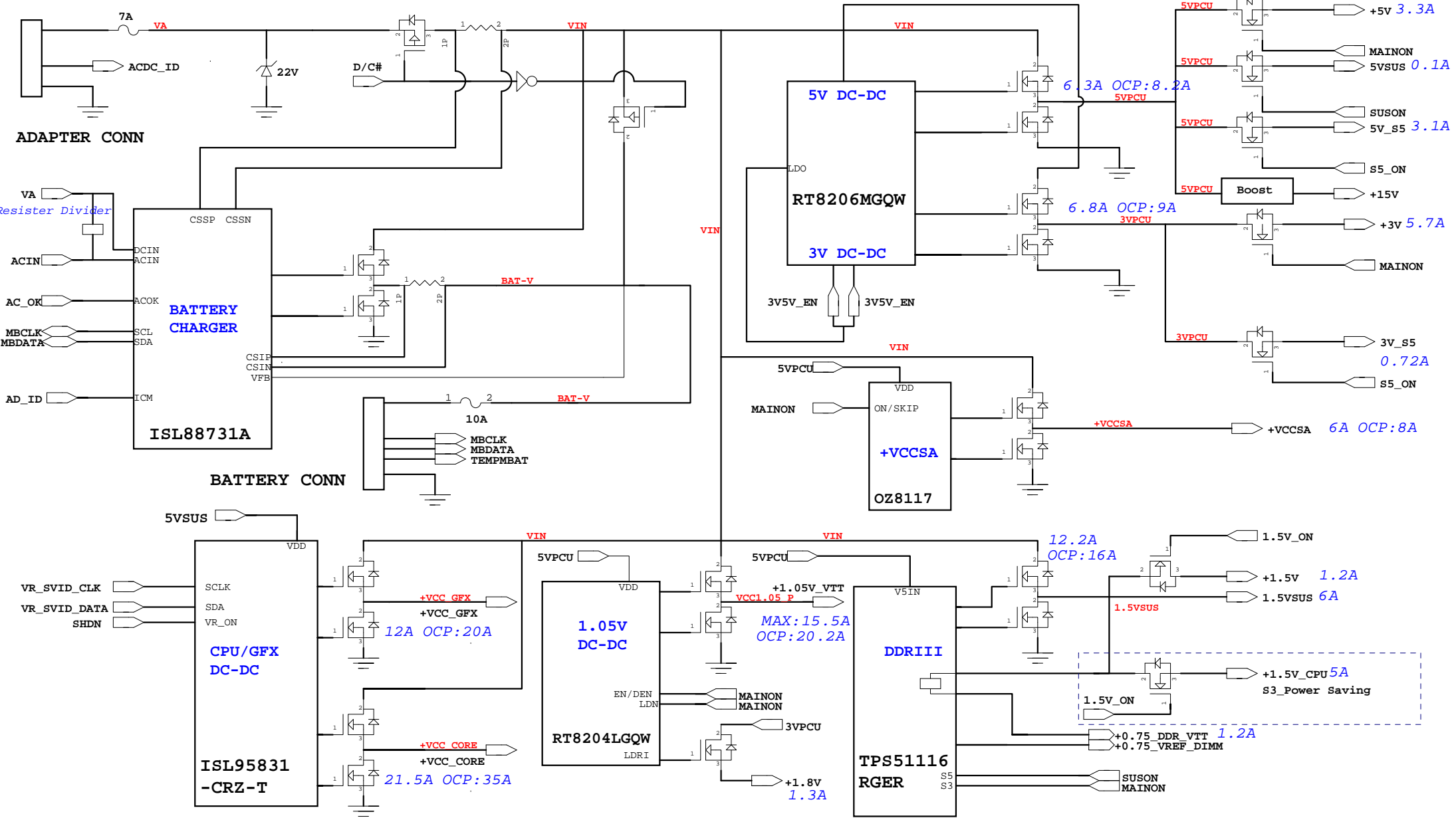


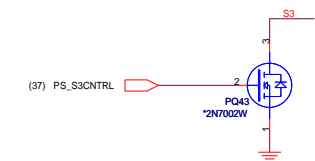
Fro ESD

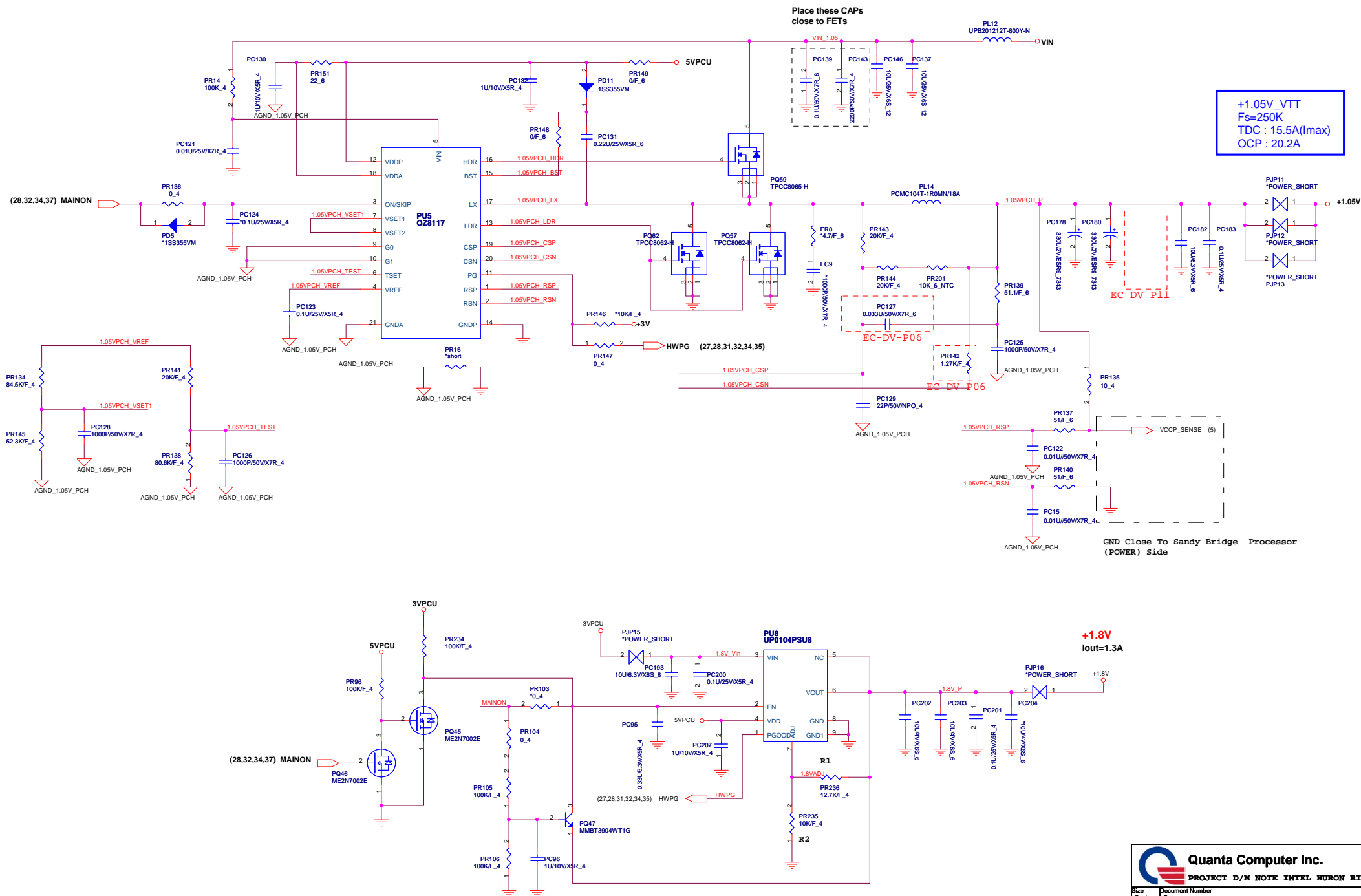


EMI

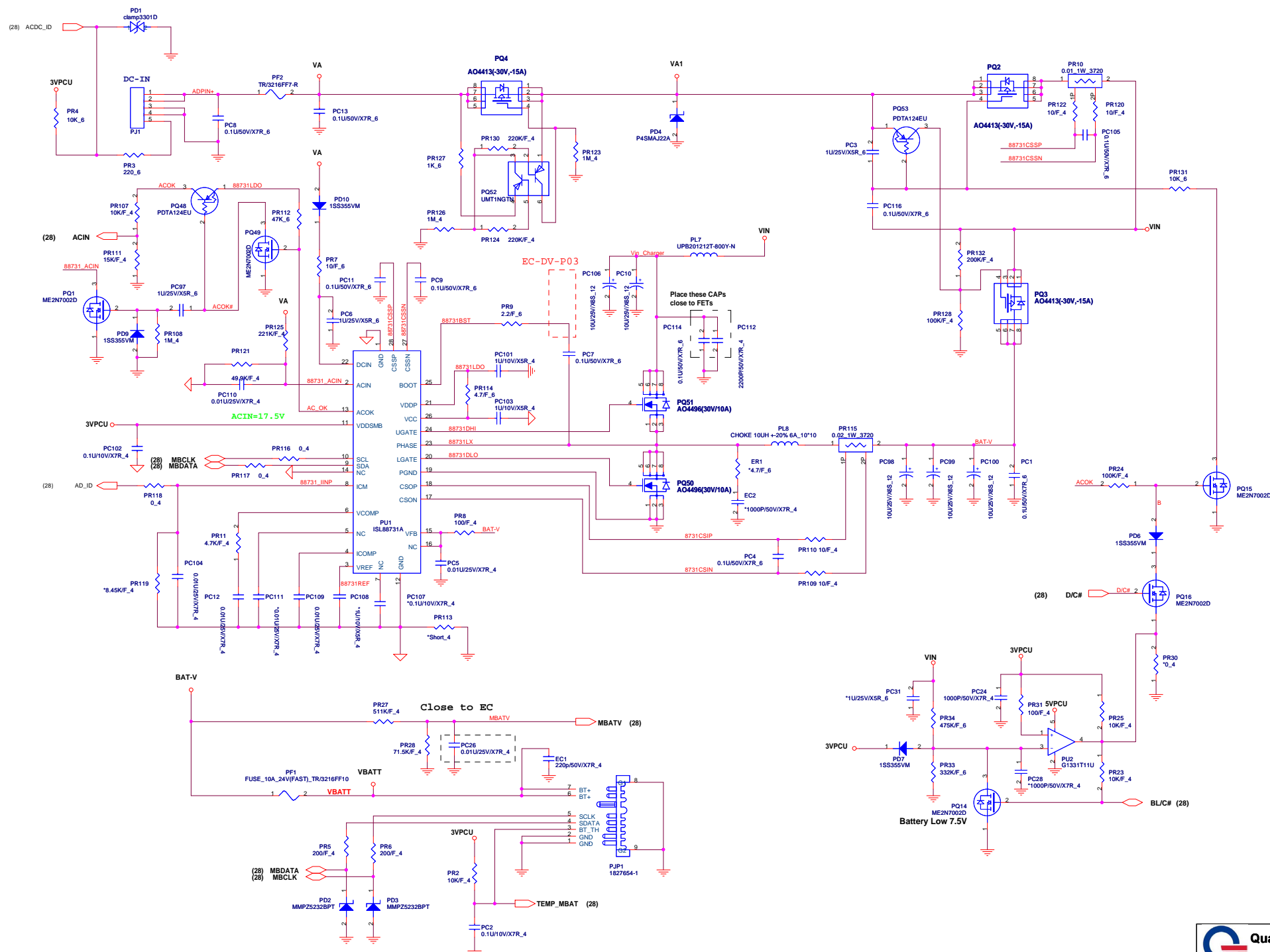




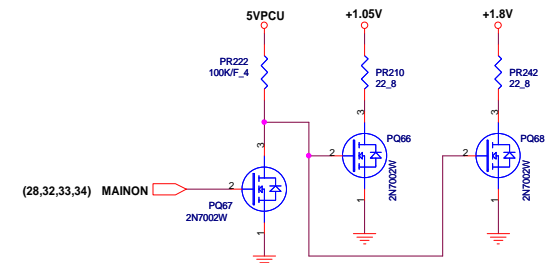
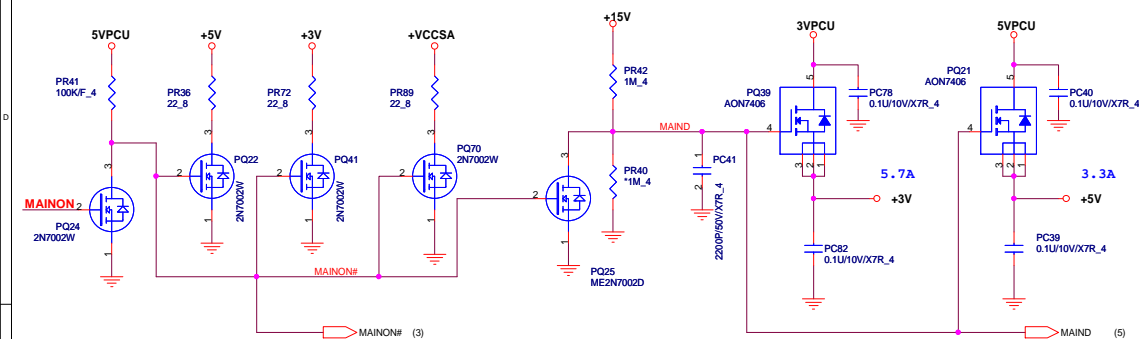




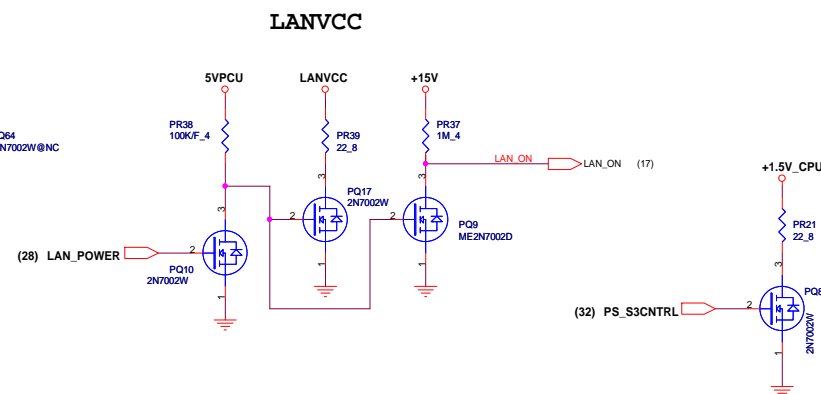
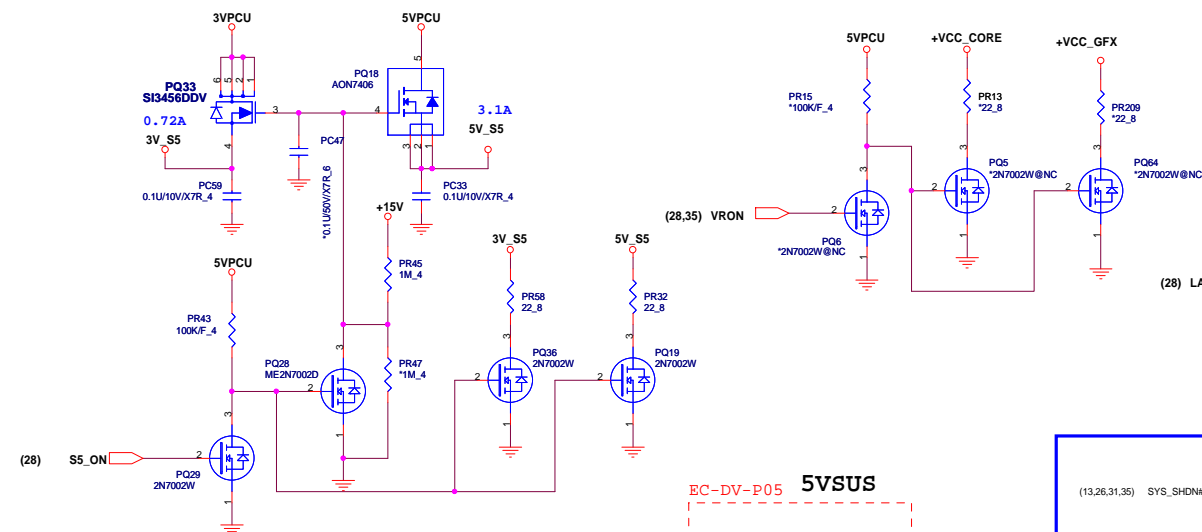




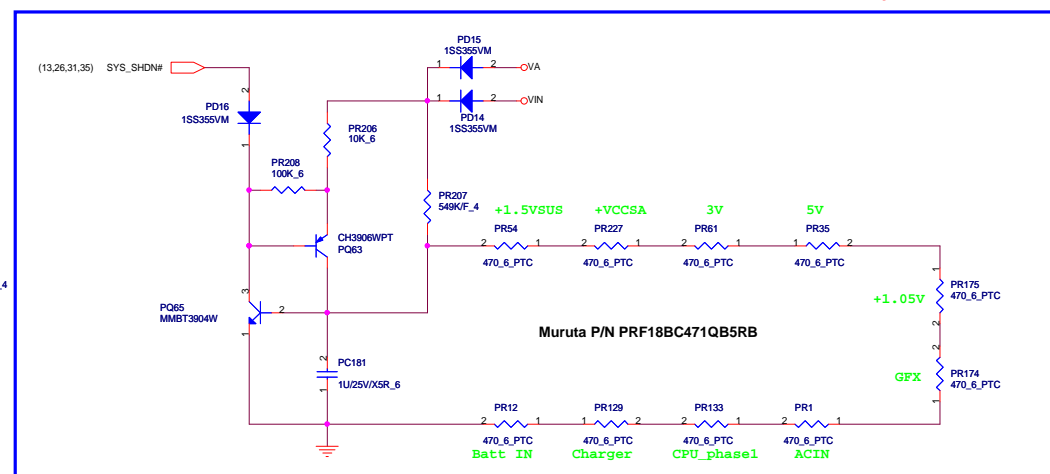
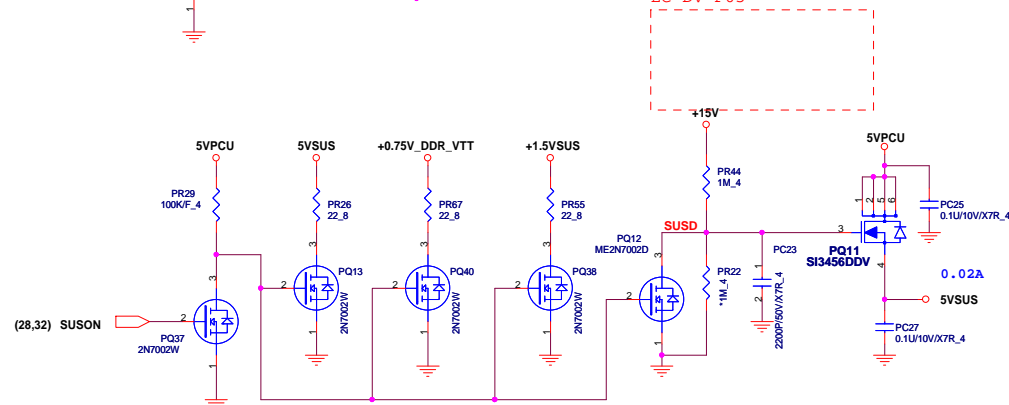
+3.3V, +5V

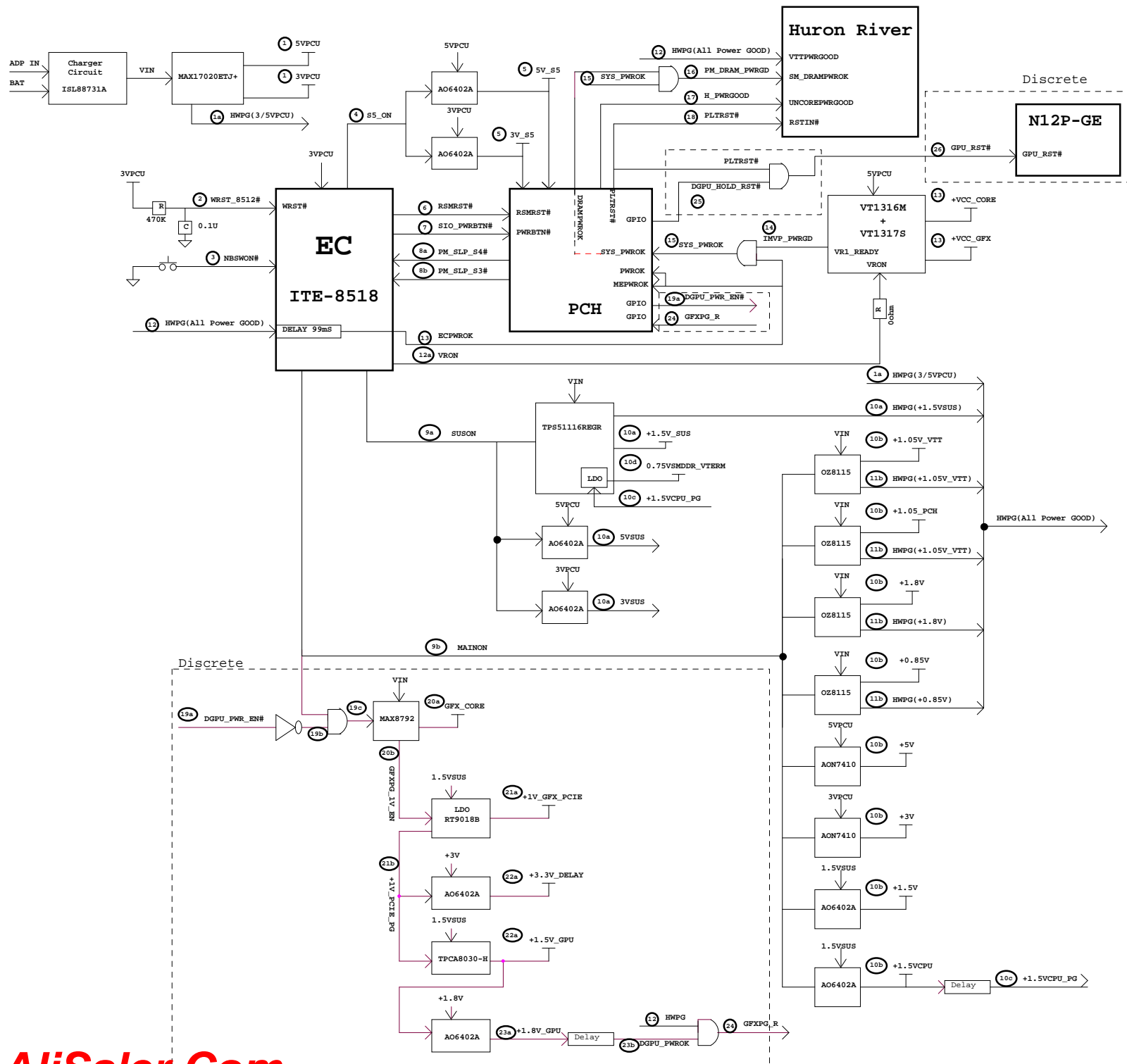


3V_S5, 5V_S5



5VSUS





[illegible]

Revision History

Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
A1A		DV	Initial release	2010/12/03	2010/12/03

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP

CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

DM NOTE Schematic EC Tracking Record DV (for DV)XXXX. XX, 2010				
EC #	Page	Date	Part Affected	Description
EC-DV-01	16	2010/11/17	U2000 and related schematic	Remove level shift and related schematic
EC-DV-02	05	2010/11/17	R11256	Follow Intel power delivery to add 10m ohm pull-up at VDDCQ
EC-DV-03	29	2010/11/17	HOLE10	Change HOLE10 footprint
EC-DV-04	20	2010/11/17	CN23	Change USB BTB connector to FFC type
EC-DV-05	17	2010/11/17	C11242	Change C11242 from 10P to 1000P and series with ESD part for ISN
EC-DV-06	28	2010/11/18	EC Pin#98, R11264, R11265	G-sensor ID select
EC-DV-07	17	2010/11/18	RV19	Change RV19 pop for ESD solution
EC-DV-08	18	2010/11/19	R916, R11216, R11266	Delete R916 and R11216, because AGND connect with DGND in GND layer
EC-DV-09	07	2010/11/22	RV8	Reserse for ESD
EC-DV-10	17	2010/11/22	RV17, RV18, C11243, C11246	Reserse for ESD
EC-DV-11	17	2010/11/22	U11005, U11006	Pin#5 connect LANVCC for ESD's request
EC-DV-12	18	2010/11/22	R281	reference CX20371-21Z CRB schematic to delete it
EC-DV-13	18	2010/11/22	R330	reference CX20371-21Z CRB schematic to delete it
EC-DV-14	18	2010/11/22	C11247	reference CX20371-21Z CRB schematic to add it
EC-DV-15	18	2010/11/22	R1283, C7373	reference Conexant combo jack latest CRB schematic to delete C7373 and change R1283 to 4.7K
EC-DV-16	18	2010/11/22	R11269	reference Conexant combo jack latest CRB schematic to add it
EC-DV-17	18	2010/11/22	R1290, C11248	reference Conexant combo jack latest CRB schematic to add C11248 and change R1290 to 200
EC-DV-18	18	2010/11/22	R11267, R11268	EMI request
EC-DV-19	20, 28	2010/11/23	U47.6, U47.7, U15.79	EC can combine USB charger IC CB[0:1] pin to one signal CB[0]
EC-DV-20	24	2010/11/23	R209, R201	Change to 4.7K
EC-DV-21	24	2010/11/22	RV9, RV10	Reserse for ESD
EC-DV-22	24	2010/11/22	RV11, RV12	Reserse for ESD
EC-DV-23	27	2010/11/22	RV13, RV14, RV15	Reserse for ESD
EC-DV-24	27	2010/11/22	RV16	Reserse for ESD
EC-DV-25	24	2010/11/29	CN9	CN9 PIN8 connect to EC
EC-DV-26	27	2010/11/29	C12000	Add C12000 for Audio vendor suggestion

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 Quanta Computer Inc. PROJECT D/M NOTE INTEL HURON RIVER		
Size	Document Number	Rev
	EC Tracking Record SIT	1A
Date:	Monday, January 31, 2011	Sheet 43 of 43