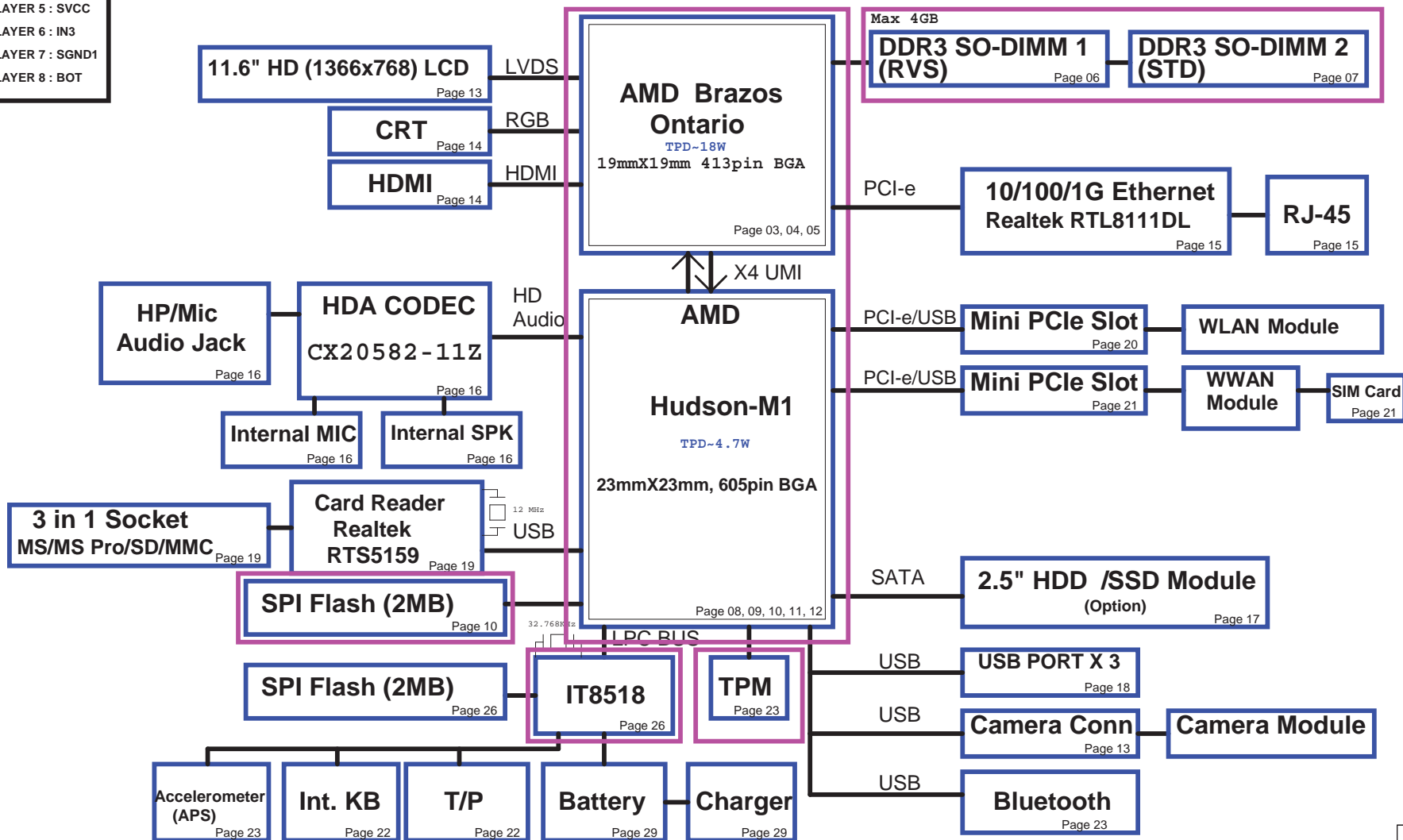


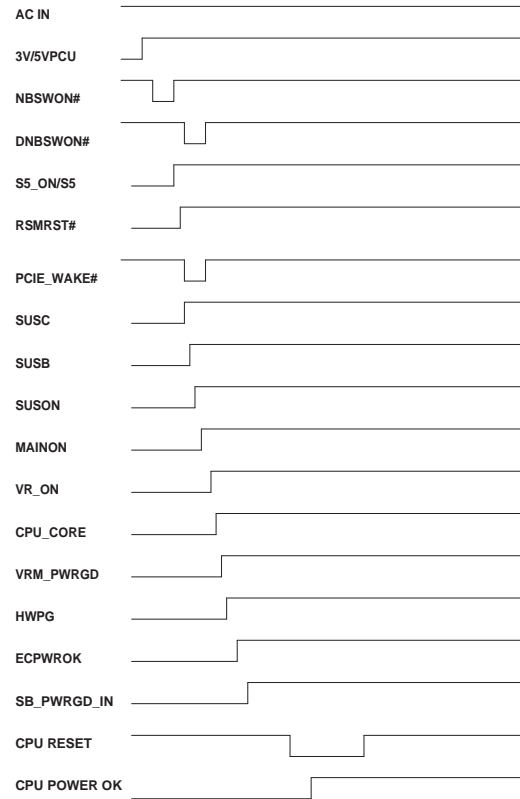
LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : IN3
LAYER 7 : SGND1
LAYER 8 : BOT



POWER

DC/DC 3V_PCU, 5V_PCU, +15V	Page 30
REGULATOR (DDR3) 1.5V_SUS, 0.75V_DDR_VTT	Page 31
REGULATOR +1V	Page 32
REGULATOR 1.1V_S5, +1.1V	Page 33
REGULATOR +1.8V	Page 34
CPU Core	Page 35
RUN POWER SW 3V_SUS, 5V_SUS, 3V_S5, 5V_S5 +3V, +5V	Page 36
Discharge	Page 36

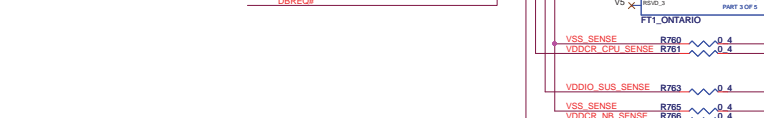
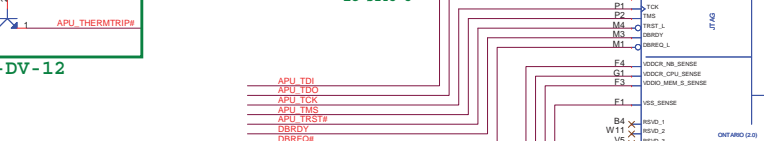
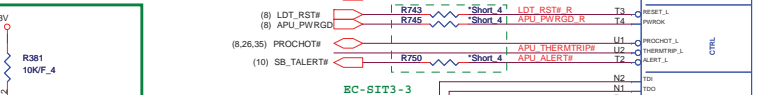
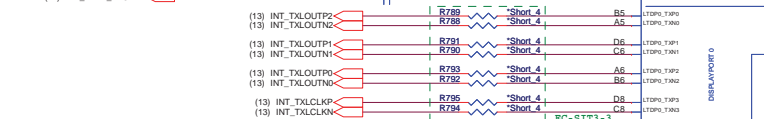
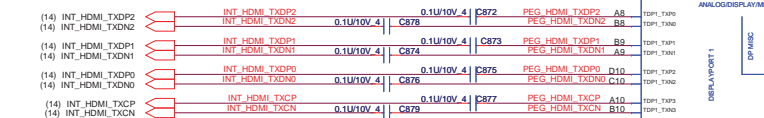
Power Sequence



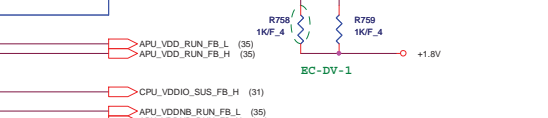
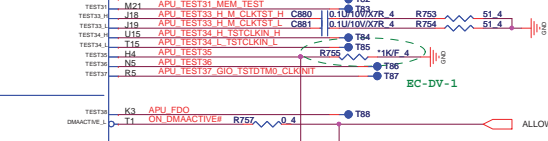
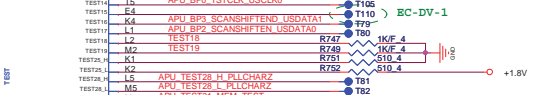
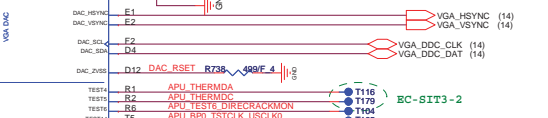
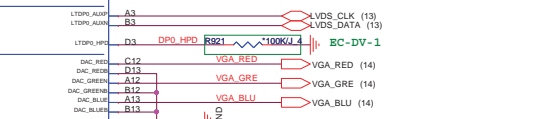
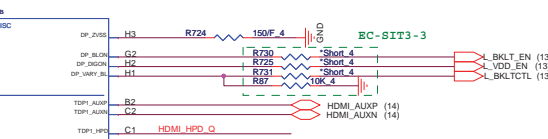
SB820 SMBUS	Pin NO.	SMBUS Function Define
PCLK_SMB PDAT_SMB (+3V)	AD22 AE22	DDR / RFID
SB_SMBCLK1 SB_SMBDATA1 (+3V_S5)	F5 F4	not used
SB_SCLK2 SB_SDATA2 (+3V_S5)	D25 F23	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used
SB_SCLK3 SB_SDATA3 (+3V_S5)	B26 E26	not used

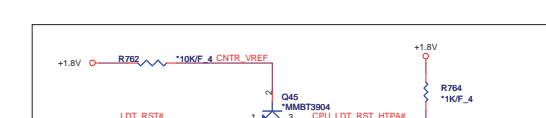
KBC SMBUS	Pin NO.	SMBUS Function Define
MBCLK MBDATA (+3VPCU)	110 111	Battery
MBCLK_THRM MBDATA_THRM (+3VPCU)	115 116	Thermal



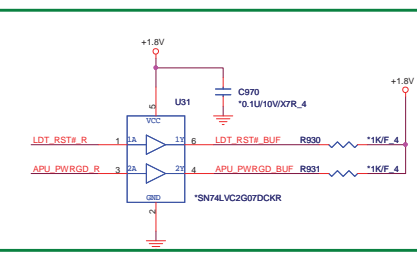
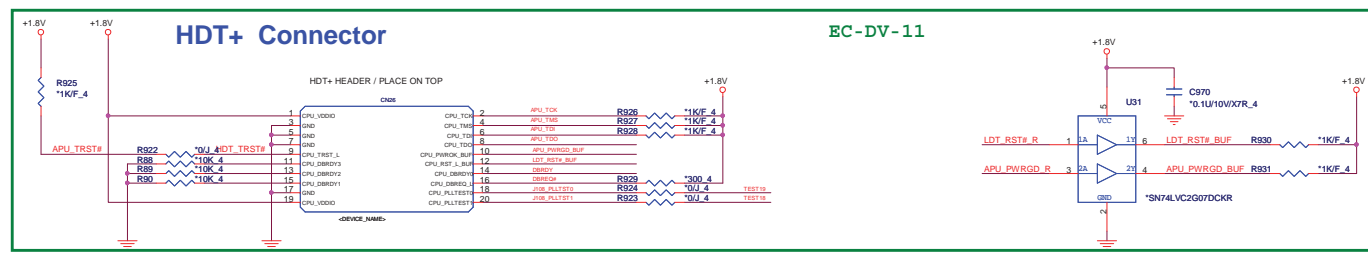
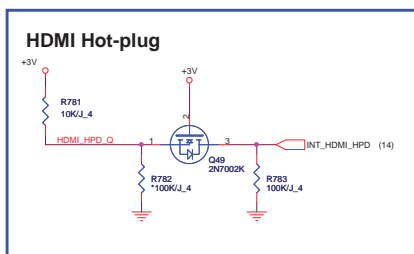
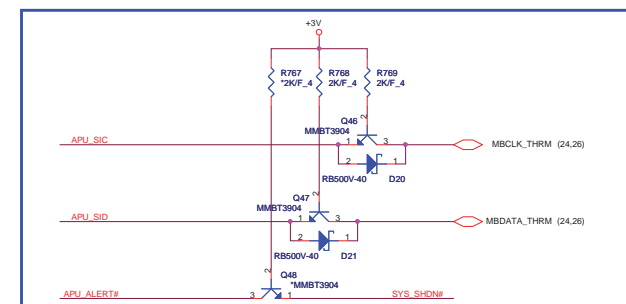
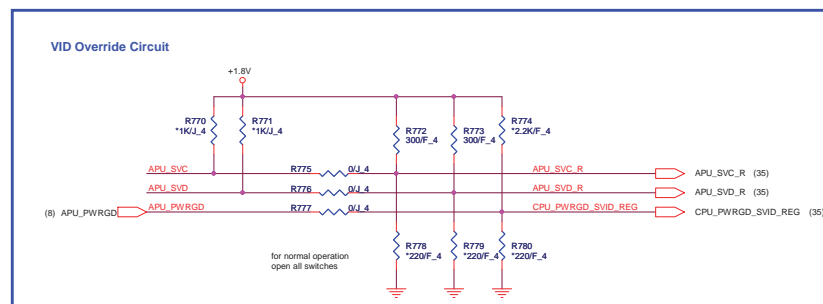


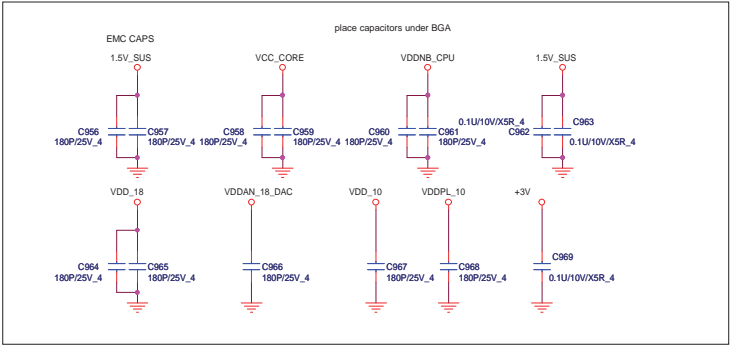
DIFFERENTIAL ROUTING





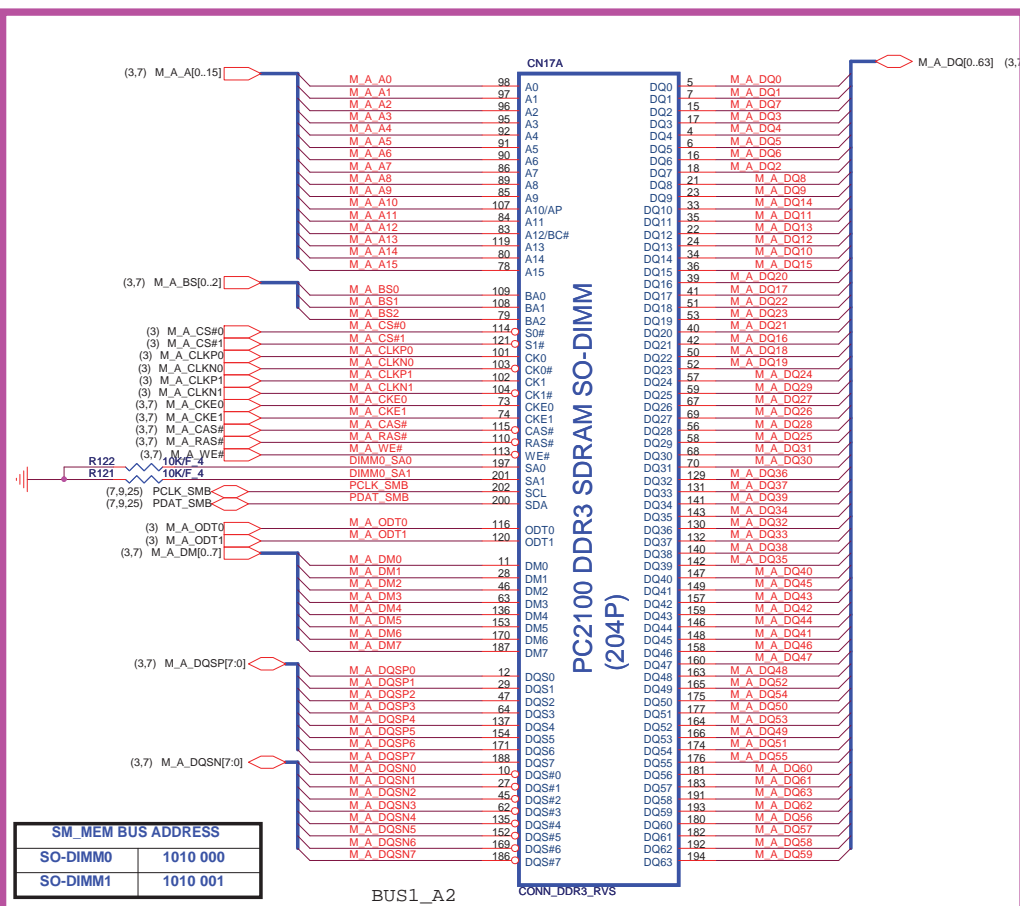
Can remove on MP----->LX



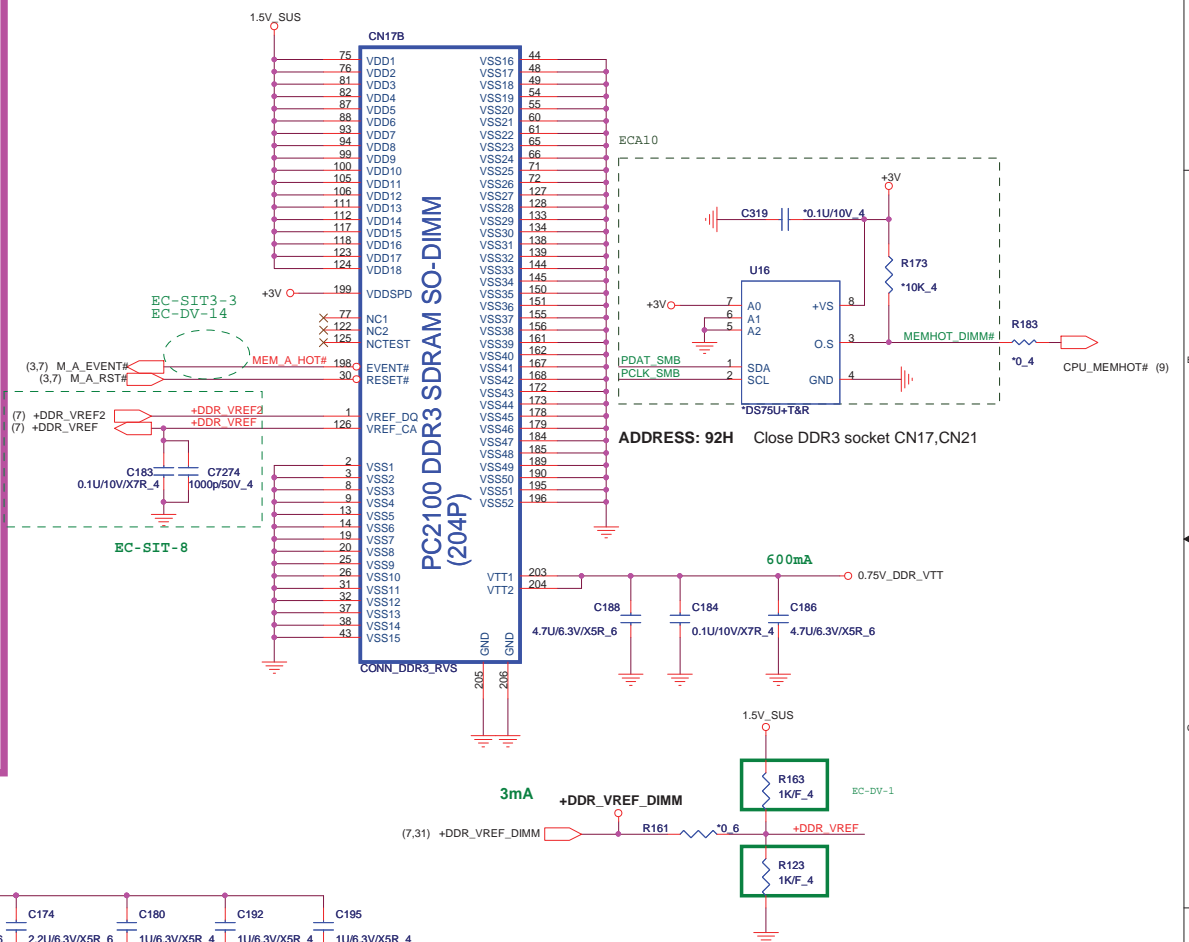
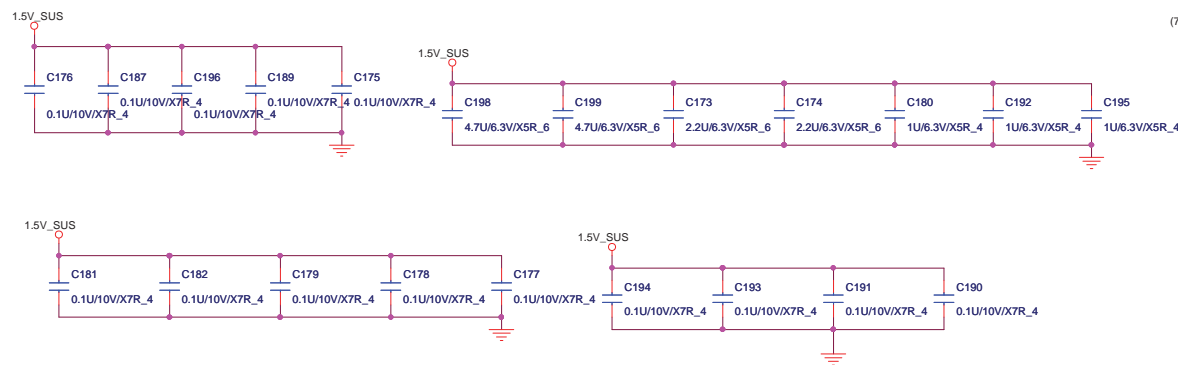


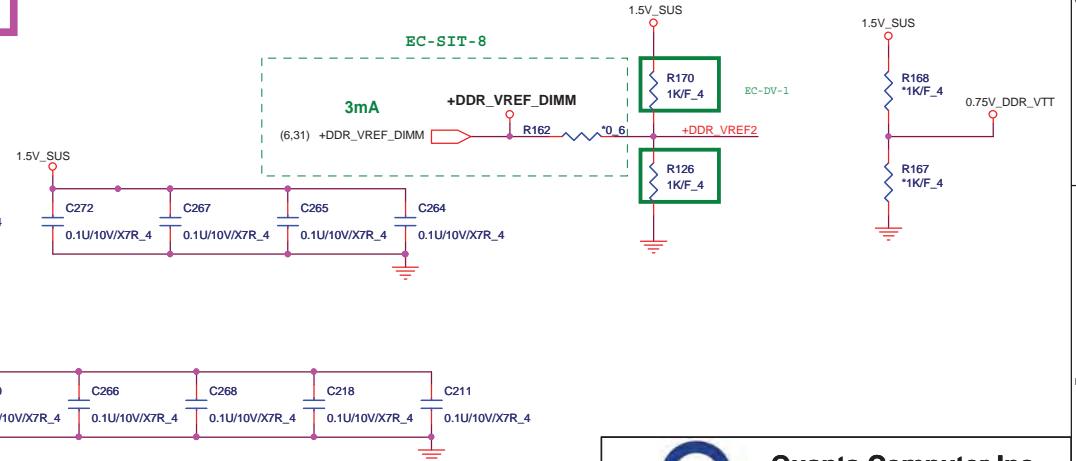
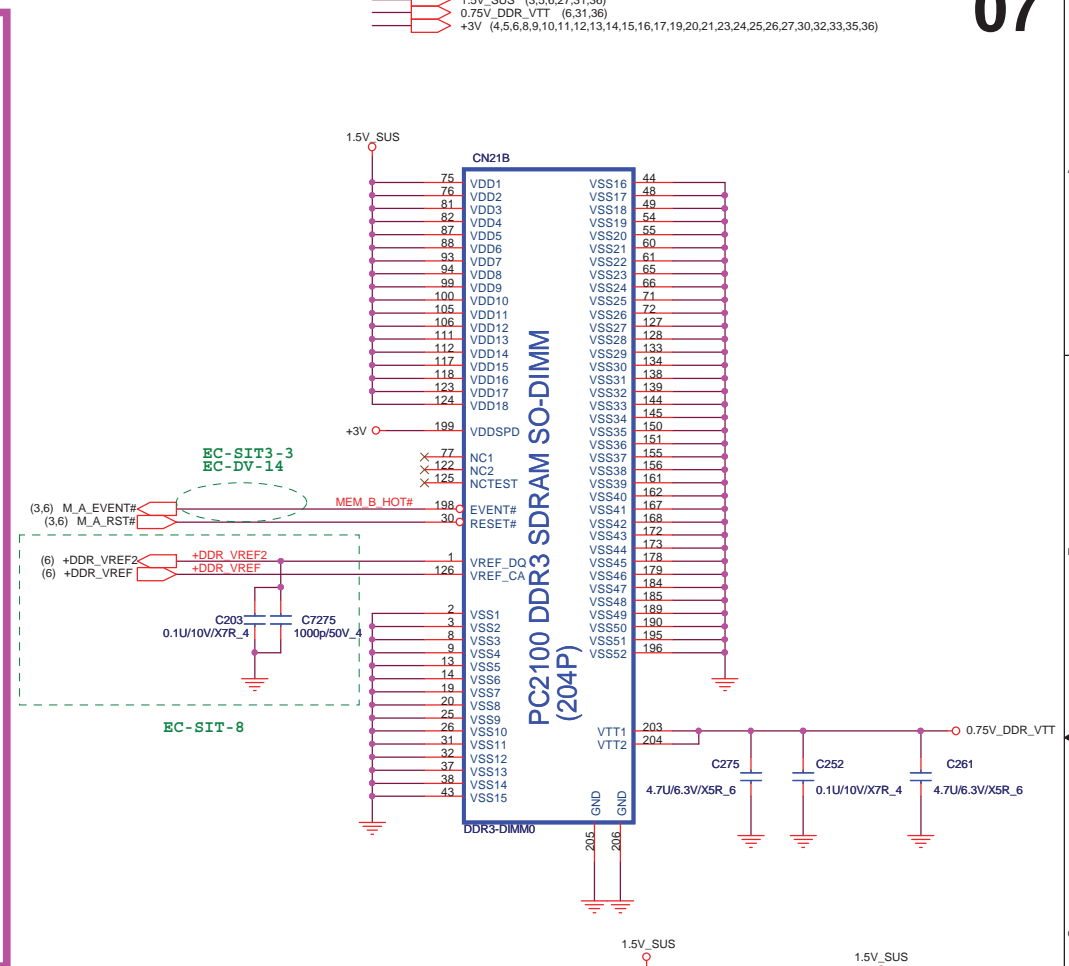
1.5V_SUS (3.5,7,27,31,36)
+DDR_VREF_DIMM (7,31)
0.75V_DDR_VTT (7,31,36)

+3V (4,5,7,8,9,10,11,12,13,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)

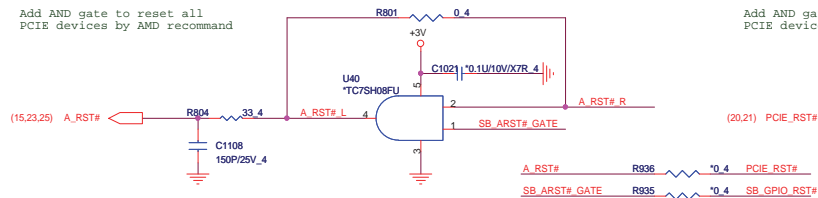


SM_MEM BUS ADDRESS	
SO-DIMM0	1010 000
SO-DIMM1	1010 001

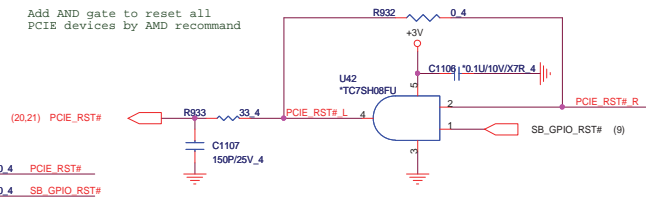




Add AND gate to reset all
PCIe devices by AMD recommend



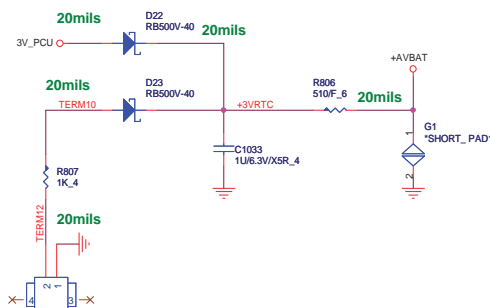
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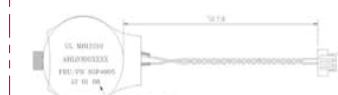
PCIE_VDD# (11)
3V_S5 (9,10,11,12,18,20,23,25,26,36)
3V_PCU (10,13,14,15,18,25,26,29,30,36)
+3V (4,5,6,7,9,10,11,12,13,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)

This page is different AMD Nile
expect RTC circuit

RTC



RTC P/N: AHL03002009 (CR2025)
Don't support chargeable Battery



To STRAPS Page

LPC_CLK0

4.3mA/750mA_4

C1040

6.8y/50V_4

C1041

22pF/50V/NPO_4

EC-DV-1

EC-SIT-15

EC-DIT-15

EC-DV-2

RF Suggest

PCI_CLK_TPM

PCI_CLK_TPM

C376

15pF/50V/NPO_4

C381

15pF/50V/NPO_4

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EC-SIT-15

EC-DIT-15

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EC-SIT-15

EC-DIT-15

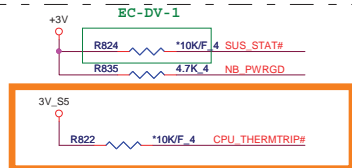
EC-DV-2

RF Suggest

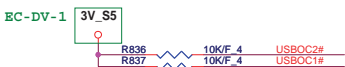
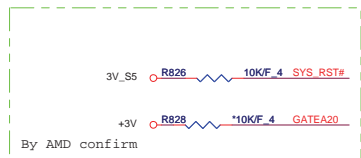
PCI_CLK_TPM

PCI_CLK_TPM

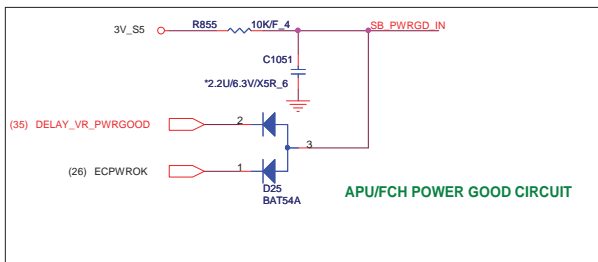
+3V SCL0/SDATA0 is 3V tolerance
AMD datasheet define it
Clock gen/Robson/TV
tuner
/DDR3/DDR3
thermal/Accelerometer



SB/ PWR_GOOD / VDDIO_33_5



To Azalia
HD audio
interface
is 3.3V5
voltage

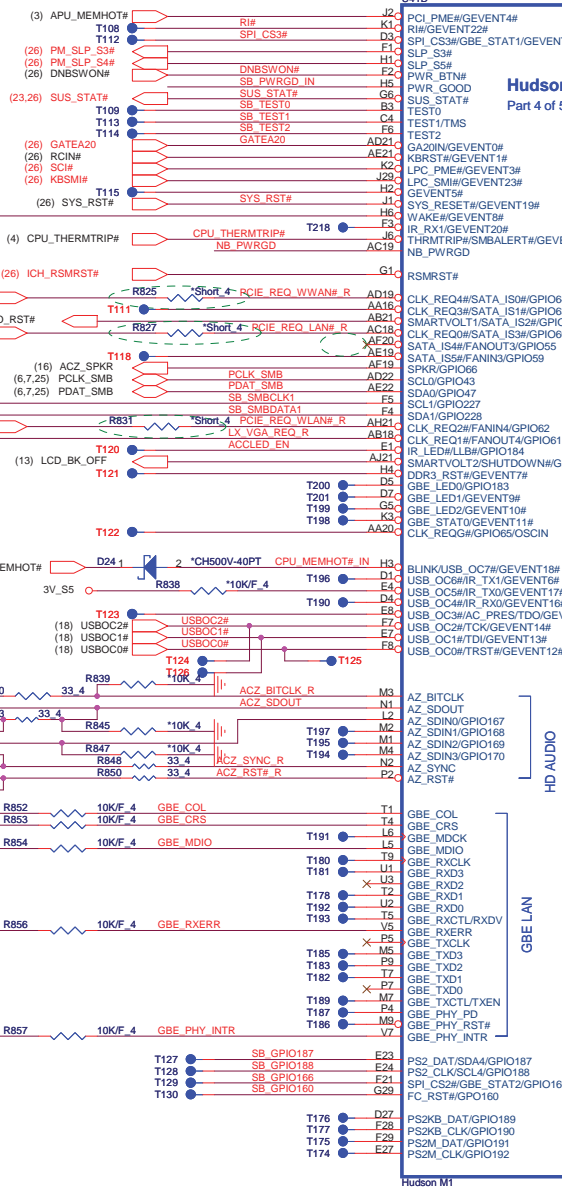


Hudson M1_SB_TEST0,SB_TEST1,SB_TEST2
has internal 10K PD.

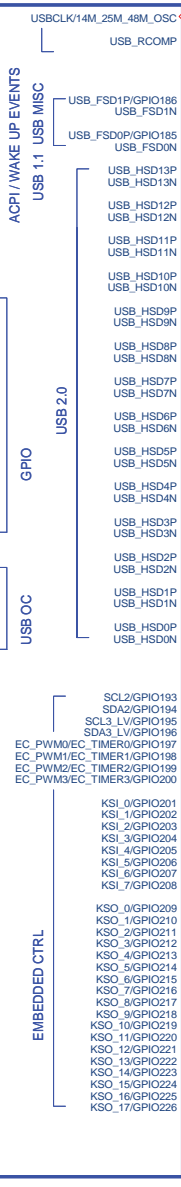
EC-SIT3-3

Add SB_GPIO_RST# form AMD recommend
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it

(16) ACZ_BITCLK_AUDIO
(12) ACZ_SDOUT
(16) ACZ_SDOUT_AUDIO
(16) ACZ_SDI0
(16) ACZ_SYNC_AUDIO
(16) ACZ_RST#_AUDIO

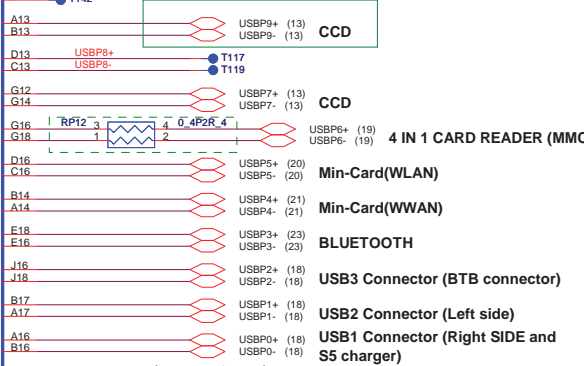
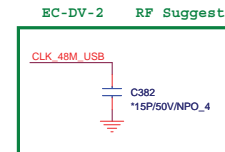


Hudson M1
Part 4 of 5



+3V (4,5,6,7,8,10,11,12,13,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)
3V_S5 (8,10,11,12,18,20,23,25,26,36)
3V_SUS (31,36)

This page is different AMD Nile



SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it

EC_PWM3/EC_TIMER3/GPIO200

EC_PWM3/EC_TIMER3/GPIO200

EC_PWM3/EC_TIMER3/GPIO200

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EC_PWM3/EC_TIMER3/GPIO200

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EC_PWM3/EC_TIMER3/GPIO200

EC_PWM3/EC_TIMER3/GPIO200



SATA PORT 0,1,2,3
can support AHCI
mode

PLACE SATA AC COUPLING
CAPS CLOSE TO Hudson M1

SATA HDD

(17) SATA_TXP0
(17) SATA_TXN0
(17) SATA_RXN0
(17) SATA_RXP0

C1052 0.01U/16V/X7R_4
C1053 0.01U/16V/X7R_4
C1054 0.01U/16V/X7R_4
C1055 0.01U/16V/X7R_4

SATA_TXP0 C AH9
SATA_TXN0 C AJ9
SATA_RXN0 C AJ8
SATA_RXP0 C AH8

T282 AH10
T283 AJ10
T284 AG10
T285 AF10
T286 AG12
T287 AF12
T288 AJ12
T289 AH12
T290 AH14
T291 AJ14
T292 AG14
T293 AF14
T294 AG17
T295 AF17
T296 AJ17
T297 AH17
T298 AJ18
T299 AH18
T300 AH19
T301 AJ19

XTLVDD_SATA-- SATA
crystal power
PLVDD_SATA--
SATA PLL
POWER

PLACE SATA_CAL RES
VERY CLOSE TO BALL
OF Hudson M1

AVDD_SATA

R867 1K/F_4
R868 931/F_4
+3V0 R869 10K/F_4
AD11

C1056 *22P/50V/NPO_4
Y10 *25MHZ
R870 *1M/F_4
C1057 *22P/50V/NPO_4
SATA_X1 AD16
SATA_X2 AC16

SPI_DI J5
SPI_DO E2
SPI_CLK K4
SPI_CS1# K9
ROM_RST# G2
T131

EC-SIT-14

16Mbit (2M Byte), SPI

Winbond AKE38ZP0N00
SST AKE28FP0K07
MX AKE37FP0Z13

SPI_CS1# R881 *47_4
SPI_CLK R884 *47_4
SPI_DO R885 *15_4
SATA_X1 AD16
SATA_X2 AC16
U44
CE# VDD 8
SCK 6
SI 5
SO 2
HOLD# 7
WP# VSS 4
TP13
*MX25L1605A

EC-DV-2 RF Suggest

SPI_CLK
C370 *15P/50V/NPO_4

EC-DV-1

Hudson M1

Part 2 of 5

FC_CLK AH28
FC_FBCLKOUT AG28
FC_FBCLKIN AF26
FC_OE#/GPIO145 AF28
FC_AVD#/GPIO146 AG29
FC_WE#/GPIO148 AG26
FC_CE1#/GPIO149 AF27
FC_CE2#/GPIO150 AF29
FC_INT1/GPIO144 AF29
FC_INT2/GPIO147 AH27
FC_ADQ0/GPIO128 AJ27
FC_ADQ1/GPIO129 AJ26
FC_ADQ2/GPIO130 AH25
FC_ADQ3/GPIO131 AH24
FC_ADQ4/GPIO132 AG23
FC_ADQ5/GPIO133 AH23
FC_ADQ6/GPIO134 AJ22
FC_ADQ7/GPIO135 AG21
FC_ADQ8/GPIO136 AH22
FC_ADQ9/GPIO137 AJ23
FC_ADQ10/GPIO138 AJ23
FC_ADQ11/GPIO139 AJ24
FC_ADQ12/GPIO140 AJ25
FC_ADQ13/GPIO141 AG25
FC_ADQ14/GPIO142 AH26
FC_ADQ15/GPIO143

FLASH

SERIAL ATA

HW MONITOR

SPI ROM

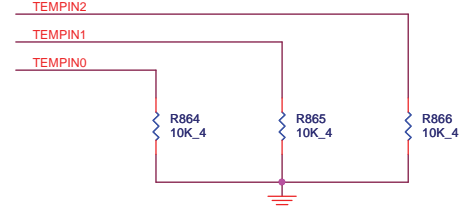
NC1
NC2

FANOUT0/GPIO52 W5
FANOUT1/GPIO53 W6
FANOUT2/GPIO54 Y9
FANIN0/GPIO56 W7
FANIN1/GPIO57 V9
FANIN2/GPIO58 W8
TEMPIN0/GPIO171 A6
TEMPIN1/GPIO172 A5
TEMPIN2/GPIO173 B5
TEMPIN3/TALERT#/GPIO174 C7
TEMP_COMM C7
VIN0/GPIO175 A3
VIN1/GPIO176 B4
VIN2/GPIO177 A4
VIN3/GPIO178 C5
VIN4/GPIO179 A7
VIN5/GPIO180 B7
VIN6/GBE_STAT3/GPIO181 B8
VIN7/GBE_LED3/GPIO182 B8
G27 X
Y2 X

AVDD_SATA (11)
+3V (4,5,6,7,8,9,11,12,13,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)
3V_S5 (8,9,11,12,18,20,23,25,26,36)
3V_PCU (8,13,14,15,18,25,26,29,30,36)

This page is different AMD Nile

AMD recommend : TEMPIN0 / TEMPIN1 / TEMPIN2
can not maintain on floating stages when without usage.
Do not care pull high or pull down.

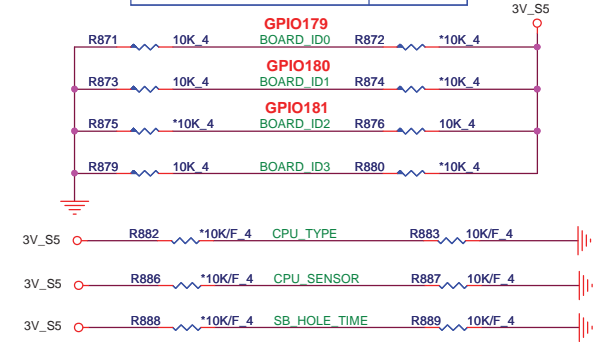


MB ID

CPU THERMAL	GPIO179
External	1
SB-TSI	0

SB8XX Hold Time	GPIO180
1.2V	1
1.1V	0

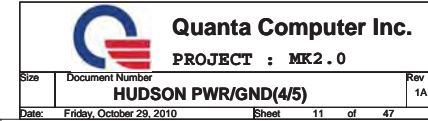
DU1/MK2	GPIO181
MK2.0 AMD	1
DU1.0 AMD	0



Quanta Computer Inc.
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	HUDSON SATA/BIDS(3/5)	1A
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PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE

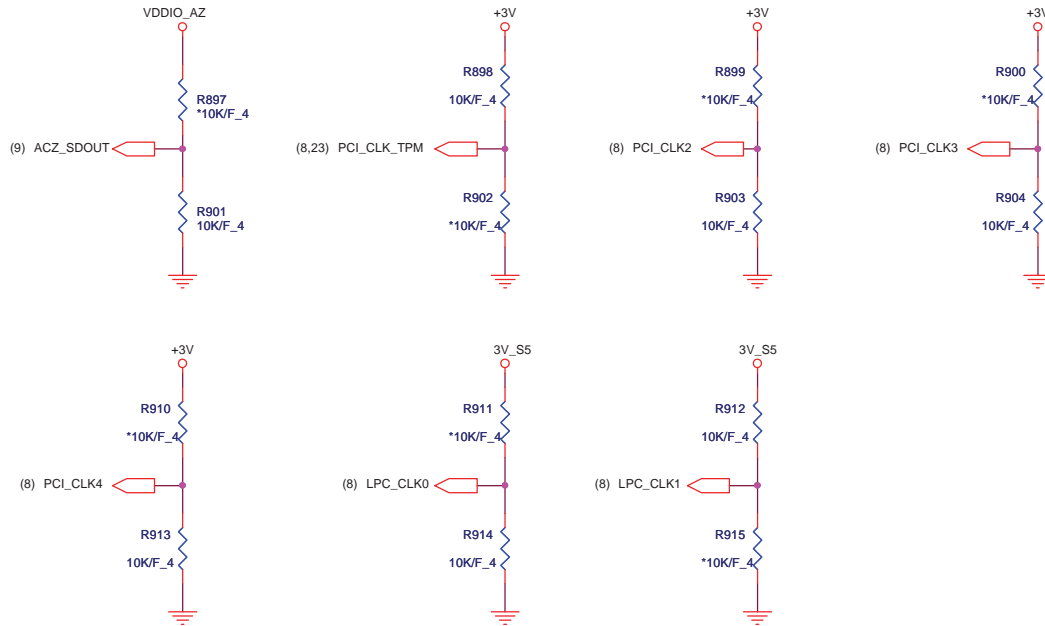




OVERLAP COMMON PADS WHERE
POSSIBLE FOR DUAL-OP RESISTORS.

REQUIRED STRAPS

internal have pull
Hi 10K , confirm AMD
ward this pull Hi
not need



PCI_CLK4 CPU/NB HT Clock Selection
0 V - Reserved.
3.3 V - Required setting for integrated clock mode.
This strap is not used if the strap CLKGEN is
configured for external clock generator mode.

REQUIRED STRAPS

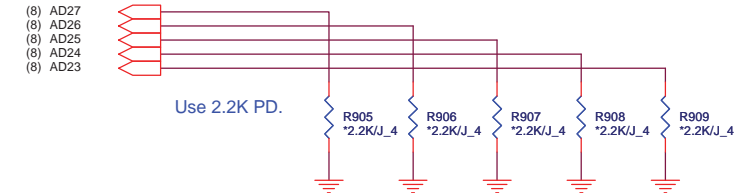
	AZ_SDOUT	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	GPIO200	GPIO199
PULL HIGH	LOW POWER MODE	ALLOW PCIE Gen2 DEFAULT	Watchdog Timer Enabled	USE DEBUG STRAP	non_Fusion CLOCK MODE	EC ENABLED	CLKGEN ENABLED DEFAULT	H,H = Reserved H,L = SPI ROM (Default)	
PULL LOW	PERFORMANCE MODE DEFAULT	FORCE PCIE Gen1	Watchdog Timer Disabled DEFAULT	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED DEFAULT	CLKGEN DISABLED	L,H = LPC ROM L,L = FWH ROM	

VDDIO_AZ (11)
+3V (4,5,6,7,8,9,10,11,13,14,15,16,17,19,20,21,23,24,25,26,27,30,32,33,35,36)
3V_S5 (8,9,10,11,18,20,23,25,26,36)

12

DEBUG STRAPS

HUDSON-M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]



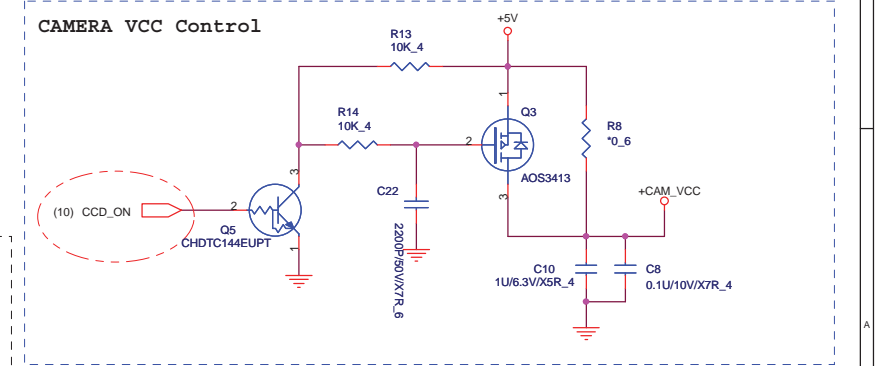
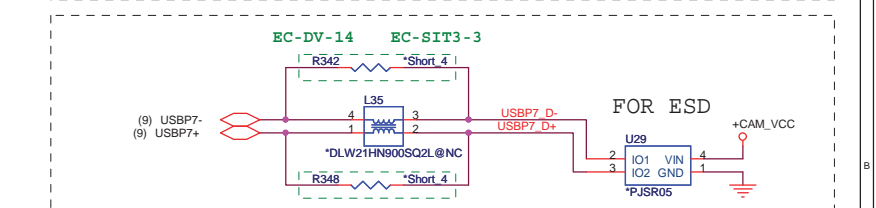
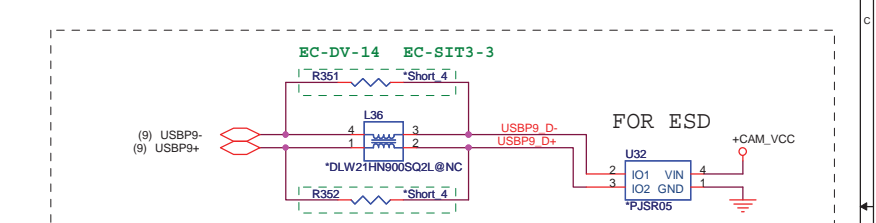
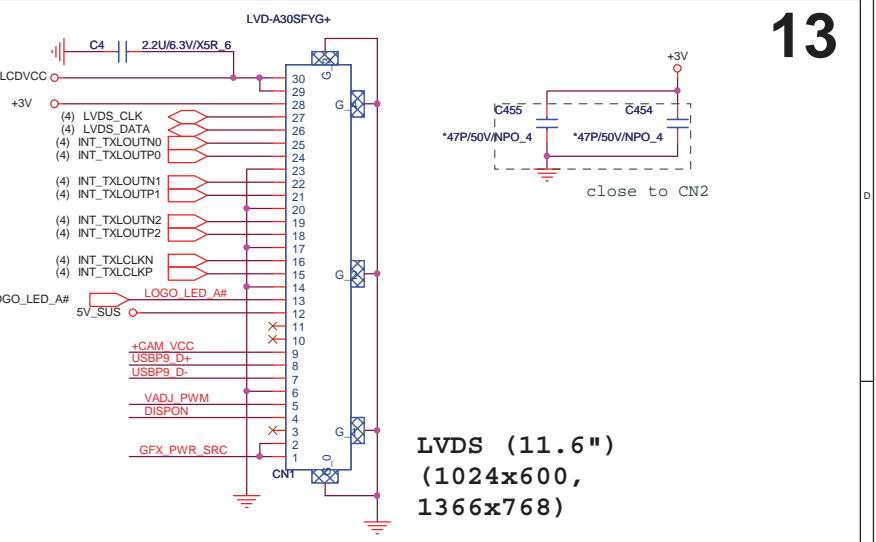
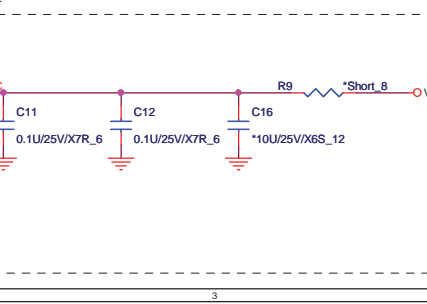
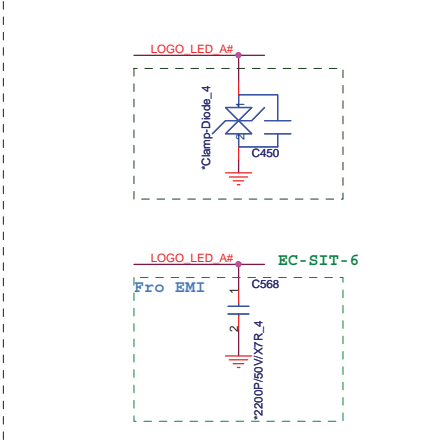
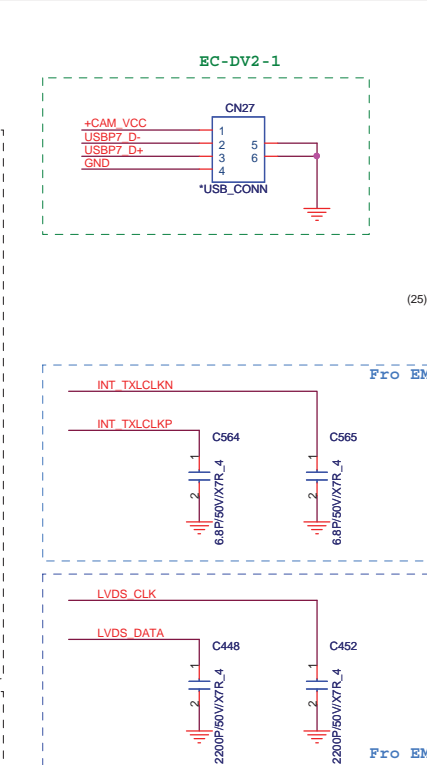
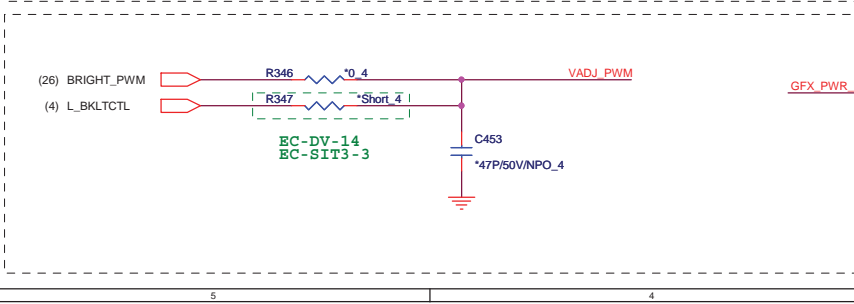
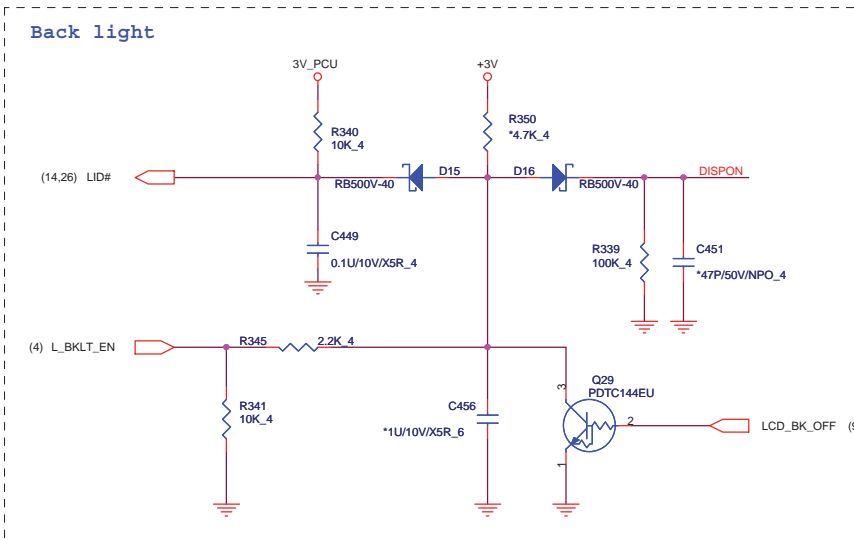
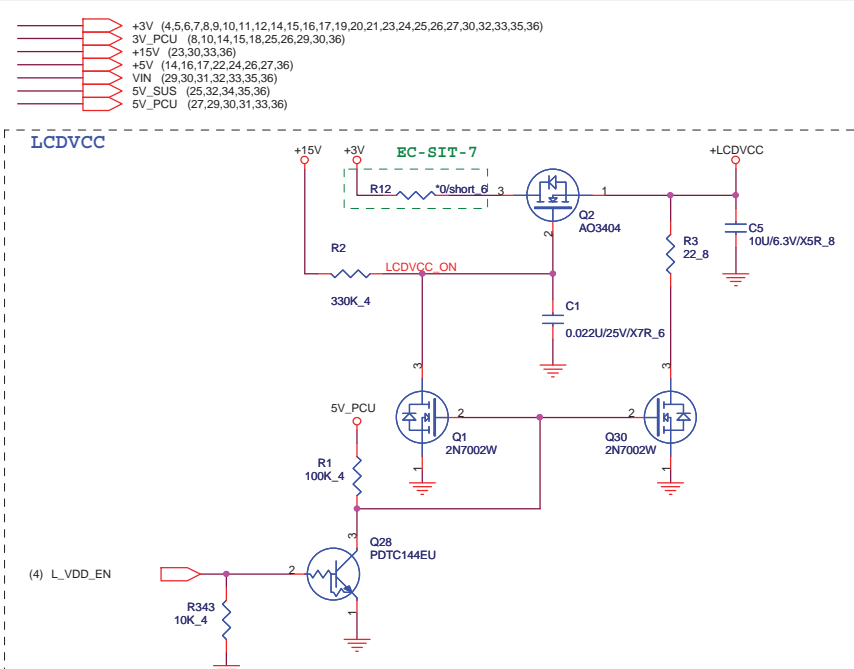
	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



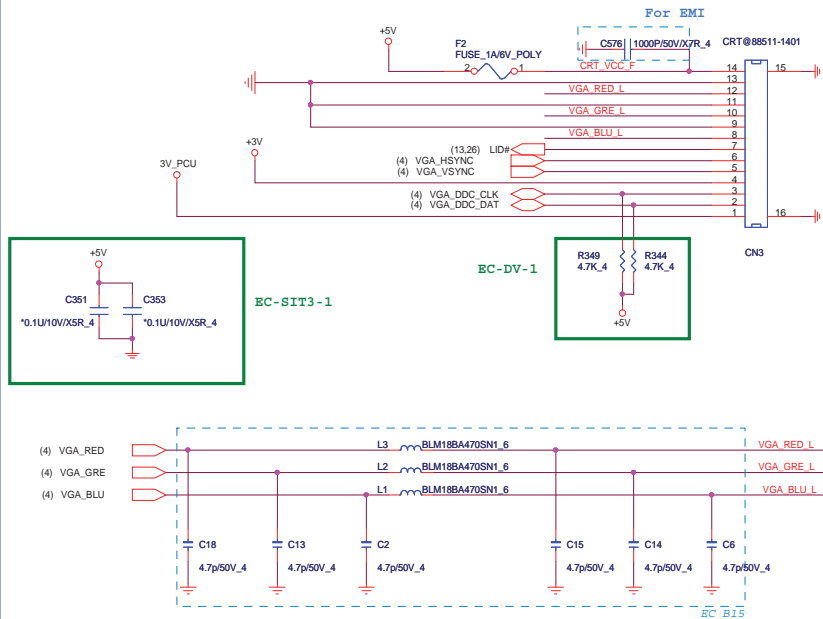
Quanta Computer Inc.

PROJECT : MK2.0

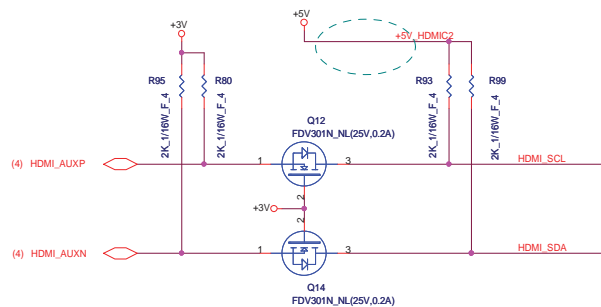
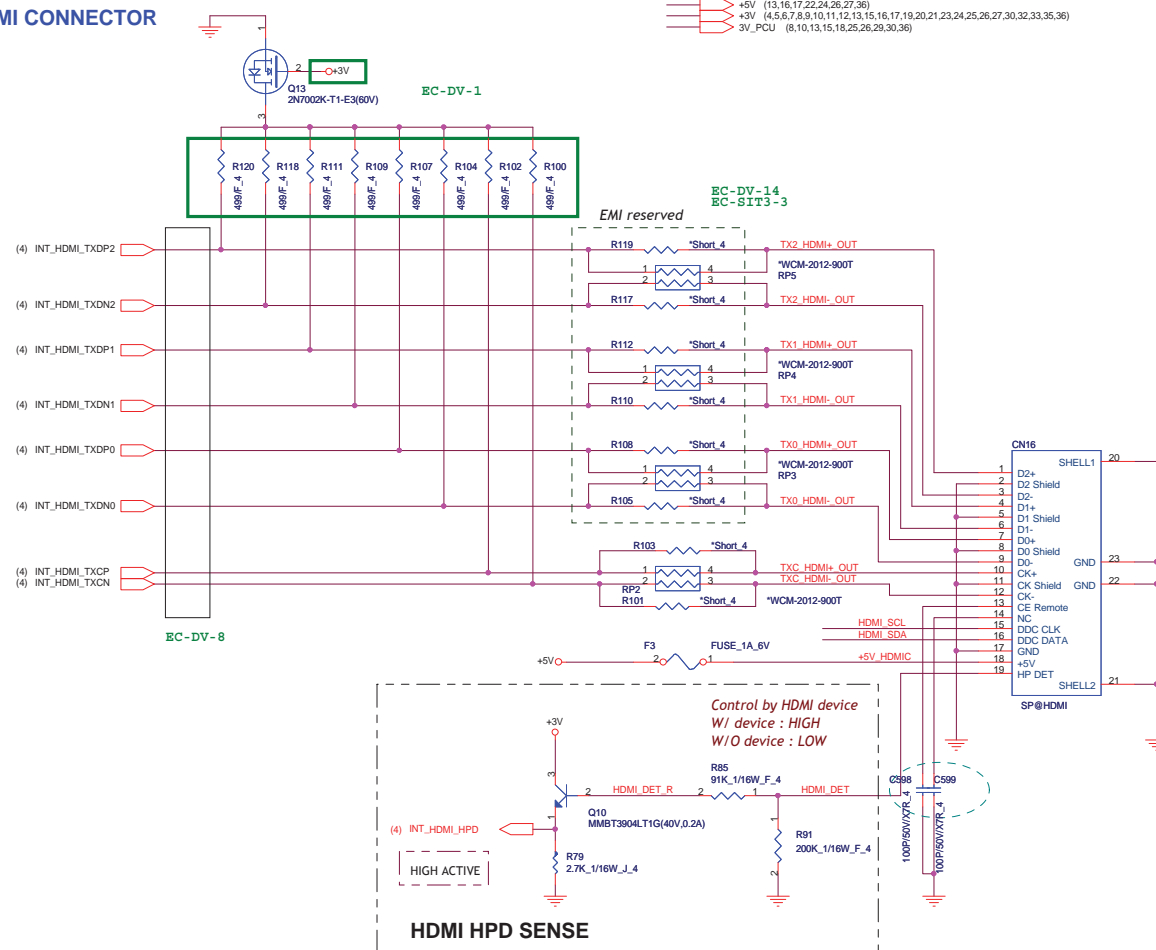
Size	Document Number	Rev
	HUDSON STRAPS/PWRGD(5/5)	1A
Date:	Friday, October 29, 2010	Sheet 12 of 47



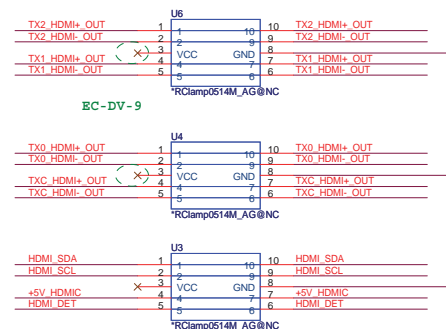
CRT FFC CONNECTOR



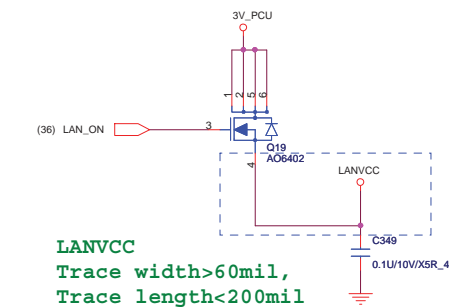
HDMI CONNECTOR



For ESD ---> Layout note: Place close to HDMI Conn



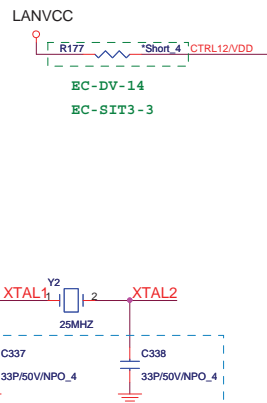
LANVCC



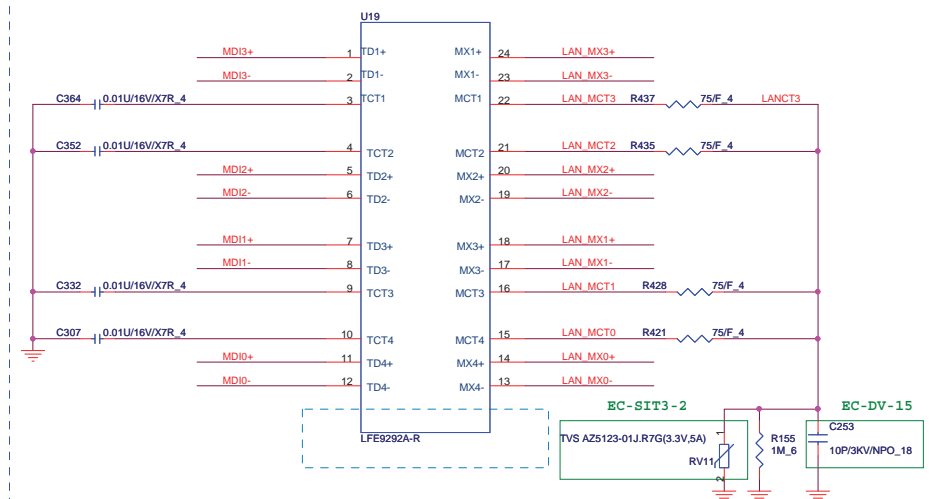
```

LANVCC
Trace width>60mil,
Trace length<200mil

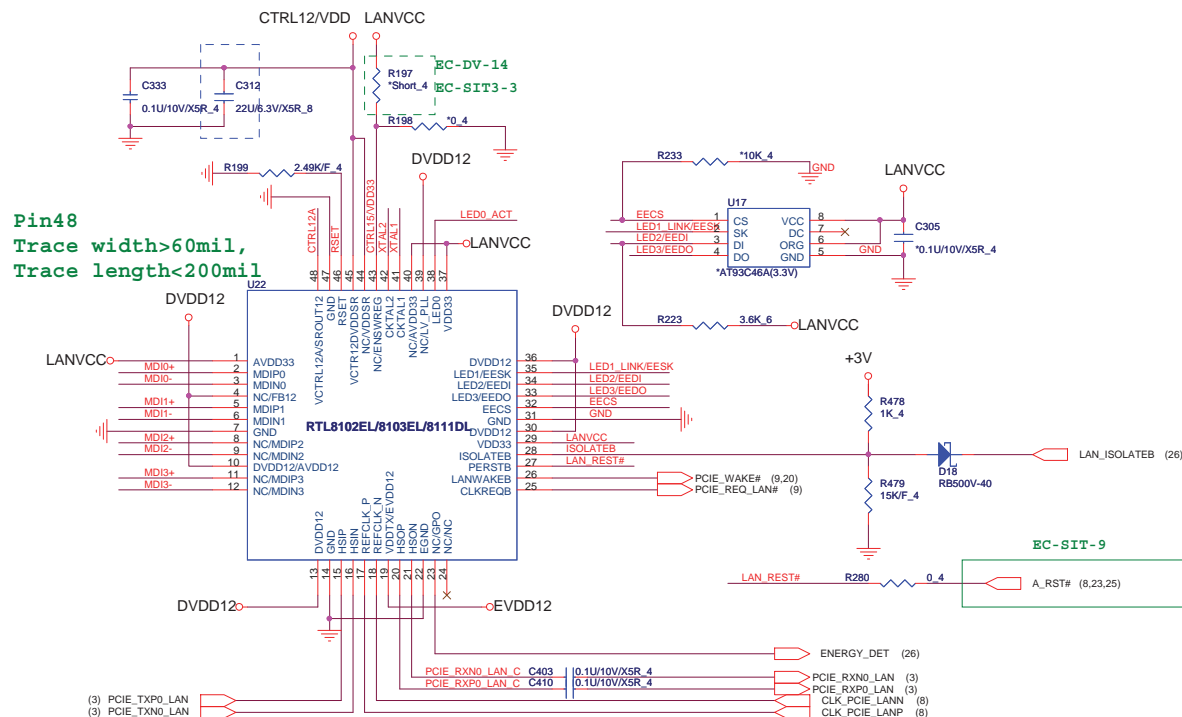
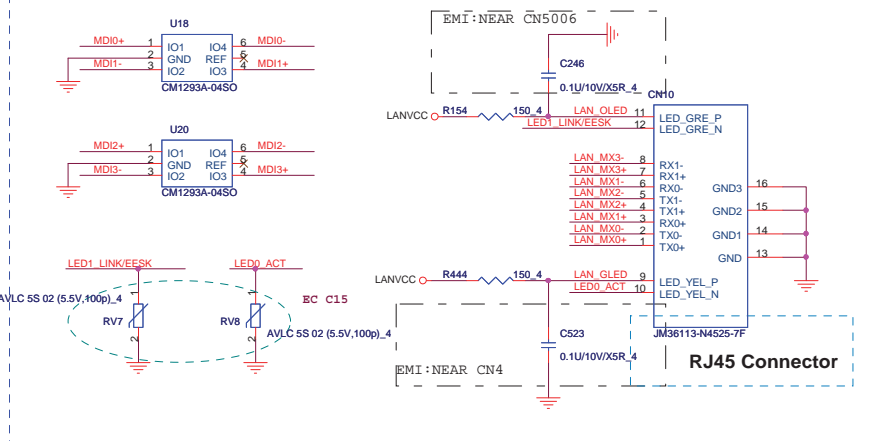
```



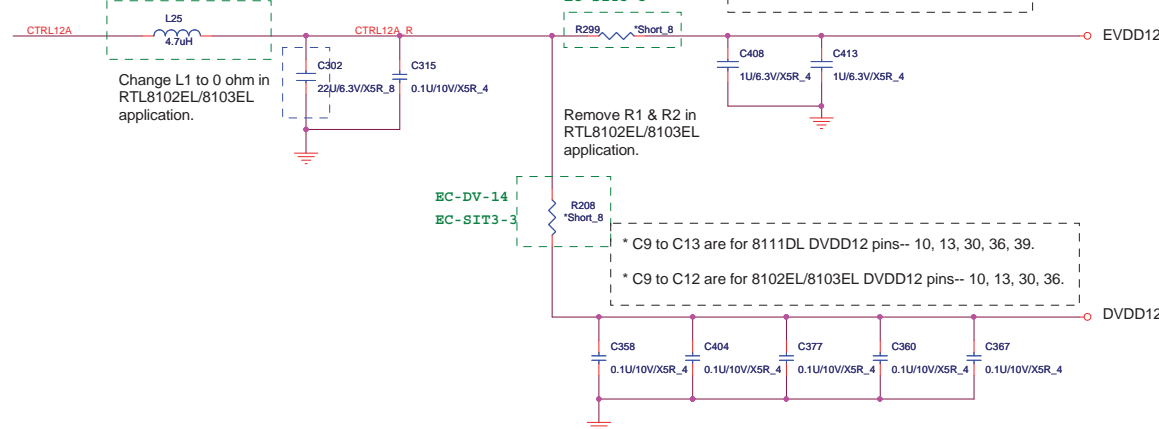
Transformer



RJ45 Connector



Note 1: The Trace length between L1 and 8111DL's Pin 1 must be within 0.5 cm. C5 and C8 to L1 must be within 0.5cm. Refer to Layout guide for more detail.




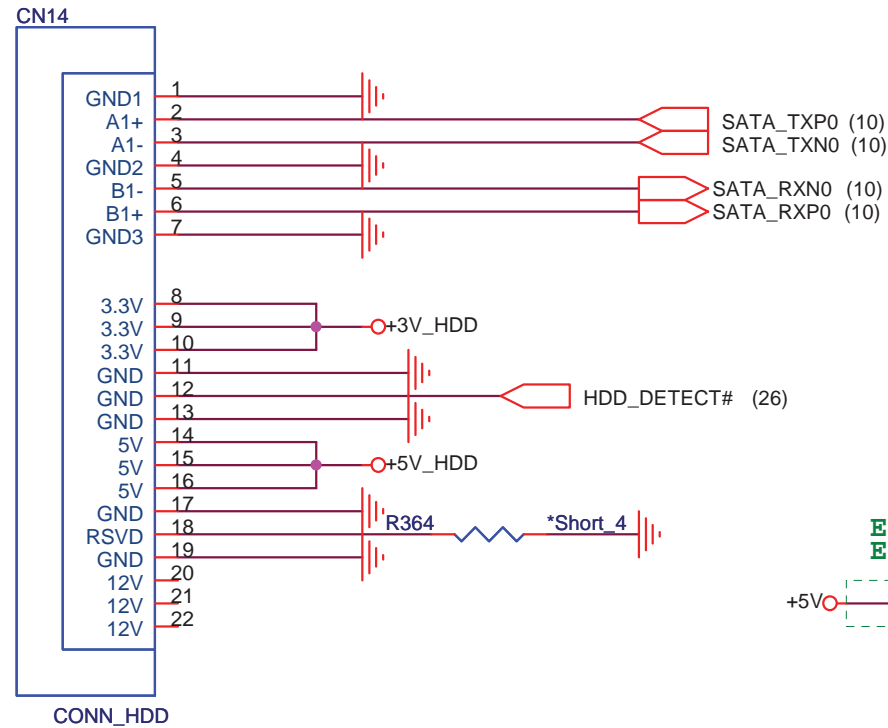
To support Wake-on-Jack or Wake-on-Ring, the CODEC VAUX_3.3 pins must be powered by a rail that is not removed unless AC power is removed.

AVDD_3.3 pin is output of internal LDO. Do NOT connect to external supply.

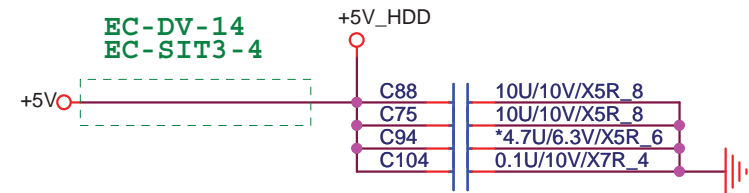
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms). Place bypass caps very close to device.



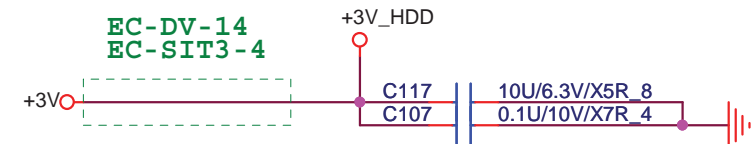
1

+3V (4,5,6,7,8,9,10,11,12,13,14,15,16,19,20,21,23,24,25,26,27,30,32,33,35,36)
+5V (13,14,16,22,24,26,27,36)



DC Current rating: 2 A (MAX)



DC Current rating: 3 A (MAX)



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USB SLEEP CHARGE (NEW)

CB0/CB1	Function	Int./Ext. R
0 0	S5 auto detect	Use Int.R
0 1	Blackberry(choice)	NC
1 0	iPod/iPhone(choice)	Use Ext. R
1 1	S0 auto detect	NC

Sleep charger notice

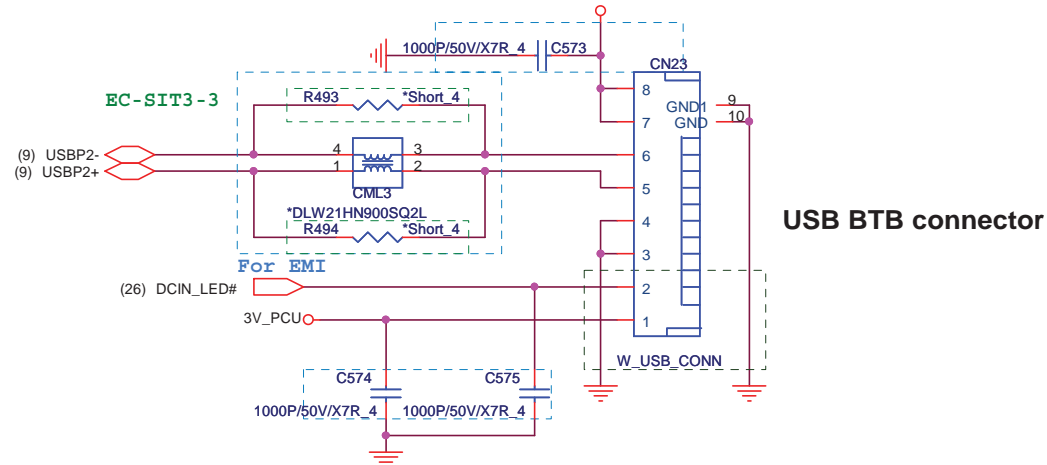
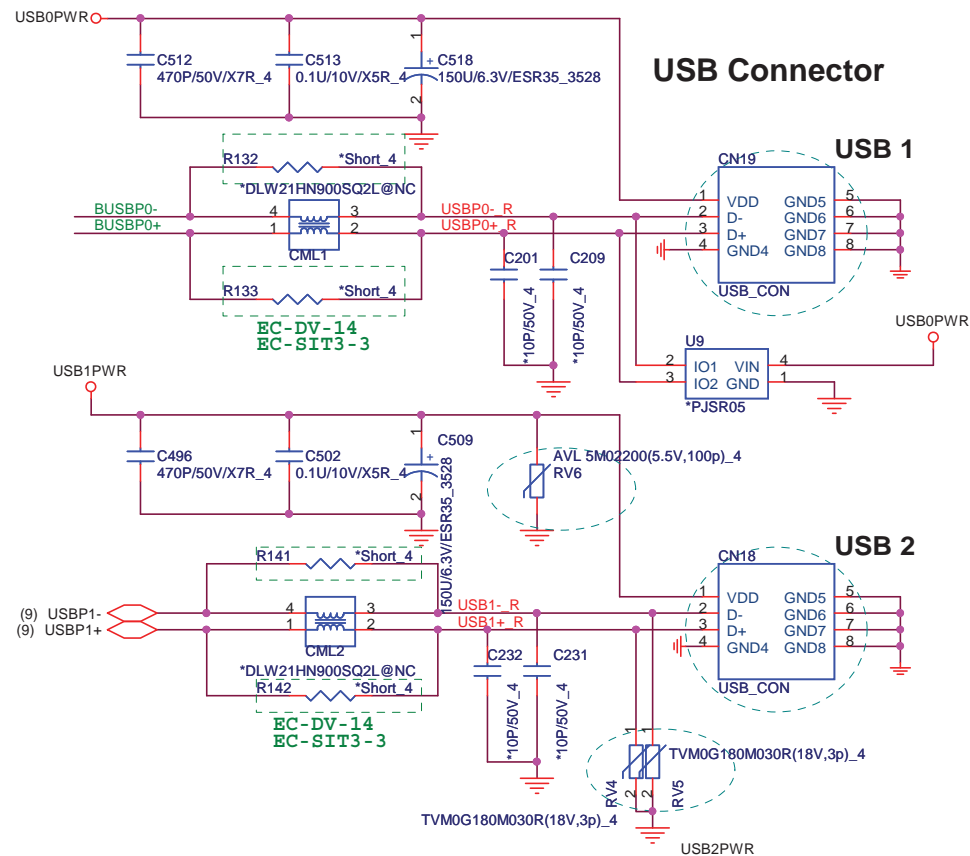
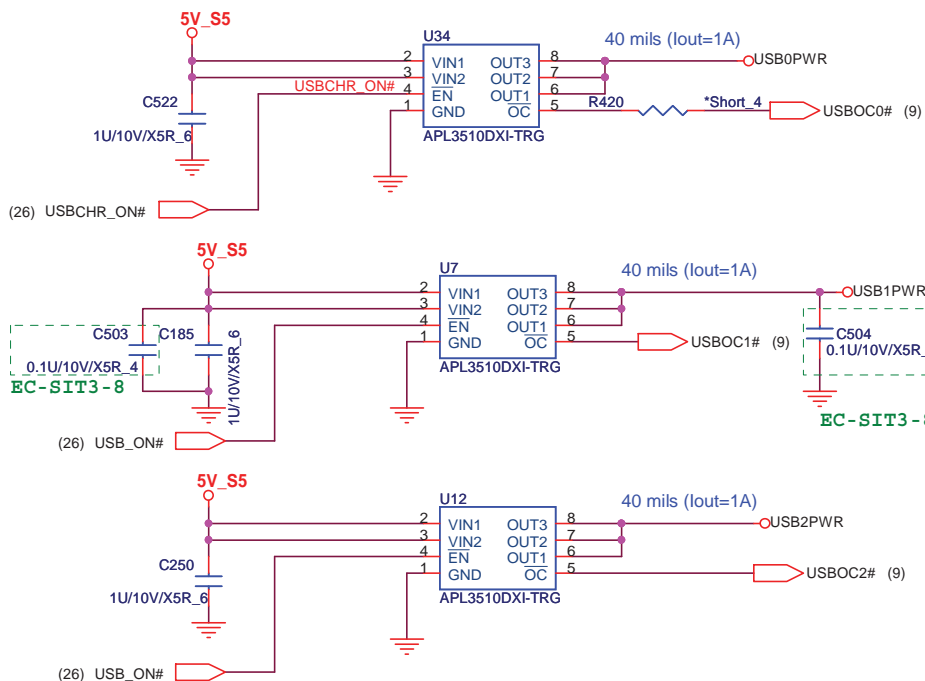
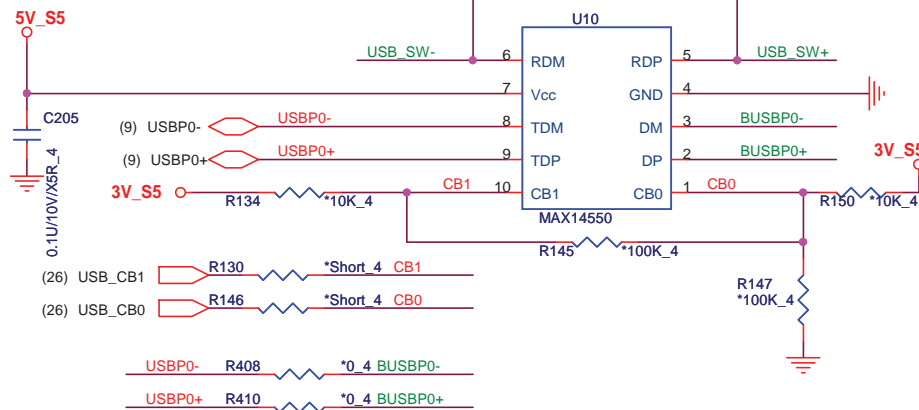


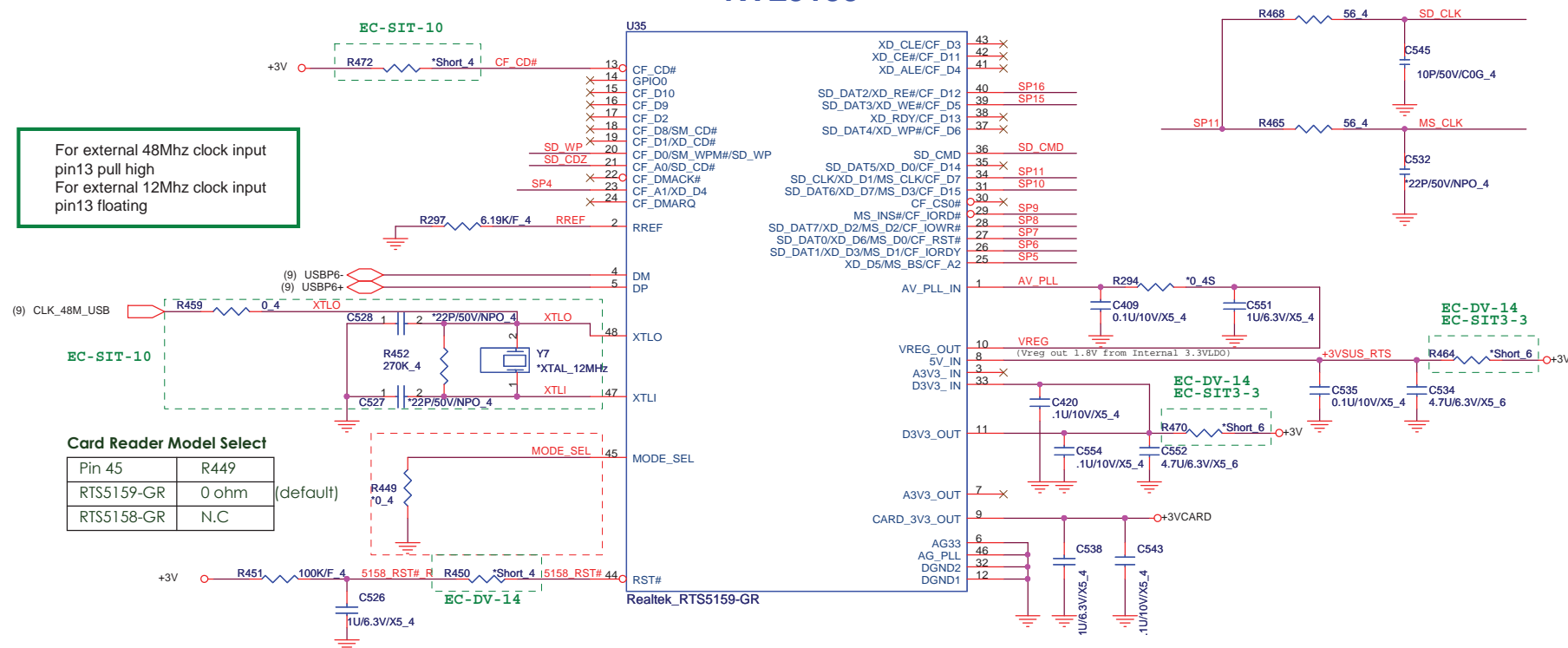
Diagram of the 40-pin connector for the 68000, showing four pins connected to 5V_S5, 3V_S5, 5V_SUS, and 3V_PCU.



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Size	Document Number USB x 3	Rev 1A
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RTL5159

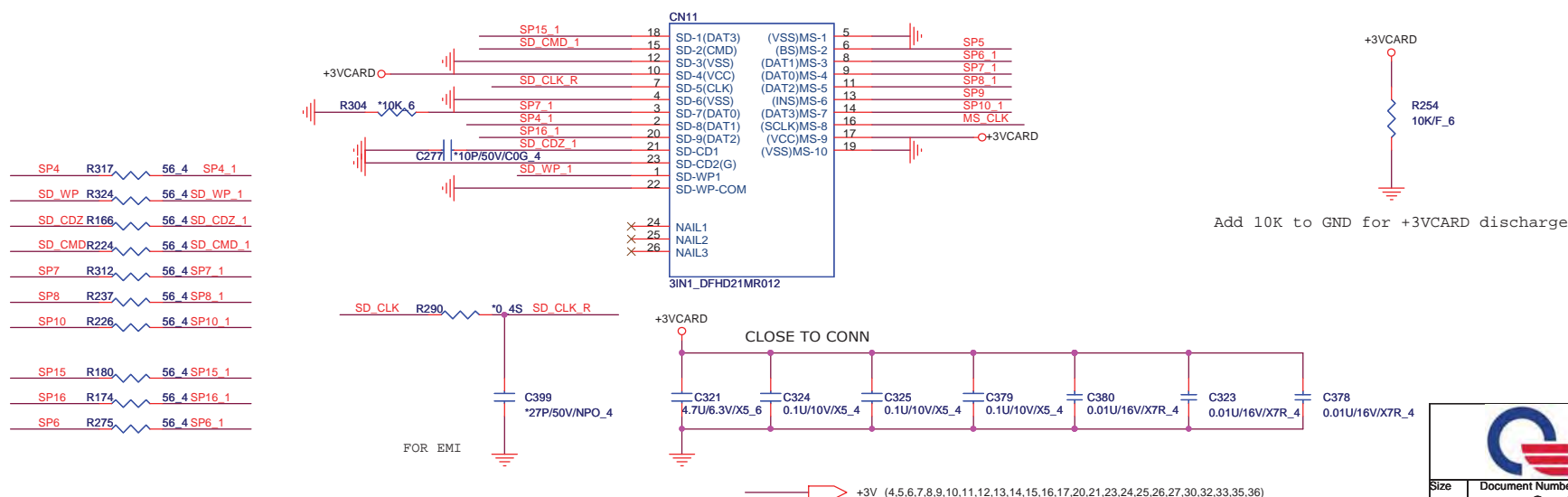


Note:

	SD/MMC	MS
SP0		
SP1		
SP2	SD_WP	
SP3	SD_CD#	
SP4	SD_DAT1	
SP5		MS_BS
SP6		MS_D1
SP7	SD_DAT0	MS_D0
SP8	SD_DAT7	MS_D2
SP9		MS_INS#
SP10	SD_DAT6	MS_D3
SP11	SD_CLK	MS_SCLK
SP12	SD_DAT5	
SP13	SD_DAT4	
SP14		
SP15	SD_DAT3	
SP16	SD_DAT2	
SP17		
SP18		
SP19		

Card Reader Model Select	
Pin 45	R449
RTS5159-GR	0 ohm (default)
RTS5158-GR	N.C

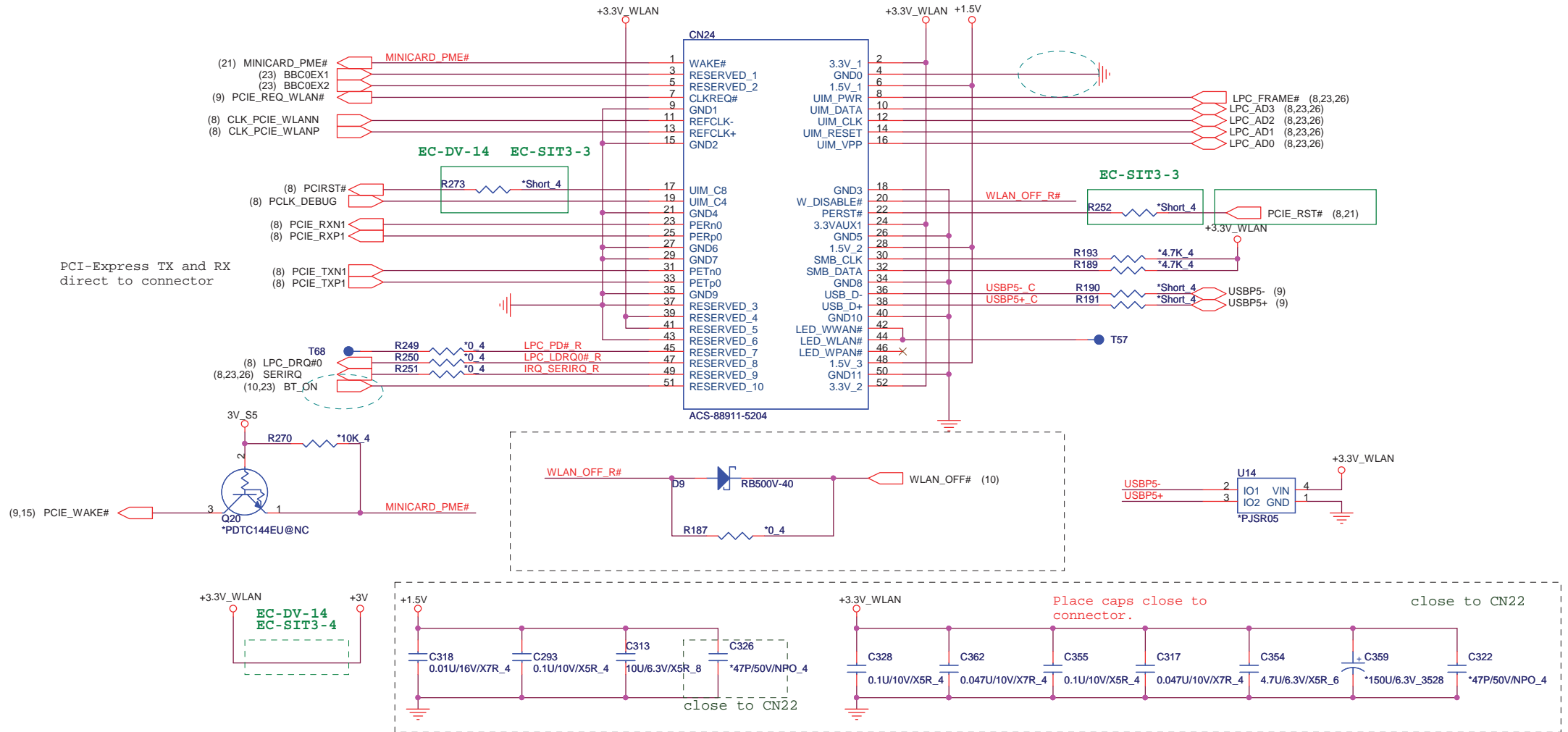
3 IN 1 CARD READER



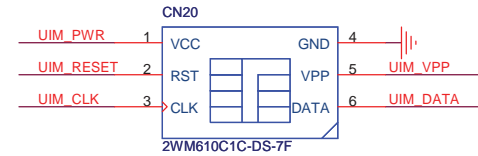
MiniCard WLAN connector

+3V (4,5,6,7,8,9,10,11,12,13,14,15,16,17,19,21,23,24,25,26,27,30,32,33,35,36)
 +1.5V (21,36)
 3V_S5 (8,9,10,11,12,18,23,25,26,36)

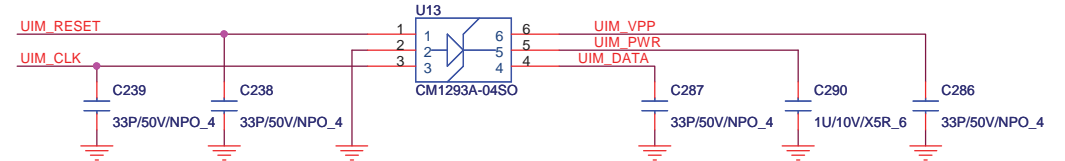
20



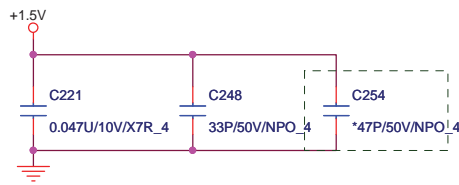
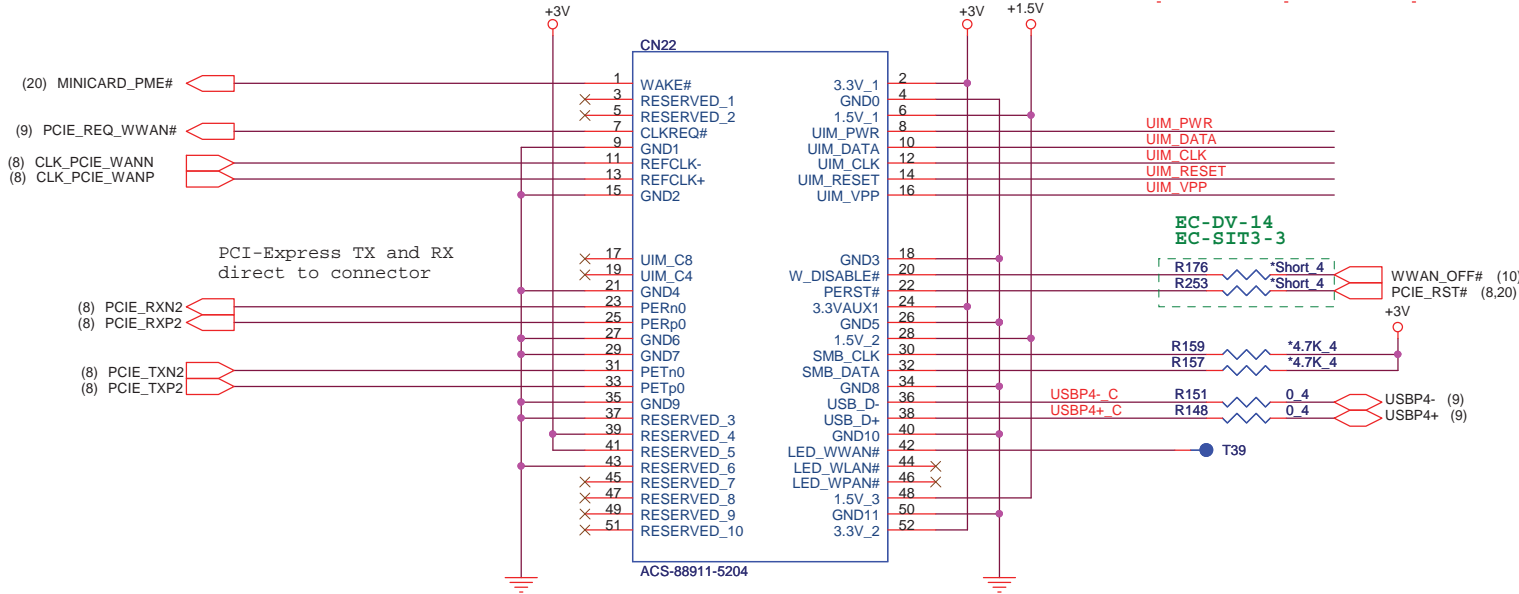
SIM Card CONN



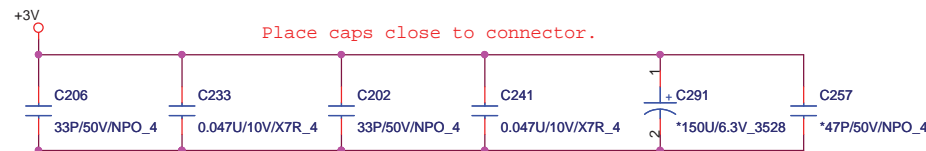
Layout Note:
UIM_RESET,UIM_CLK,UIM_DATA routing as short as possible



MiniCard WWAN connector

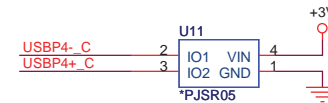


close to CN21

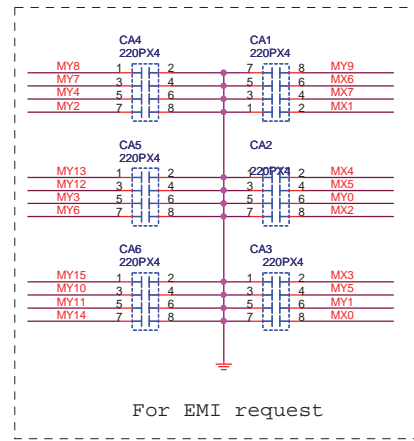
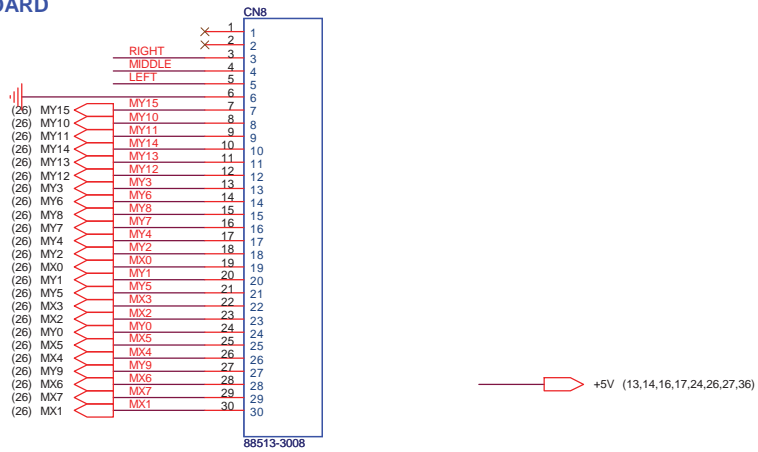


Place caps close to connector.

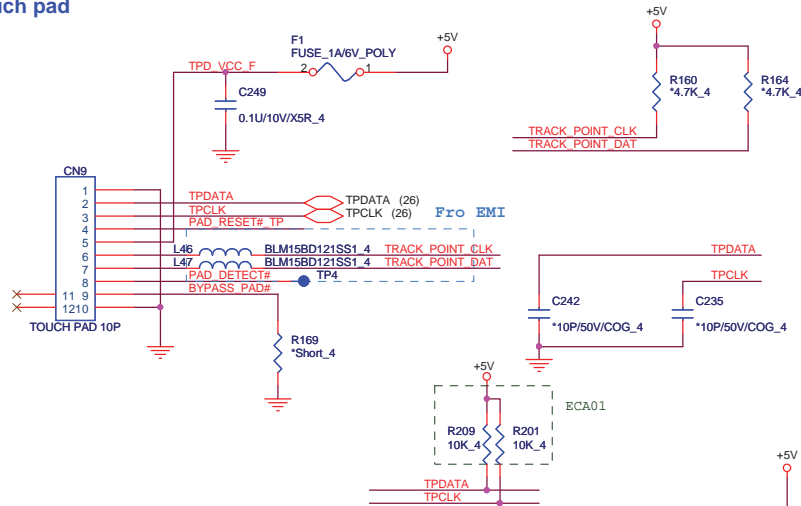
close to CN21



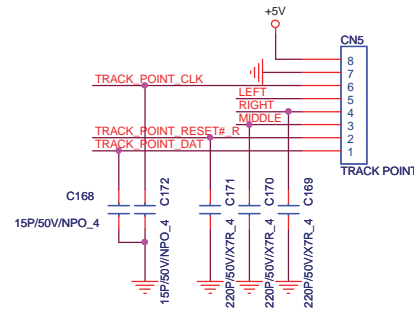
KEYBOARD



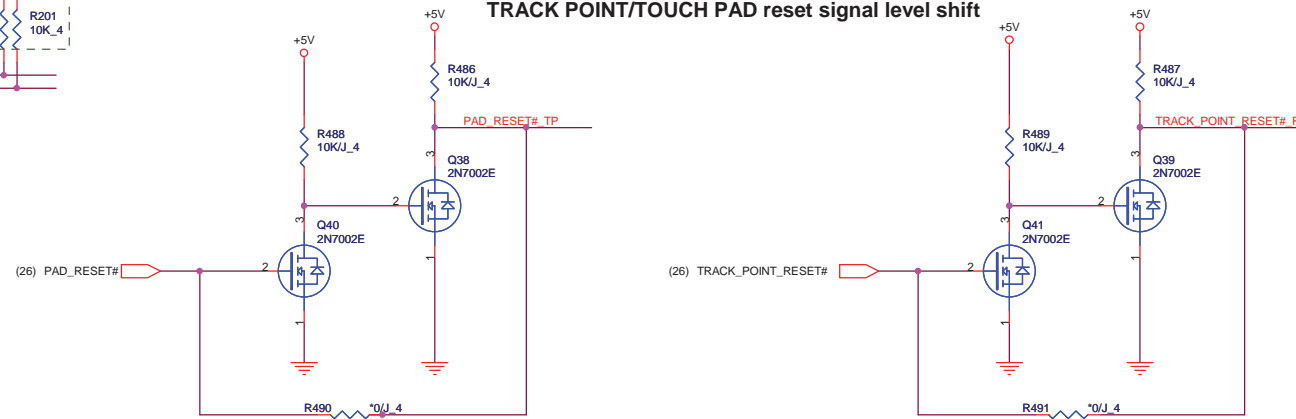
Touch pad



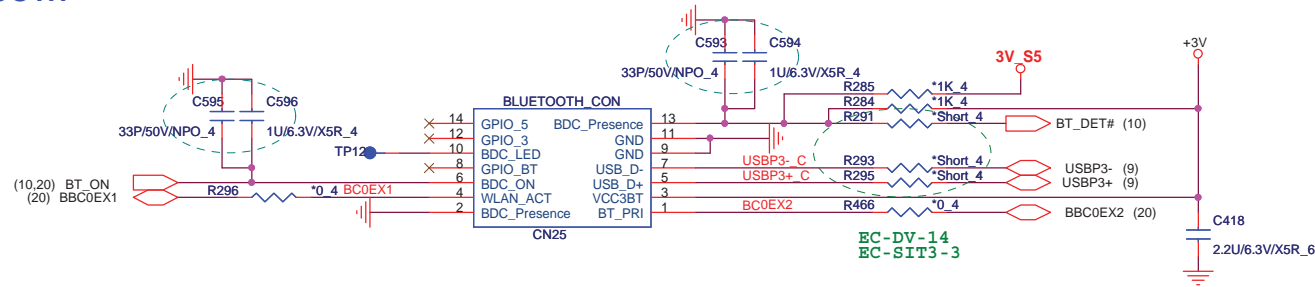
TRACK POINT



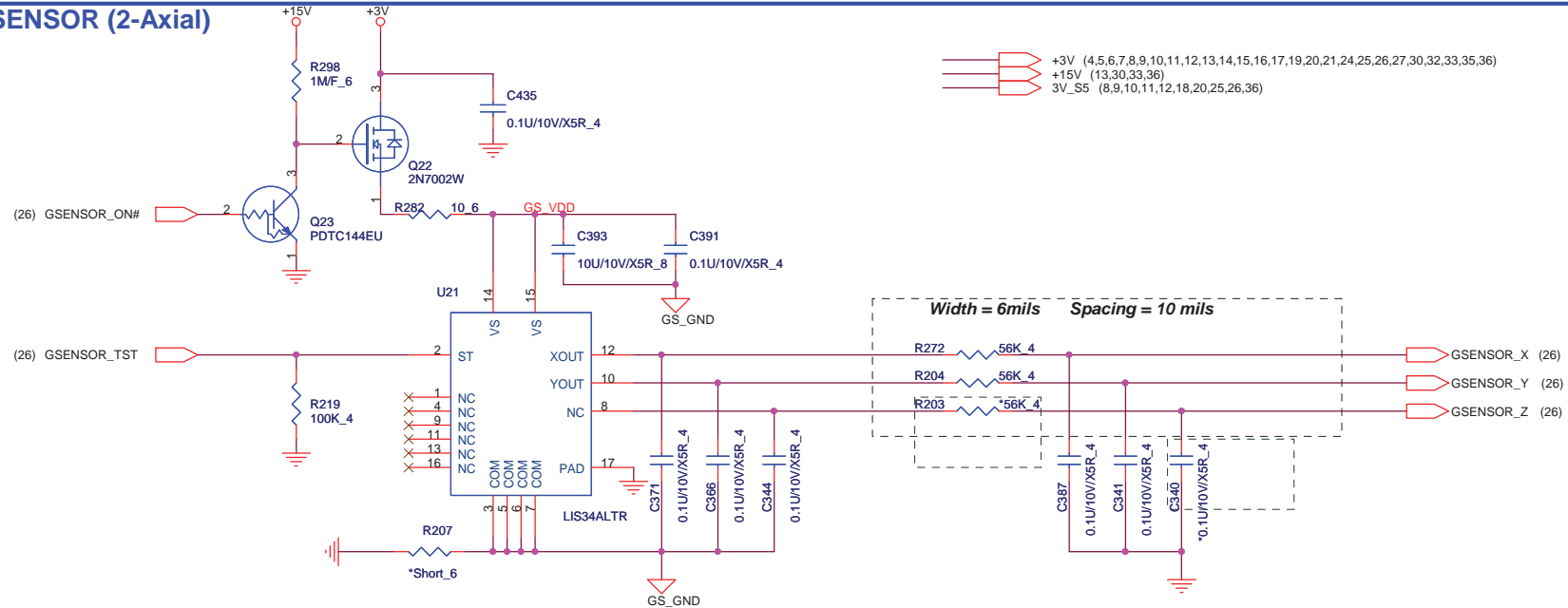
TRACK POINT/TOUCH PAD reset signal level shift



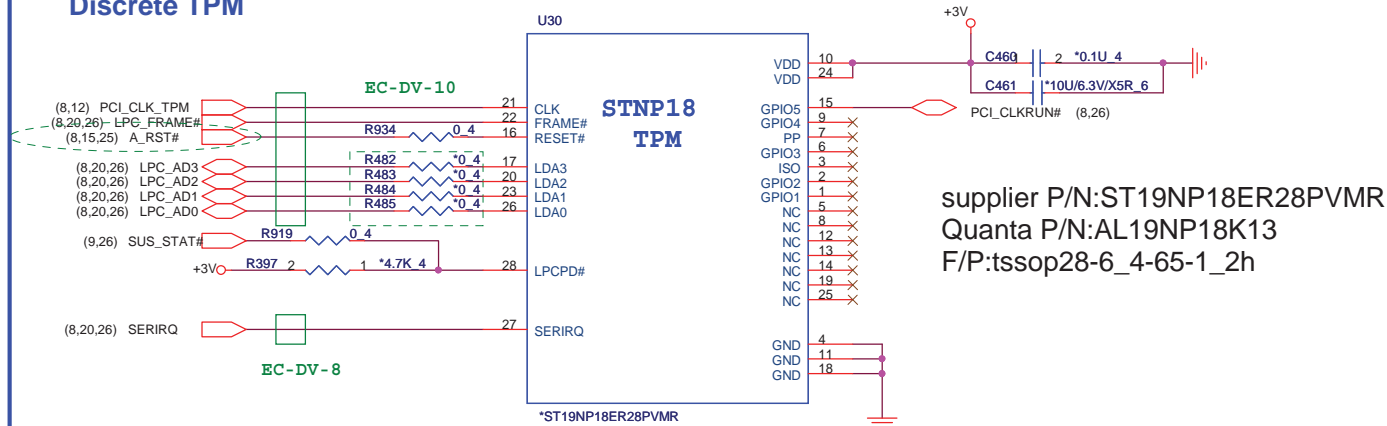
BLUETOOTH



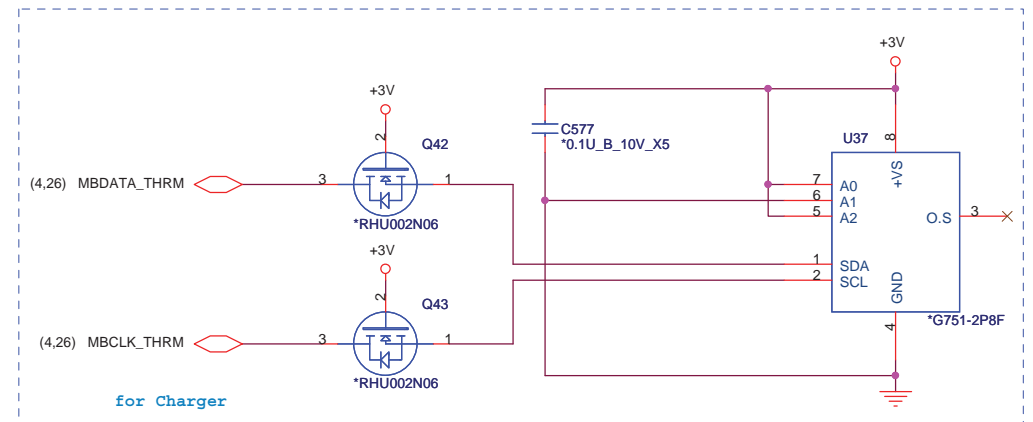
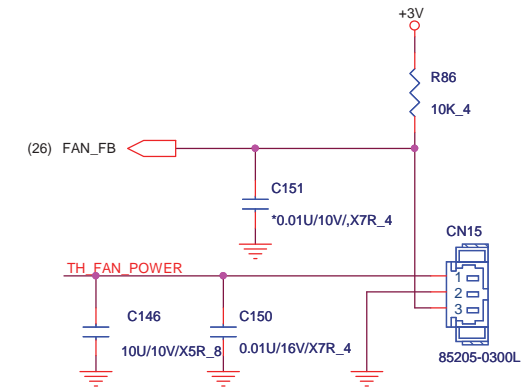
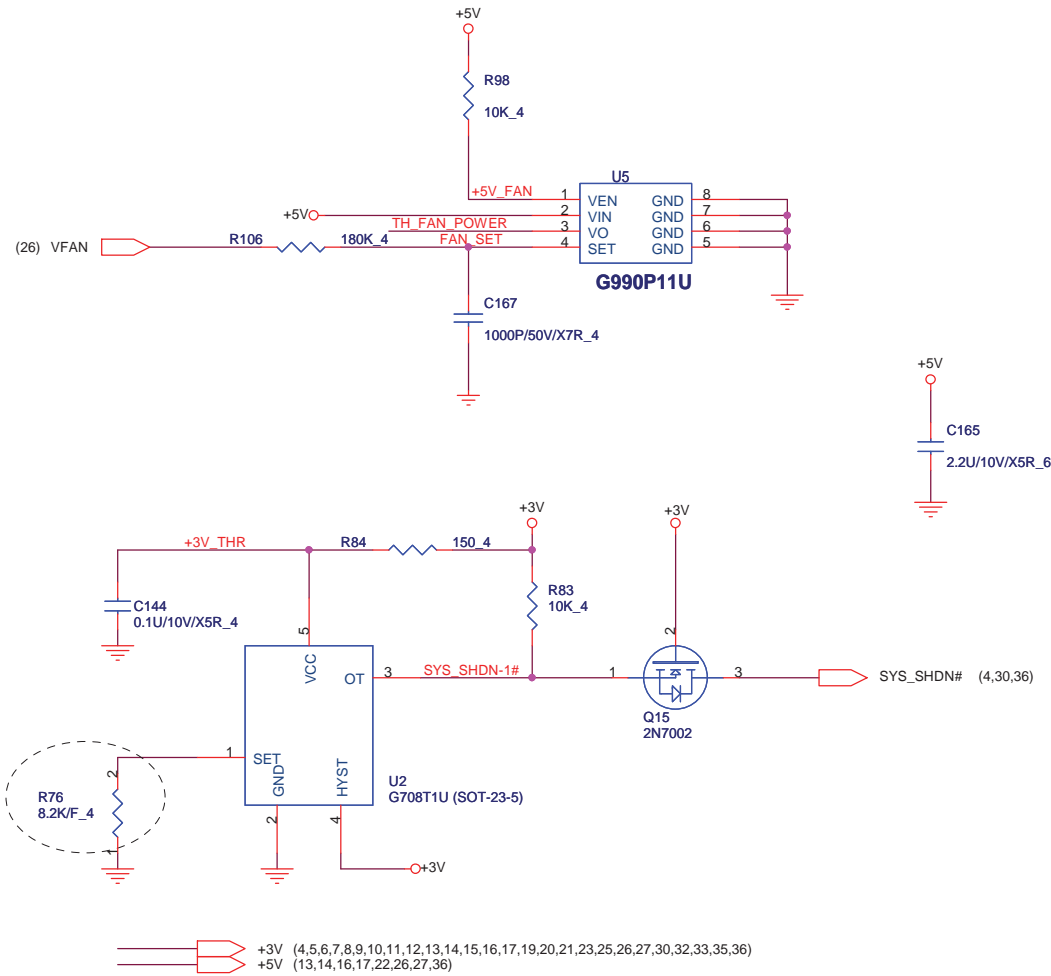
G-SENSOR (2-Axial)



Discrete TPM



FANPWR = 1.6*VSET



for Charger

ADDRESS: 9AH

ADDRESS							
1	0	0	1	A2	A1	A0	0
MSB				LSB			

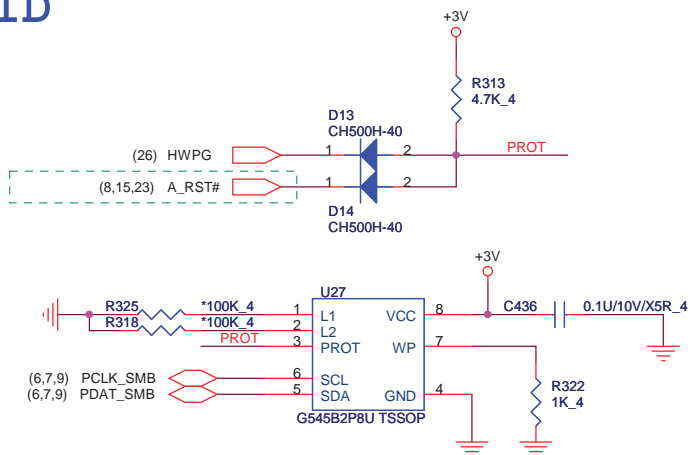


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	FAN/Thermal	1A
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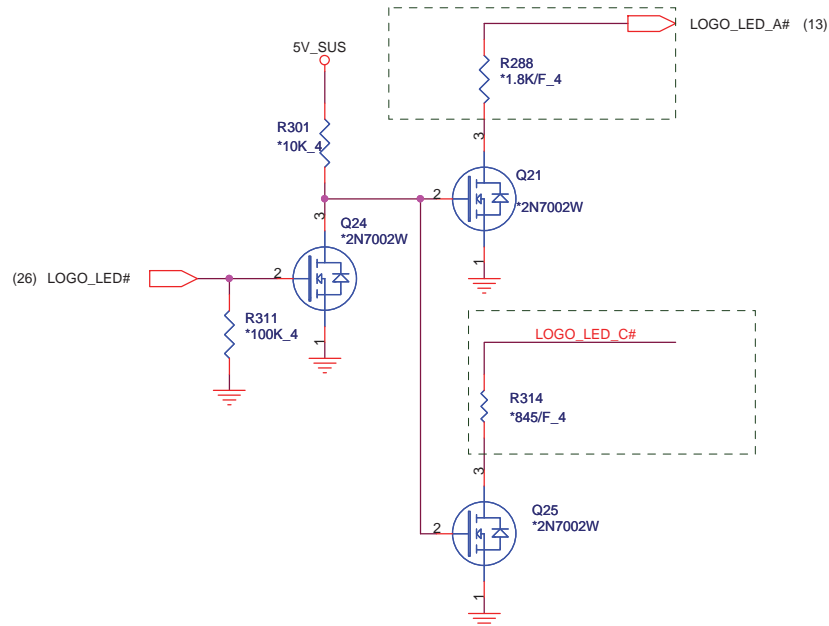
RFID



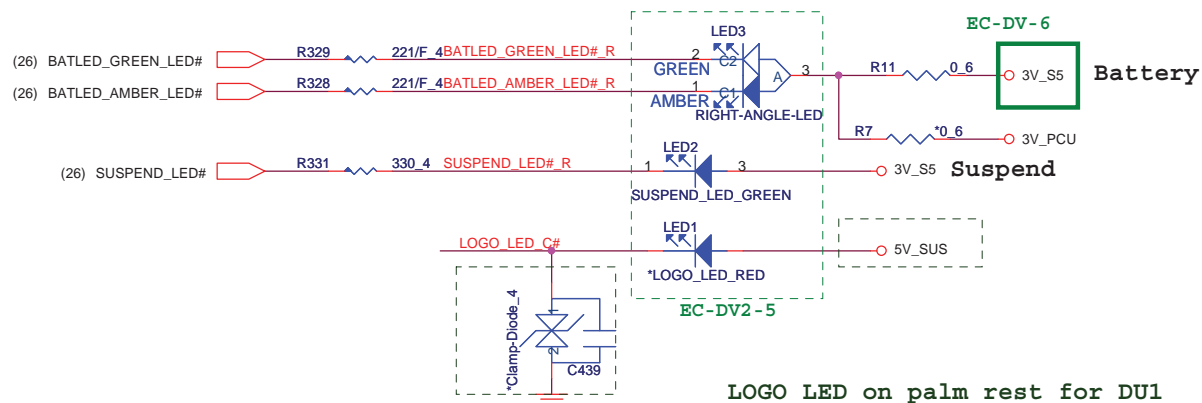
EC-SIT-6

LED Driver

LOGO LED on panel cover for DU1

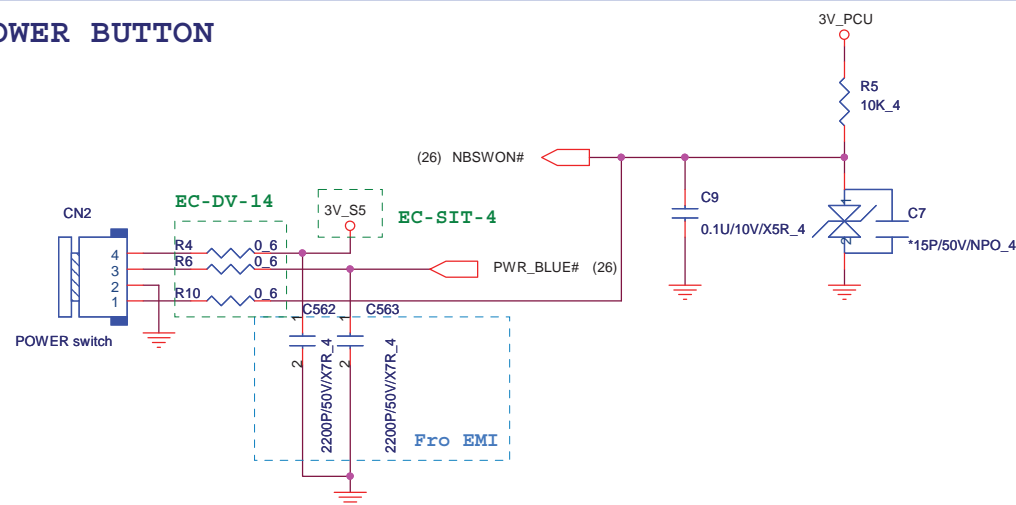


+3V (4,5,6,7,8,9,10,11,12,13,14,15,16,17,19,20,21,23,24,26,27,30,32,33,35,36)
 3V_PCU (8,10,13,14,15,18,26,29,30,36)
 3V_S5 (8,9,10,11,12,18,20,23,26,36)
 5V_SUS (13,32,34,35,36)



LOGO LED on palm rest for DU1

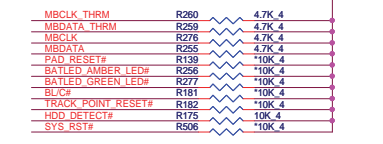
POWER BUTTON

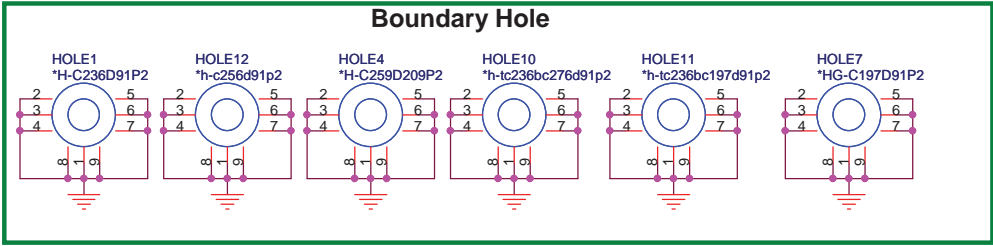
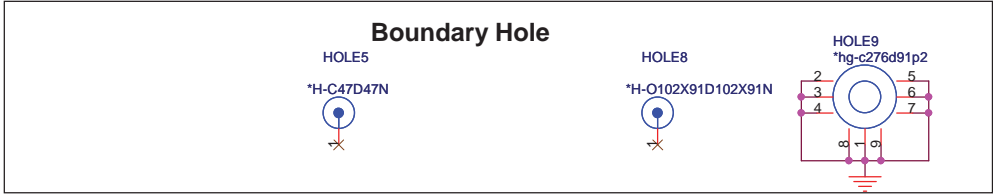
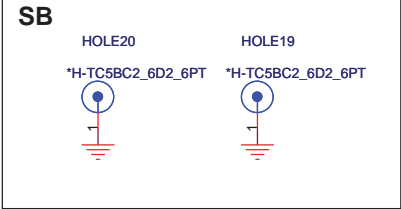
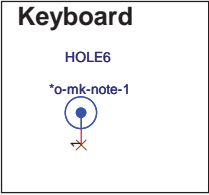
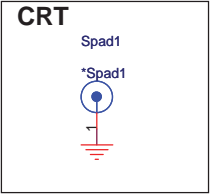
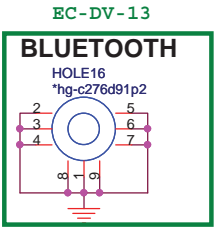
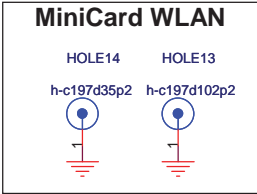
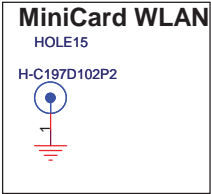
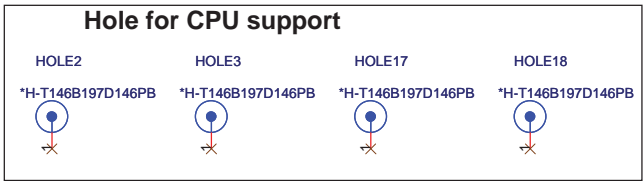


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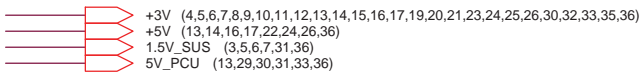
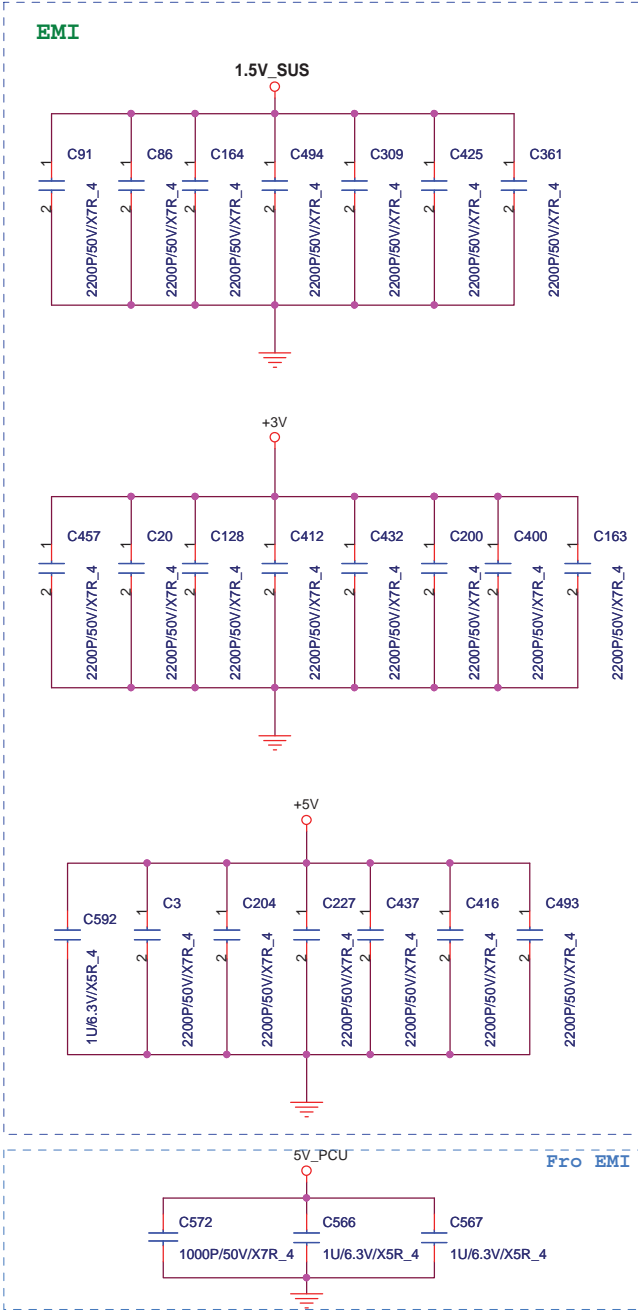
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Size	Document Number	Rev
	SW/LED/RFID_EEPROM	1A
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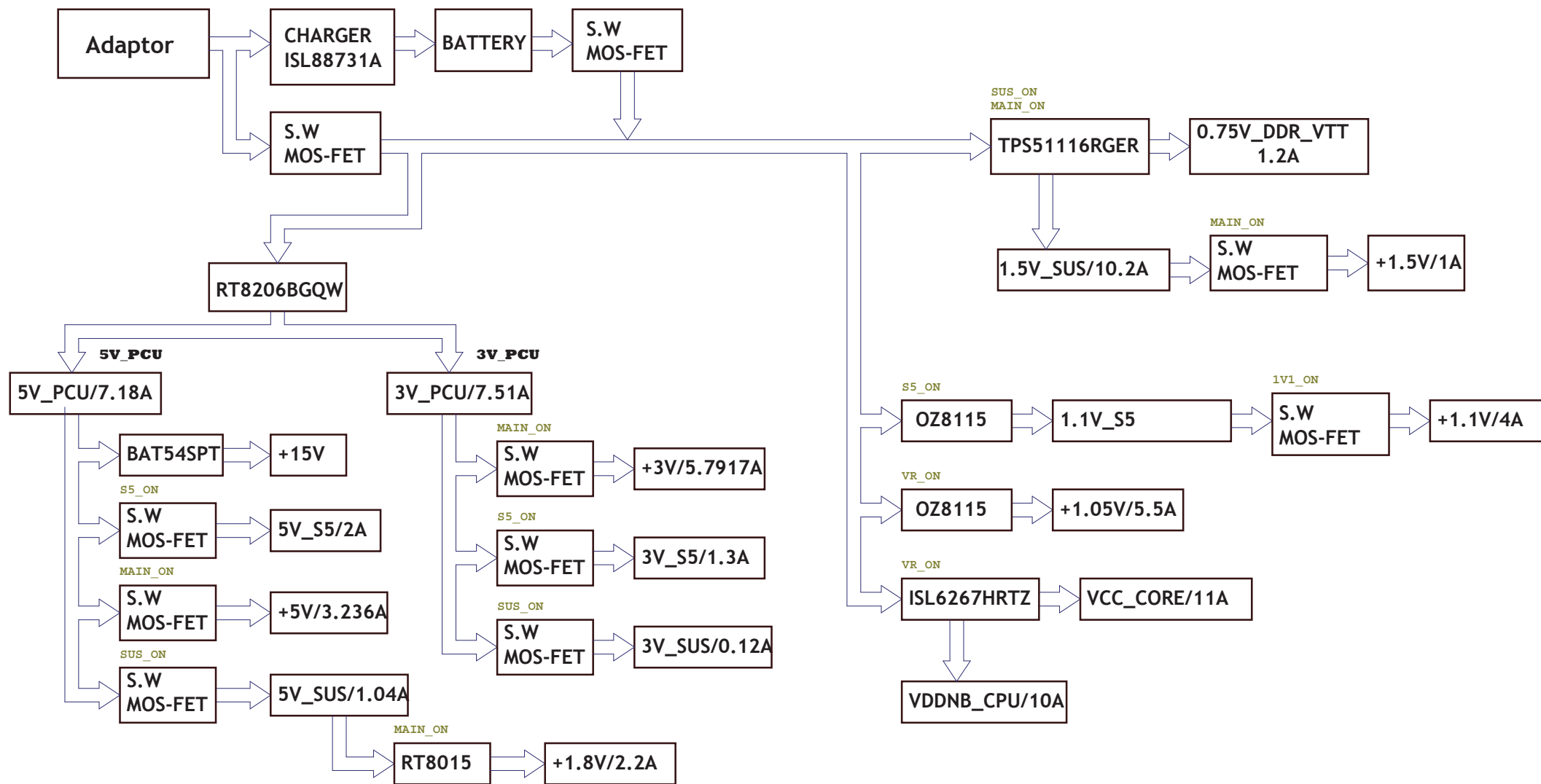


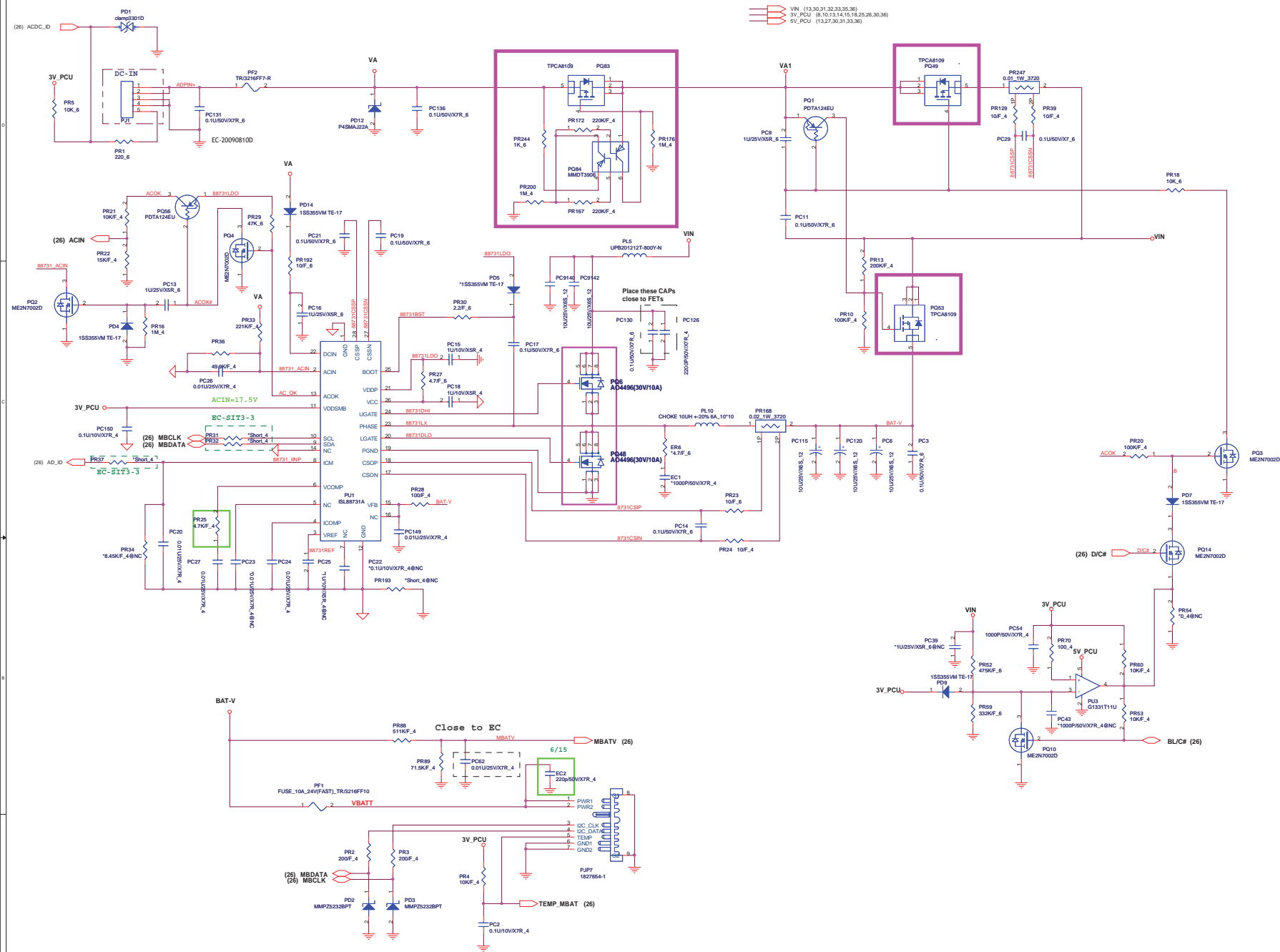
EC-DV-13

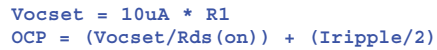


Brazos SYSTEM POWER BLOCK DIAGRAM

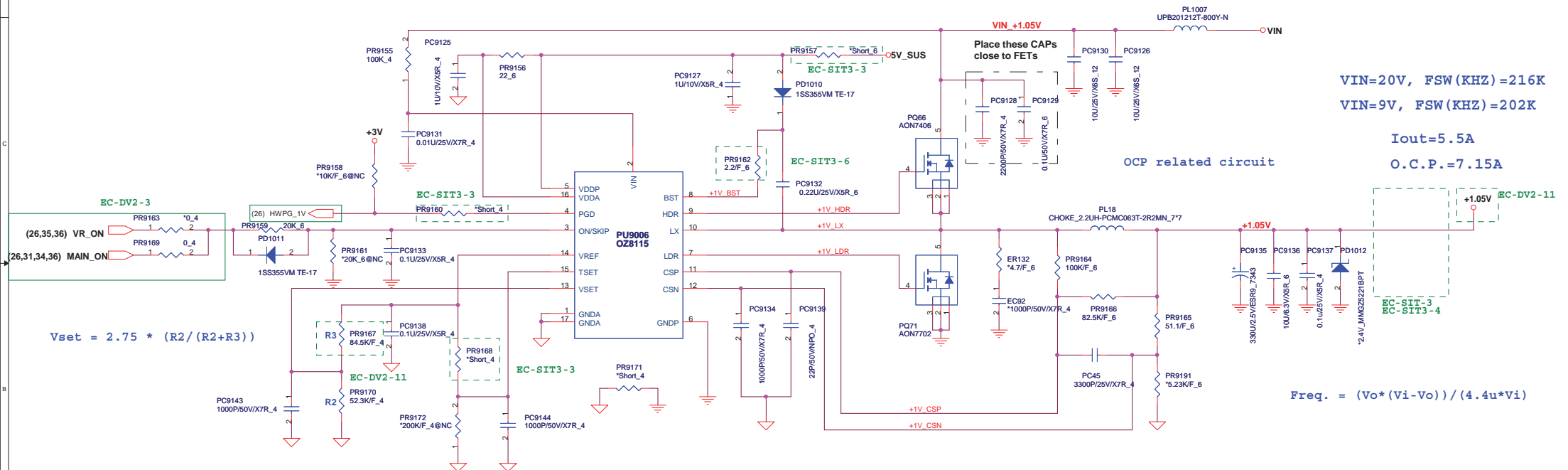
28







(13,29,30,31,33,35,36) VIN
(3,5,36) +1.05V
(13,25,34,35,36) 5V_SUS
(4,5,6,7,8,9,10,11,12,13,14,15,16,17,19,20,21,23,24,25,26,27,30,33,35,36) +3V



Quanta Computer Inc.
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	+1.05V (OZ8115)	1A
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This page is different AMD Nile

VIN=20V, FSW(KHZ)=236K

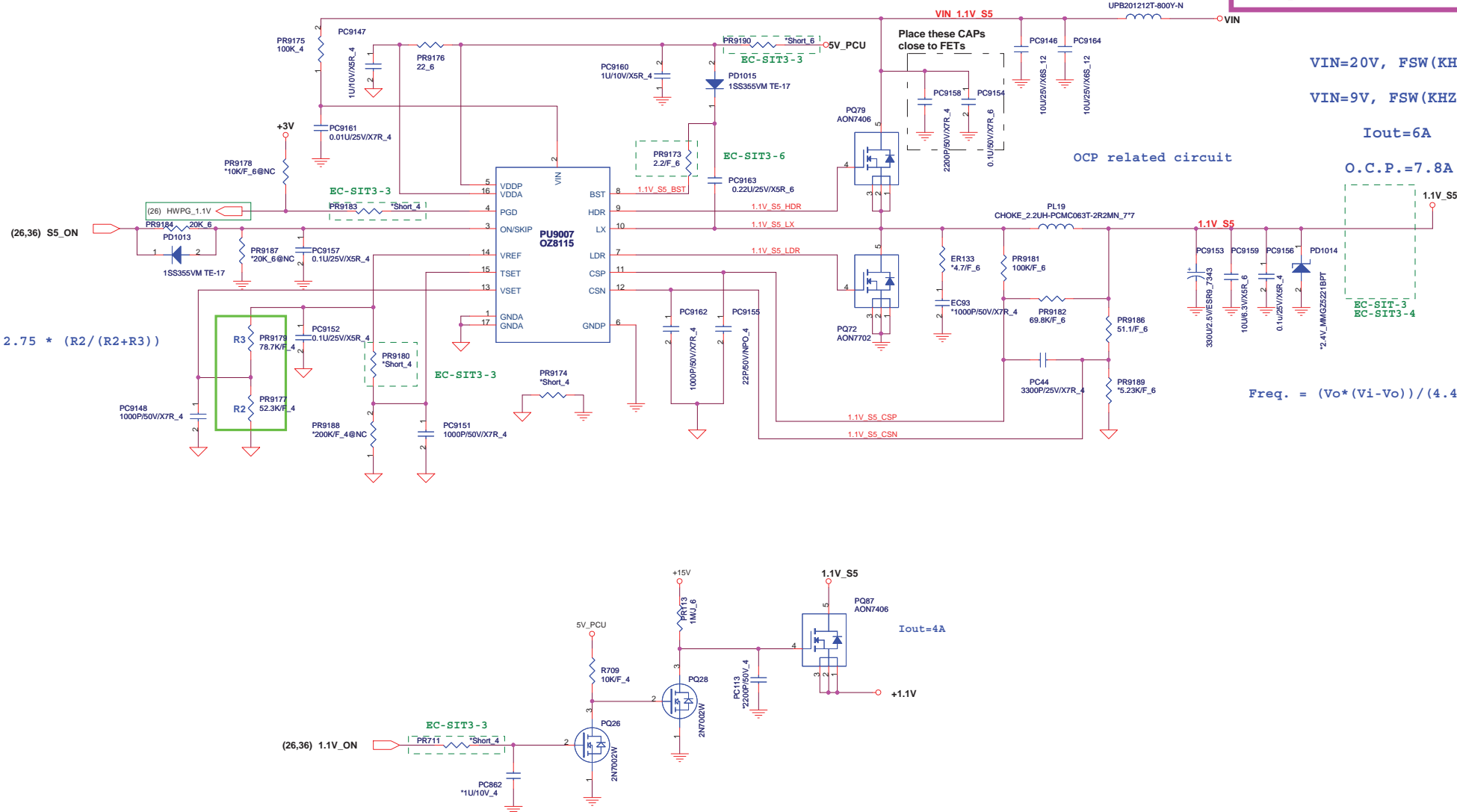
VIN=9V, FSW(KHZ)=219K

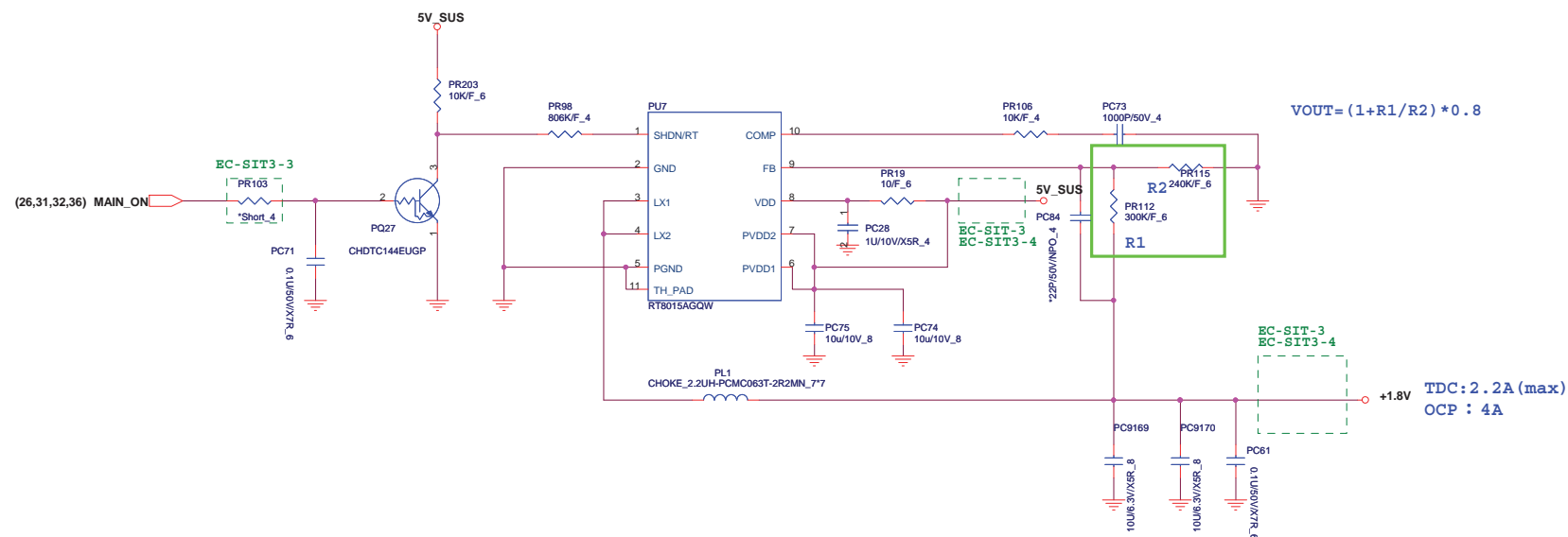
Iout=6A

O.C.P.=7.8A

Freq. = (Vo*(Vi-Vo))/(4.4u*Vi)

$$V_{set} = 2.75 * (R2 / (R2 + R3))$$



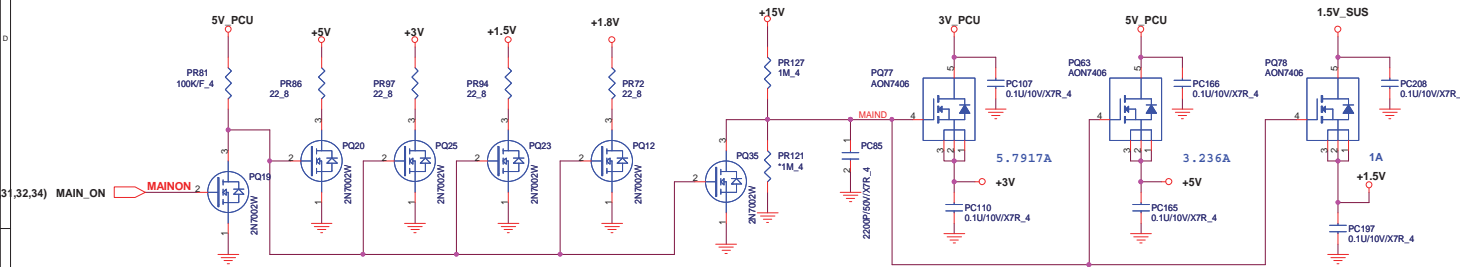


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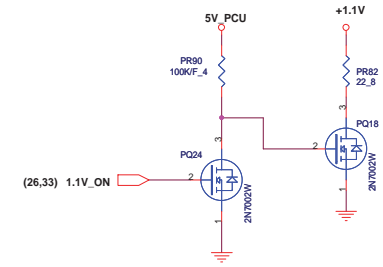
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	+1.8V (RT8015AGQW)	1A
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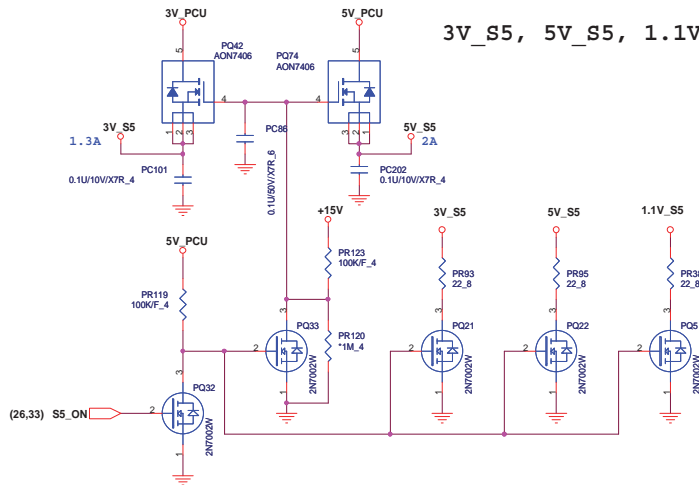
+3V, +5V, +1.8V, +1.5V



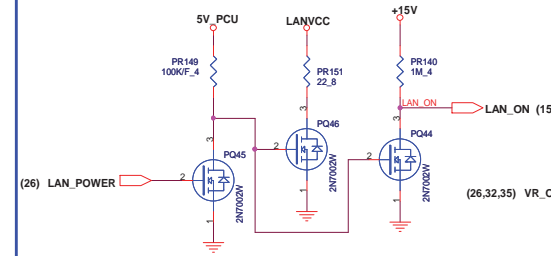
+1.1V



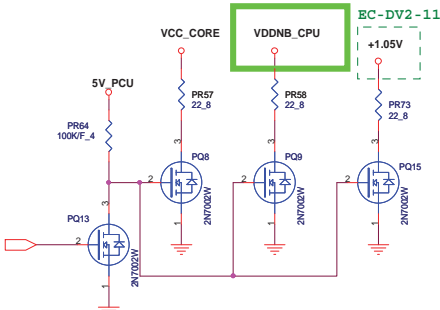
3V_S5, 5V_S5, 1.1V_S5



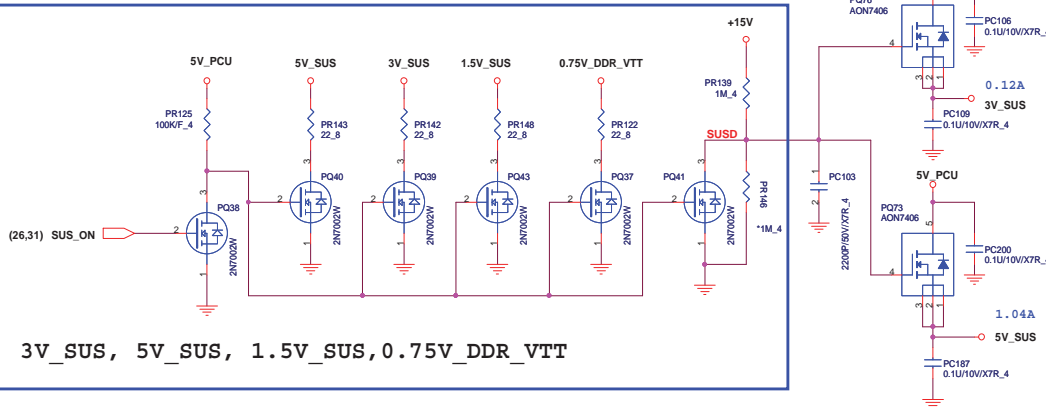
LANVCC



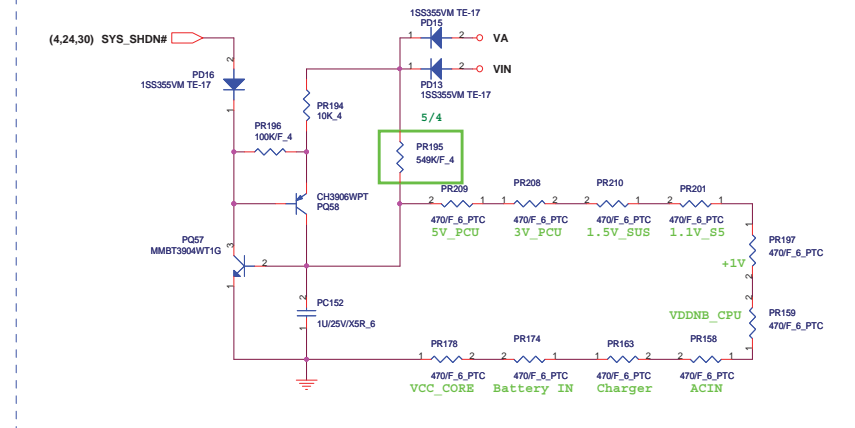
VCC_CORE, VDDNB_CPU, +1V



3V_SUS, 5V_SUS, 1.5V_SUS, 0.75V_DDR_VTT



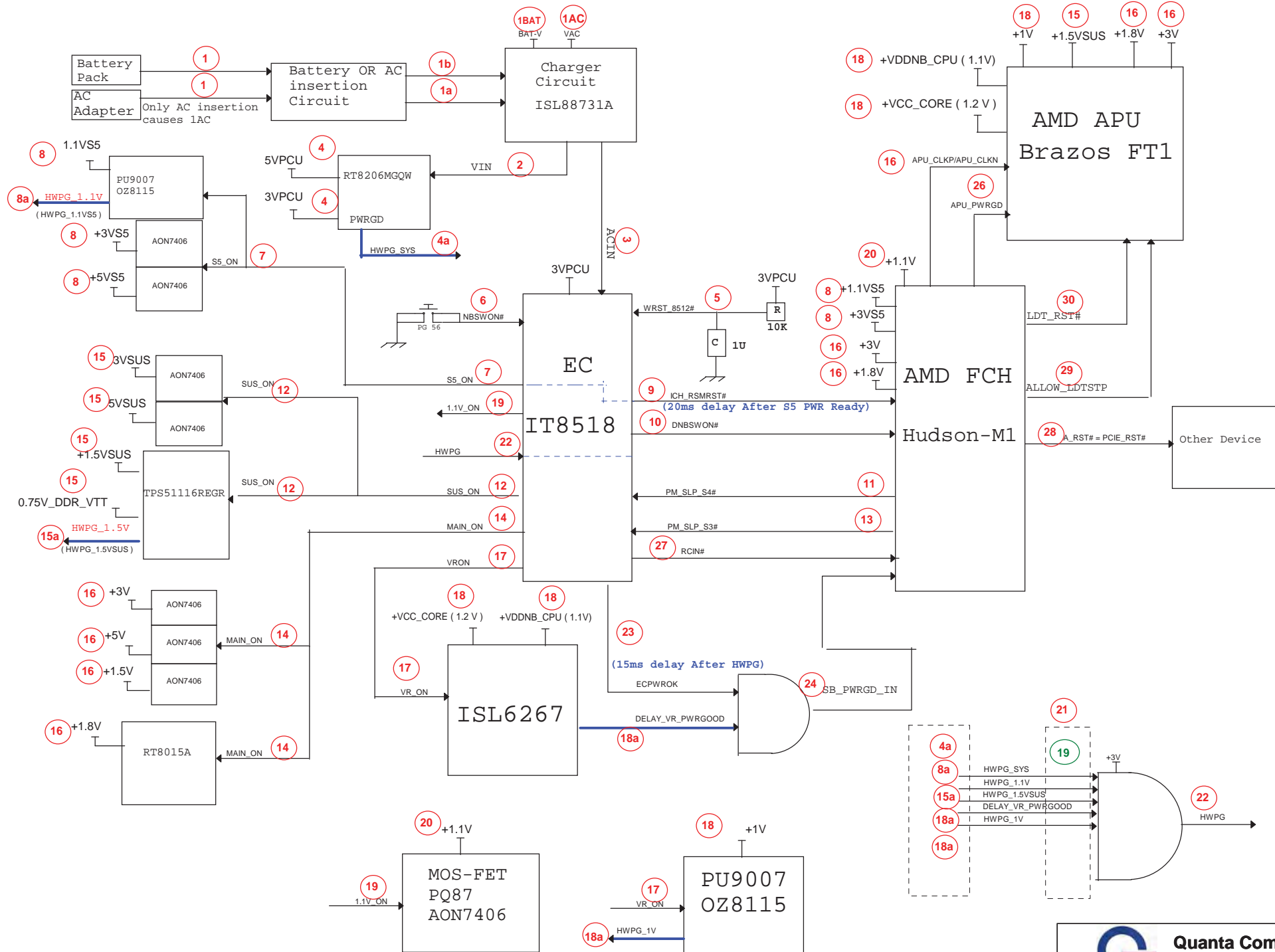
(4,24,30) SYS_SHDN#



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	Discharge	1A
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Revision History

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Revision	Date	Phase	Change List	Release Schematic Date	Release Gerber File Date
A1A		DV	Initial release		

Schematic Value Explanation Description :

RESISTOR

Value	F	4	6	8	12	1210	*	Description
*1K/F_4	1%	0402 (1005)					DE POP	1K ohm 1% SMD 0402 package and DE POP
1K_6	5%		0603 (1608)				POP	1K ohm 5% SMD 0603 package and POP
1K_8	5%			0805 (2125)			POP	1K ohm 5% SMD 0805 package and POP
1K_12	5%				1206 (3216)		POP	1K ohm 5% SMD 1206 package and POP
1K_1210	5%					1210 (3225)	POP	1K ohm 5% SMD 1210 package and POP


CAPACITOR

Value	Voltage	Material	6				*	Description
*0.1U/10V/X5R_4	10V	X5R	0402 (1005)				DE POP	0.1UF 10V X5R SMD 0402 package DE POP
1U/25V/X7R_6	25V	X7R	0603 (1608)				POP	0.1UF 25V X7R SMD 0603 package POP

EC #	Page	Date	Part Affected	Description
EC-DV-01 (AMD Suggest)	11	10/08/01	C1094	Change value from 0.1U to 1U
	11	10/08/01	L60	Add a Inductor and connect to VDDPL_1.1V
	11	10/08/01	C1073	Change value from 4.7U to 2.2U
	11	10/08/01		PCH NET"XDDXL_33_S" change power rail from 3V_S5 to +3V
	4	10/08/01	R728	Because Prochot# has been pull up +3V, delete one pull up resistor. Delete R728.
	8	10/08/01	C1042, C1045, C1043, C1044	Change value from 18P to 22P.
	10	10/08/01	U44	Change SPI ROM input and output with PCH.
	4	10/08/01	R92	"LTDPO_APD"add pull down resistor
	4	10/08/01	R739,R740	Delete R739, R740
	14	10/08/01	R344,R349	"VGA_DAC_SDA and VGA_DAC_SCL" add pull up 4.7k resistor from +3V to +5V power rail.
	14	10/08/01	R100,R102,R104,R107,R109,R111,R118,R120	Change resistor value to 499 ohm
	14	10/08/01	Q13	Change Q13 power rail from +3X to +5V
	03	10/08/01	C871, C19	Add C871 and C19
	06	10/08/01	R123,R163	Change value from 10k to 1K
	11	10/08/01		Change "VDDIO_AZ" from +1.5V_SUS to +3V
	9	10/08/01	R324	Change value from 4.7K to 10K
	9	10/08/01	R324	USBOC1# and USBOC2# change pull up voltage from 3V_SUS to 3V_S5
EC-DV-02	8 9 10 26	10/08/02	C376,C381 C382, C370 C375	Add RF tesm suggest
EC-DV-03	9	10/08/02	RP12	Change footprint type for layout
EC-DV-04	26	10/08/02	U15	Change EC from IT8502E to IT8518
EC-DV-05	26	10/08/02	R192, R195	To prevent EC leakage issue
EC-DV-06	25	10/08/02		Change battery LED power rail from 3V_PCU to 3V_S5
EC-DV-07	26	10/08/02	R96,Q31	Fro EC suggest, change power LED control singnal from low active to high active.
EC-DV-08	14 23	10/08/02		Celete duplicate net.
EC-DV-09	14	10/08/02		Delete GND net of pin3 from U4 and U6
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EC #	Page	Date	Part Affected	Description
EC-DV2-1	13	10/08/24	CN27,R342,R348	Because LVDS CONN still combine, delete USB component.
EC-DV2-2	9	10/08/24	R937,R938,R849,R851	EPROM setteing from SPI to LPC ROM.
EC-DV2-3	32	10/08/24	PR9153,PR9169	AMD Suggest it to meet power sequence.
EC-DV2-4	3,8	10/08/24	C109,C110	AMD Suggest that use APU PCIe interface to link LAN to enhance its performance.
EC-DV2-5	25	10/08/24	LED1,LED2,LED3	For ID design. Delete LED1 ,add LED2 and LED3
EC-DV2-6	30	10/08/24	PR221	For 5V_PCU OCP
EC-DV2-7	30	10/08/24	PR215	For 3V_PCU OCP
EC-DV2-8	35	10/08/24	PR277	For VDDNB_CPU OCP
EC-DV2-9	35	10/08/24	PR267	For VCC_CORE OCP
EC-DV2-10	35	10/08/24	PL9	For CPU Ripple voltage
EC-DV2-11	32	10/08/24	PR9167	For AMD request change +1V to +1.05V
EC-DV2-12	31	10/08/24	PC169	For 1.5V_SUS output ripple voltage
EC-DV2-13	35	10/08/24	PC231,PC212,PR246,PC222,PC242, PC228,PC254,PR270,PR267	Chip vendor suggest.
EC-DV2-14	26	10/08/24	D7006,D7007,D7008,D7009,R508,R509,R510,R511	Mount Diode for easy debug


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EC list for DV2


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EC #	Page	Date	Part Affected	Description
EC-SIT-1	35	10/09/17	PU9	Chip vendor(Intersil) suggest that some power chip pin change from +5V to 5V_SUS to prevent 5V leakage current.
EC-SIT-2	31~34	10/09/17	PJP2,PJP6,PJP12,PJP13,PJP14,PJP15, PJP16,PJP17,PJP18	Power jump PCB footprint change from open type to short type
EC-SIT-3	26	10/09/17	R512	For S3/S4/S5 leaksge issue from 20mA to 5mA. This pin is re-define from output to input. But EC don't use this pin. Resever it.
EC-SIT-4	25	10/09/17	CN2 pin4	Power LED plan change from 3VPCU to 3V_S5 to prevent LED flight one tie issue during plug adapter. Fix ECR72256 from Vendor(ITE) suggestion
EC-SIT-5	26	10/09/17	Q31, R194	Power LED enable lever from high active to low active. Delete Q31, add R194. Fix ECR72256 from EC team member request
EC-SIT-6	25 13	10/09/17	Q24,Q21,Q25,R311,R301,R288,R314 C568	Because MK2B don't support Logo LED function, delete them. Delete Q24,Q21,Q25,R311,R301,R288,R314,C568
EC-SIT-7	13	10/09/17	R12	Reserve R12(short pad) to prevent LCD short current verication.
EC-SIT-8	6 7	10/09/17	C7274, C7275	Change DDR DIMM Module VREF_CA and VREF_DQ reference power.
EC-SIT-9	15	10/09/17		Because LAN interface cahnge FCH to APU, change its reset signal from PCIE_RST# to A_RST#.
EC-SIT-10	19	10/09/17	Y7, C257, C258,R472,R459	Cardreader clock input from 12MHZ crystal to FCH internal clock.
EC-SIT-11	5	10/09/17	C927, R9796,C934	Delete C927,C934 for layout. Add R796 for AMD suggest.
EC-SIT-12	8	10/09/17	C1111	Reserve a capacitor for RF team request.
EC-SIT-13	11	10/09/17	L48,L50,L52	AMD suggest. Change its current sustain from 1.5A to 5A.
EC-SIT-14	10	10/09/17	R881,R884,R885,R877,R878,C1058	Because BIOS and EC use the same ROM, delete them from BOM.
EC-SIT-15	8	10/09/27	C1043,C1044	Crystal vendor suggest(TXC and Hosonic)that chage fromm 22P to 10P to get good sin=gnal
EC-SIT-16	26	10/10/05	R194	Change value from 0 ohm to 68 ohm to meet ITE8518 current limit issue.

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EC #	Page	Date	Part Affected	Description
EC-SIT3-1	15,16,18	10/10/28	RV1, RV3, RV9,RV10,RV11,C503,C504	Add ESDprotect component for ESD request.
EC-SIT3-2	4	10/10/28	R739,R740,R741,R742,T116,T179	Delete unnecessary component R739,R740,R741,R742. Add T116 ,T179.
EC-SIT3-3	3	10/10/28	R718	change to short pad
	4		R743,R745,R750,R788,R789,R791,R790,R793,R792,R795,R794,R730,R725,R731	
	5		R785,R786	
	6		R124	
	7		R158	
	8		R809,R810,R811,R812	
	9		R825,R827,R831	
	11		R890,R891,R893,R894	
	13		R342,R348,R347,R351,R352	
	14		R119,R117,R112,R110,R108,R105,R103,R101	
	15		R177,R197,R208,R299	
	16		R477,R306,R323	
	18		R132,R133,R141,R142	
	19		R470,R464,R450,R472	
	20		R273,R252	
	21		R176,R253	
	23		R291,R293,R295	
	26		R508,R509,R510,R511	
	29		PR31,PR32,PR37	
	30		PR155,PR218,PR153,PR126,PR207,PR219,PR145,PR222	
	31		PR132,PR206,PR228,PR230,PR238,PR214,PR235,PR9157,PR9160,PR9168,PR9190,PR9183,PR9180,PR711,PR103,PR256,PR243	
	35		PR160,PR287,PR245,PR283,PR241	
EC-SIT3-4	5	10/10/28	R787,R796,R784	delete power jump
	17		R38,R72	
	20		R200	
	31		PJP12,PJP13,PJP6	
	32		PJP14,PJP15	
	33		PJP16,PJP17	
	34		PJP2,PJP18	
EC-SIT3-5	35	10/10/28	PR251,PR249	Change for PSI function
EC-SIT3-6	32,33	10/10/28	PR9162,PR9173	Change for switch phase voltage

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EC #	Page	Date	Part Affected	Description