

Genesis-1 Block Diagram

LGS-1 91.4RQ01.001

JULY. 18, 2011

PCB Layer Stackup

L1:Component
L2:GND
L3:Signal 1
L4:VCC
L5:Signal 2
L6:Signal 3
L7:VCC
L8:Signal 4
L9:GND
L10:Component

Battery Charger/Selector

BQ24760 75

INPUTS	OUTPUTS
VINT20	CHARGER_OUT12

System DC/DC

TPS51220ARSN 79

VINT20	VCC5M
	VCC3M

CPU DC/DC

VT1318M/VT1324S 80

VCC5M_OUT	VCCCPUCORE
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GMCH GFX CORE

VT1324S 81

VCC5M_OUT	VCCGFXCORE
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VCC1R5B

VT355FCX 86

VCC5M_OUT	VCC1R5B
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VCC0R675B

MAX1510 87

VCC1R35A

VT356FCX 88

VCC5M_OUT	VCC1R35A
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VCC1R35A	VCC0R675B
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VCC1R8B

BD9139 89

VCC5M_OUT	VCC1R8B
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VCC1R05AMT

VT356FCX 85

VCC5M_OUT	VCC1R05LAN
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VCC1R05B_VTT

VT356 84

VCC5M_OUT	VCC1R05B_VTT
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VCCSA

VT371 90

VCC5M_OUT	VCCSA
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<Core Design>

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Wistron Corporation

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Title

Block Diagram

Size
A3

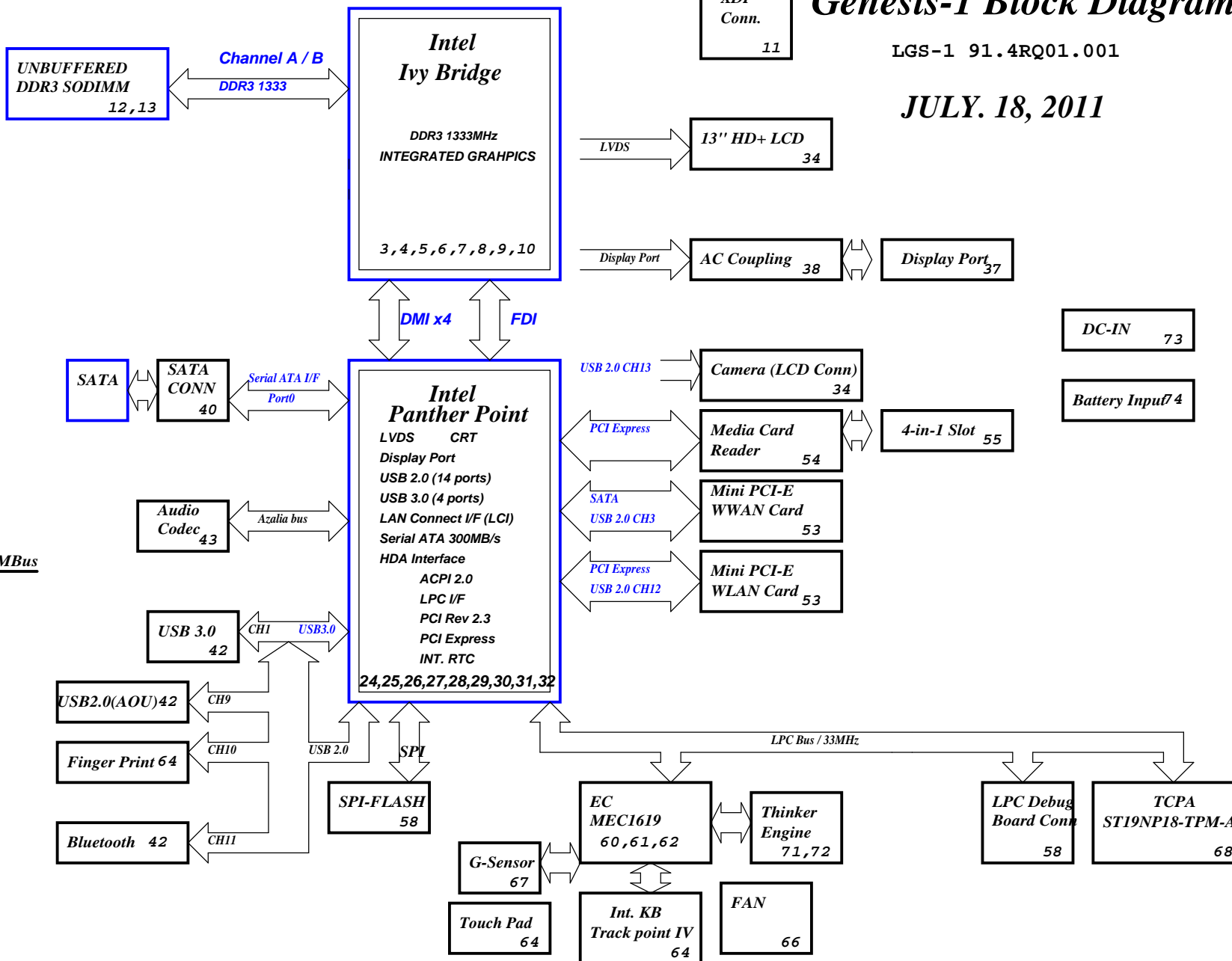
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RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210

The naming rule is
Capacitor type + value + rating + size + tolerance + material
SCD1U10V2MX-1
SC=> SMT Ceramic, TC=> POS cap or SP cap
D1U => 0.1uF
10V => the voltage rating is 10V
2=> 0402, 3=>0603, 5=>0805
M=>tolerance M, K, Z
X=> X7R/X5R, Y=> Y5V
-1 => symbol version, nonsense to EE characteristic

PLANAR_ID[3..0]

IBEXPEAK-M	39	38	48	49	Planar ID Version	Planar PCB Version
PLANAR_IDn	3	2	1	0		
	0	0	0	0	Genesis-1 initial	N/A
	0	0	0	1	FVT	N/A
	0	0	1	0	SIT	SC
	0	0	1	1		
	0	1	0	0		
	0	1	0	1		
	0	1	1	0		
	0	1	1	1		
	1	0	0	0		
	1	0	0	1		
	0	1	1	1		

WWW.AliSaler.Com

EC HISTORY

[illegible]

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Title	Author	Date	Page	Page	Page	Page	Page	Page	Page

Reference

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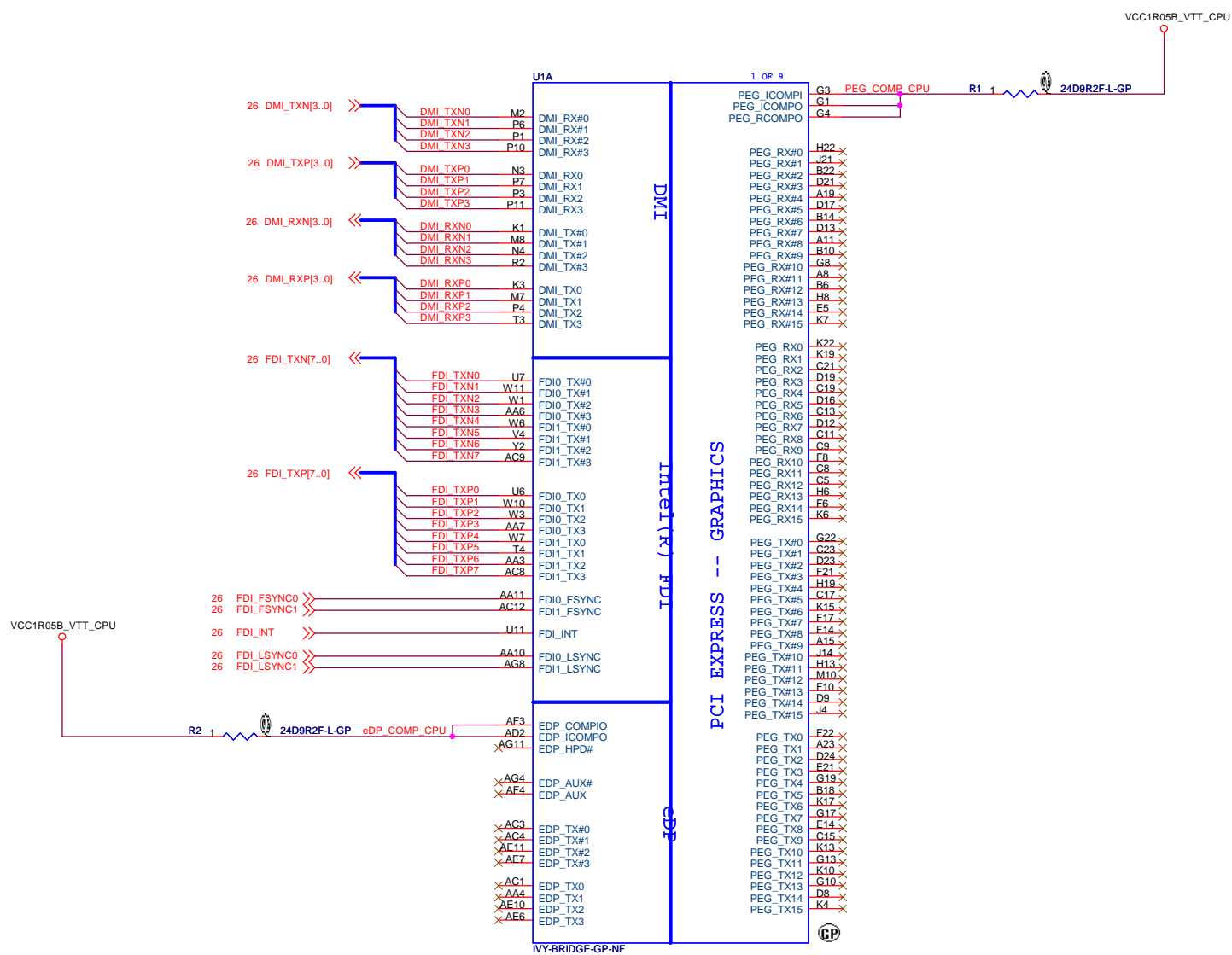
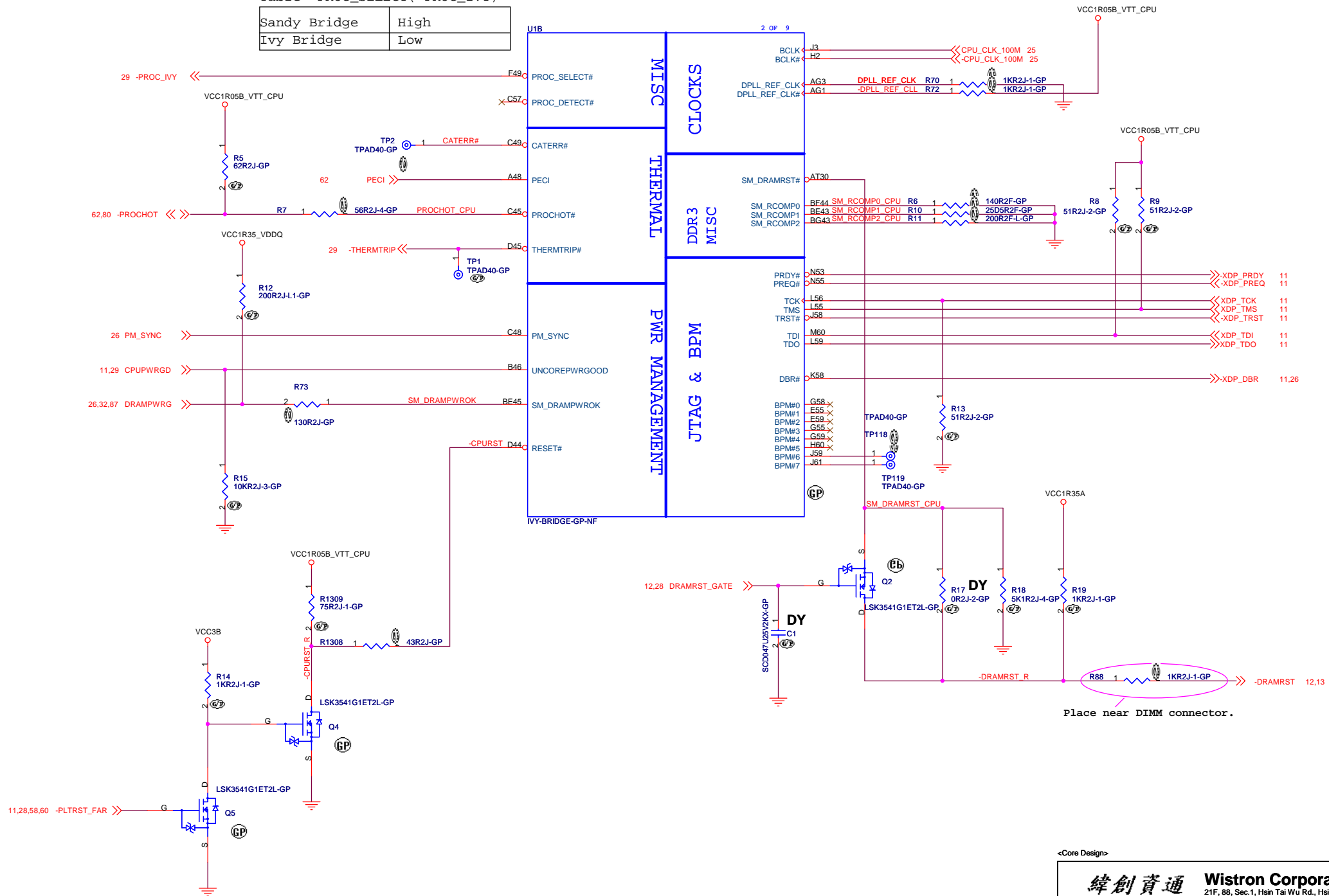


Table -PROC_SELECT(-PROC_IVY)

Sandy Bridge	High
Ivy Bridge	Low



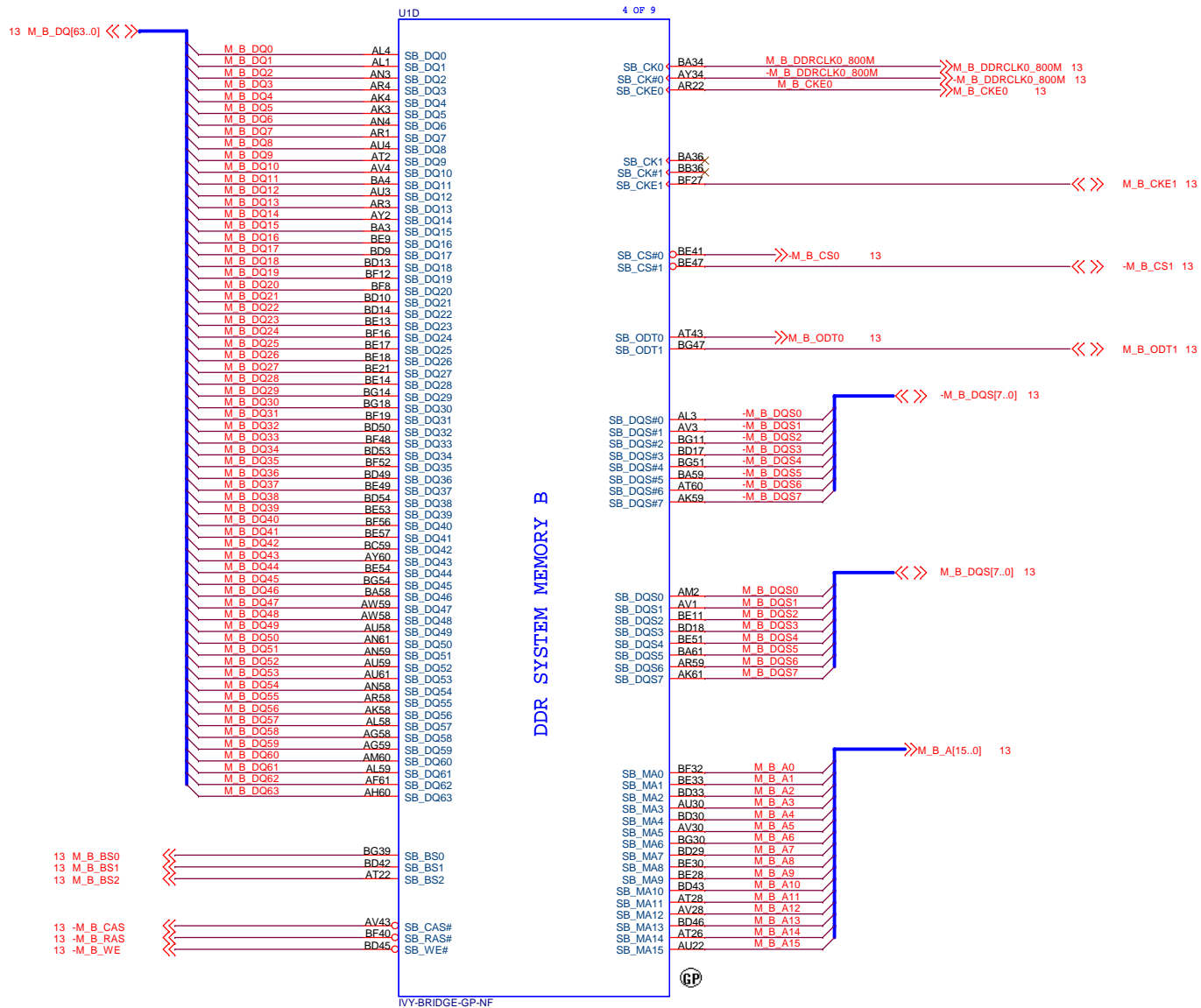
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Title CPU(2/8):CLK/MISC/JTAG

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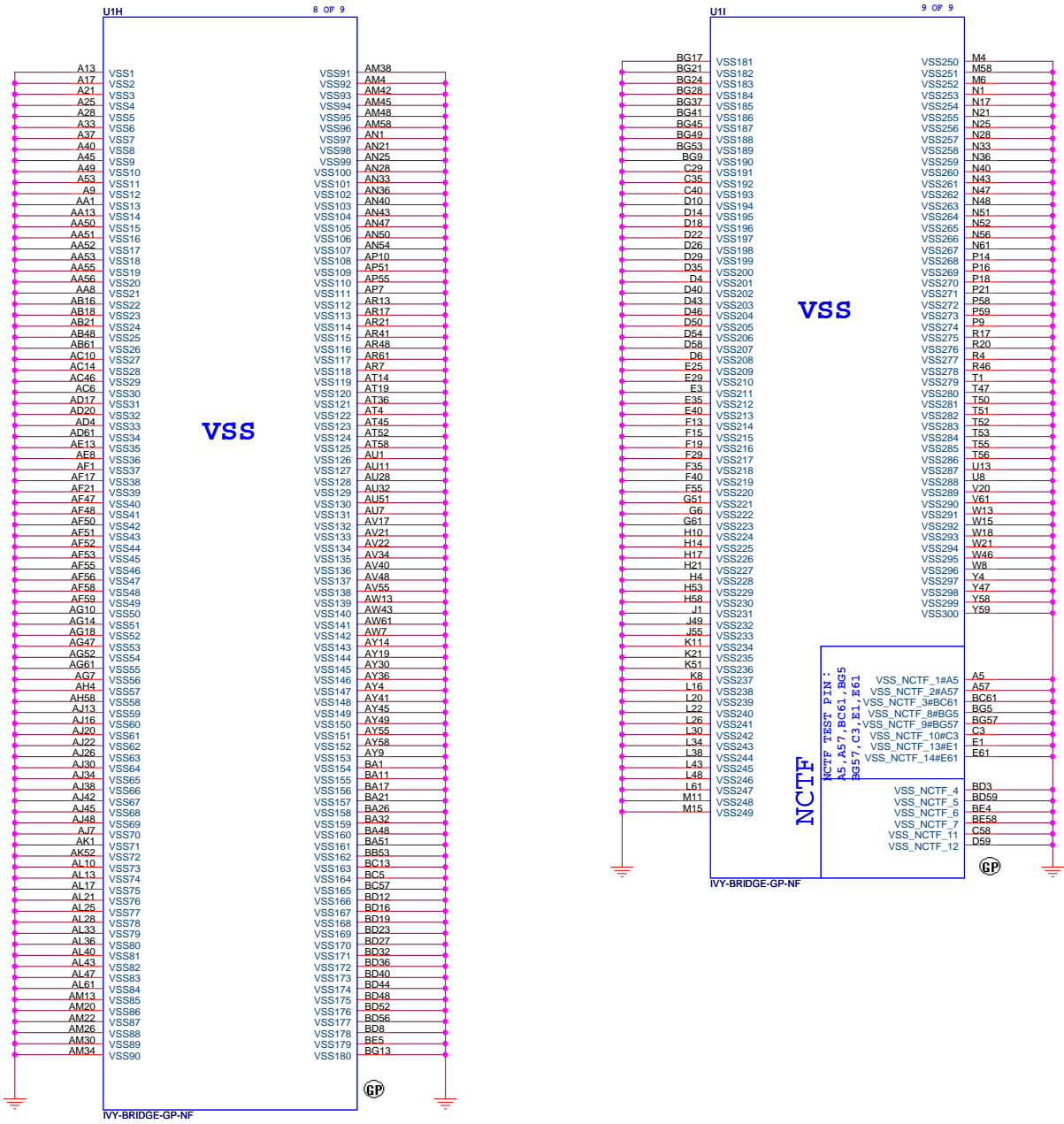


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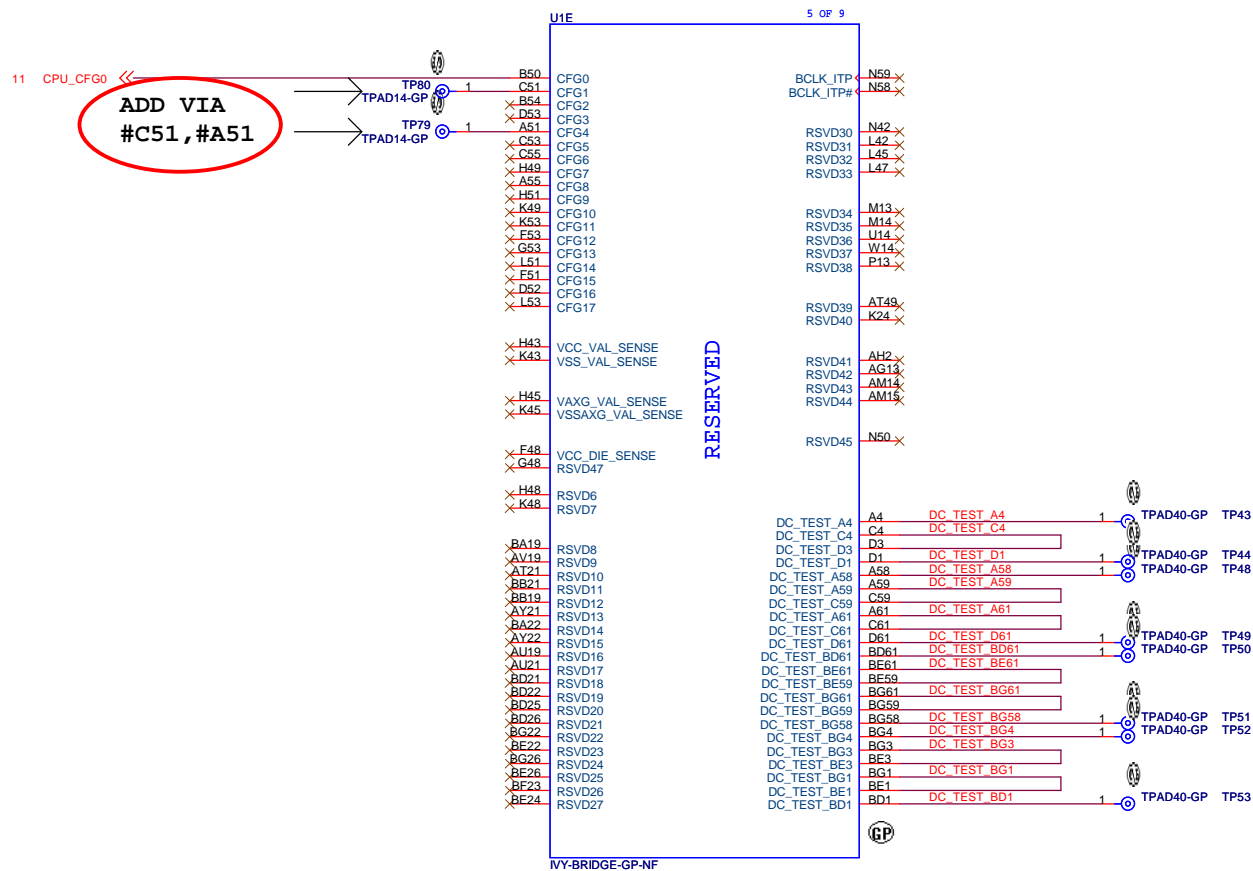
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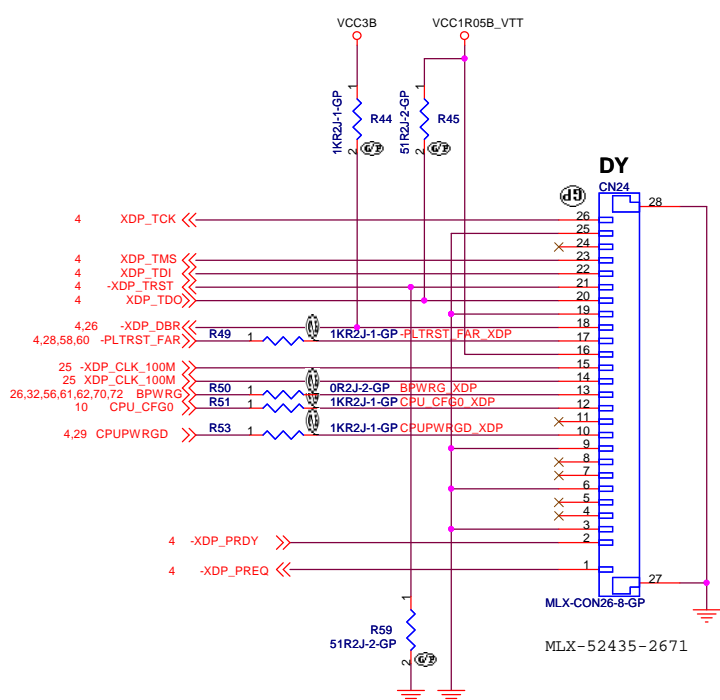
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CPU(8/8):CFG/Reserved		
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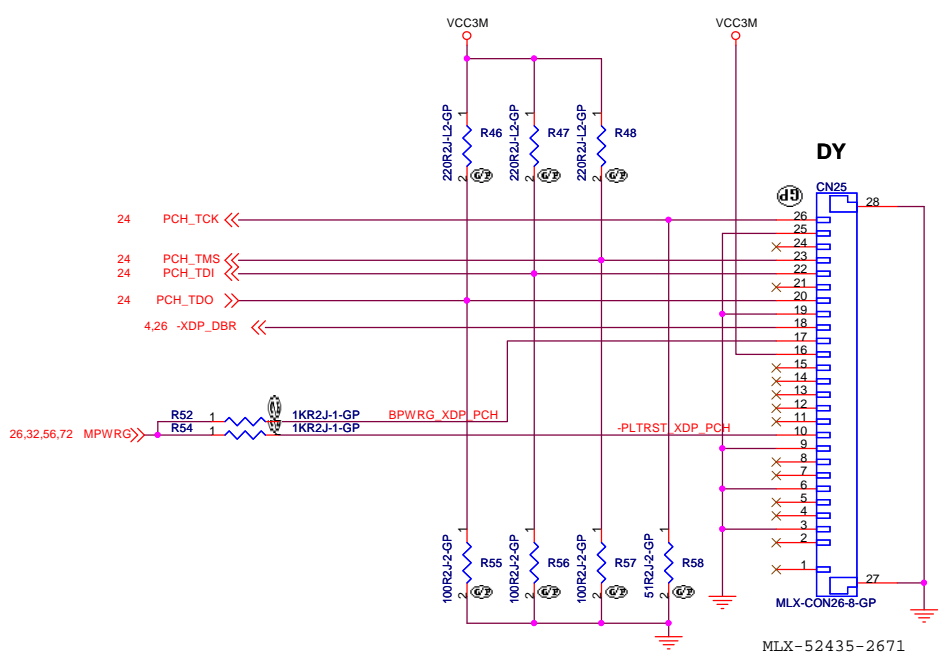


DEBUG Interface for Processor.

XDP1 NOTE:"ASM" FOR PDV/SDV ONLY

		ENABLE	DISABLE
TDO	R45	ASM	DY
TRST#	R59	ASM	ASM
DBRST#	R44	ASM	ASM
RESET#	R49	ASM	DY
CFG0	R51	ASM	DY
PWRGD	R53	ASM	DY
BPWRG	R50	ASM	DY
	CN24	ASM	DY

PDV Logic

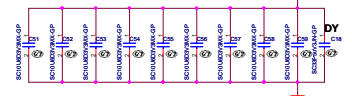
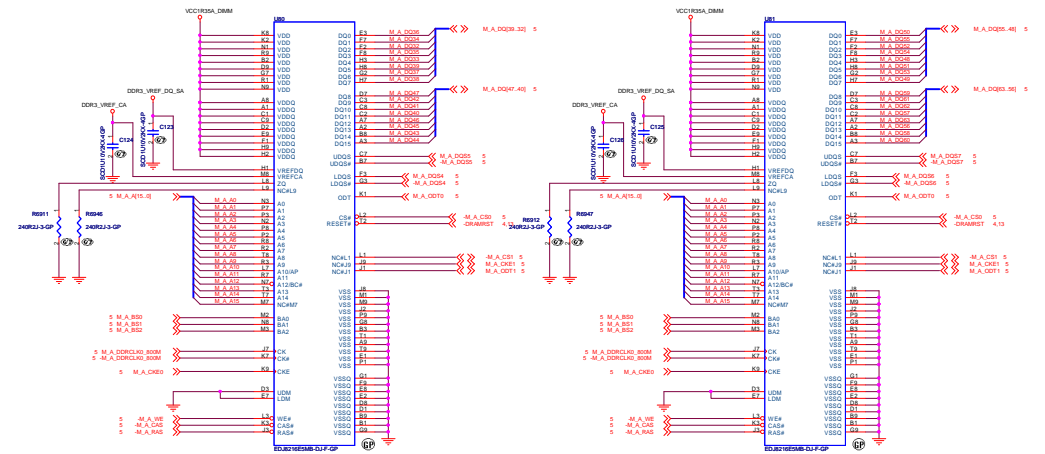
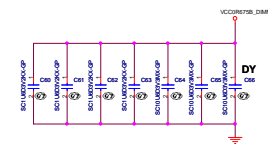
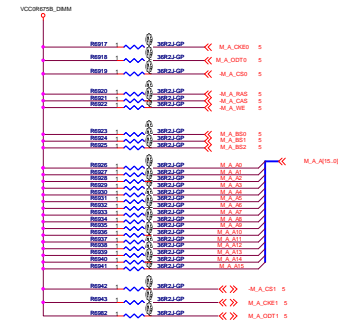


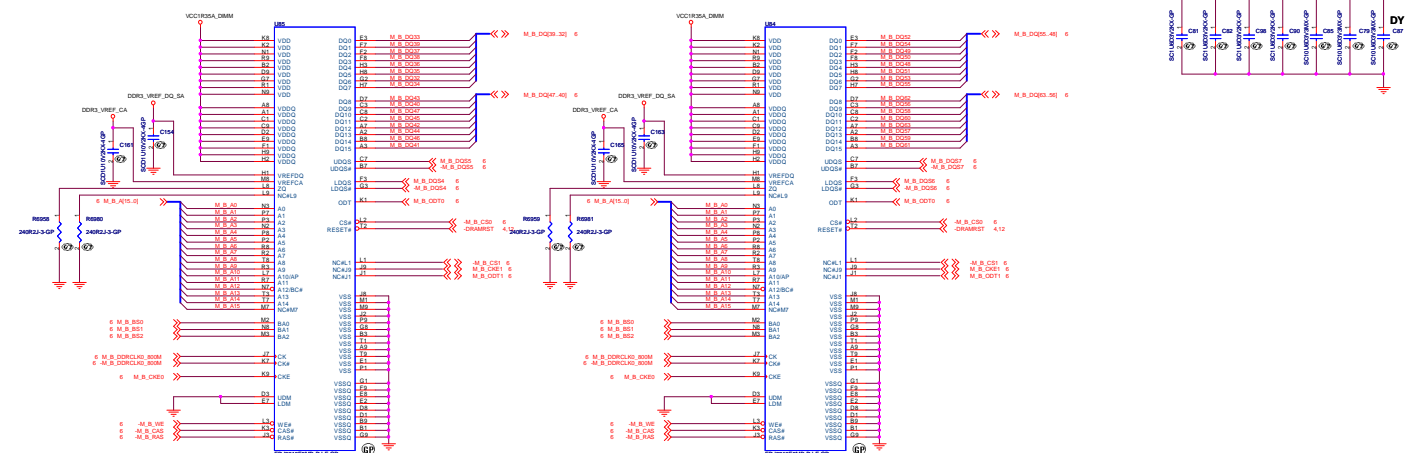
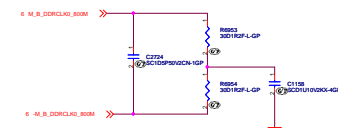
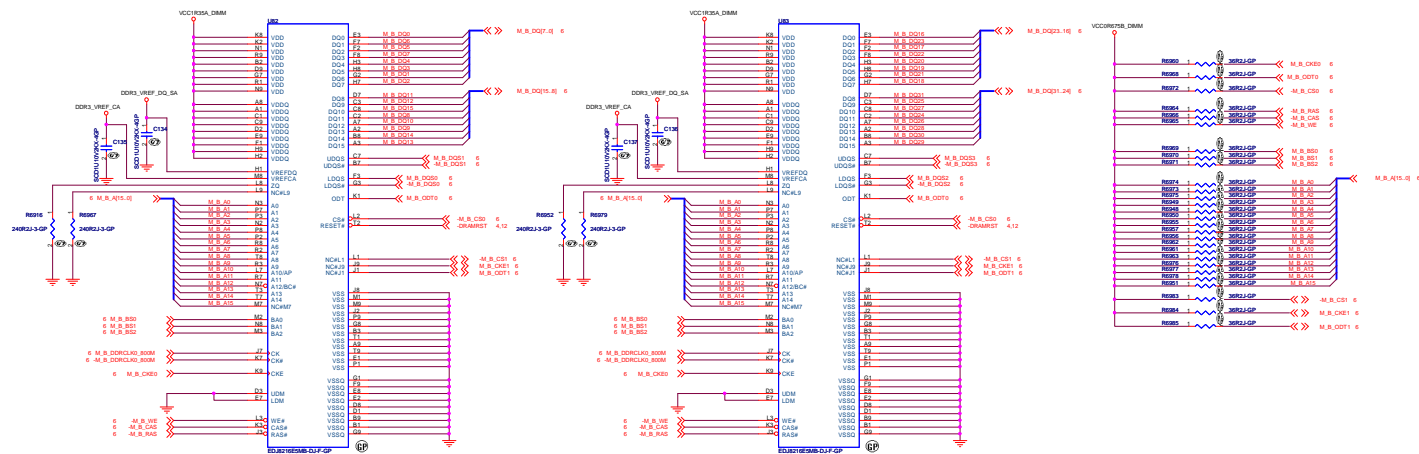
DEBUG Interface for PCH.

XDP2 NOTE:"ASM" FOR PDV/SDV ONLY

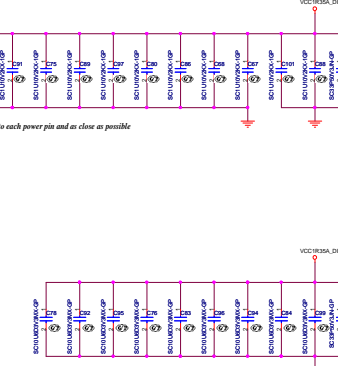
		ENABLE	DISABLE
TDO	R46	220	DY
	R55	100	DY
TMS	R48	220	DY
	R57	100	DY
TDI	R47	220	DY
	R56	100	DY
TCK	R58	51	51
MPWRG	R52	ASM	DY
	R54	ASM	DY
	CN25	ASM	DY

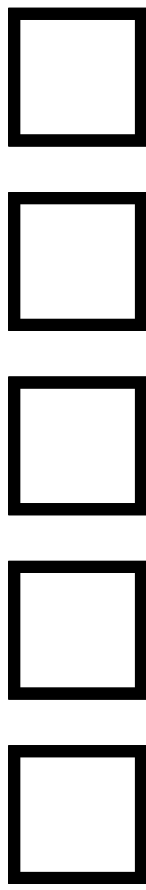
PDV Logic





Place one cap to each power pin and as close as possible





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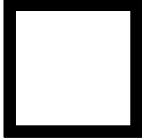
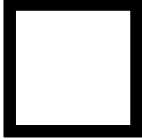
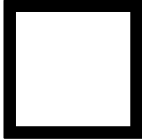
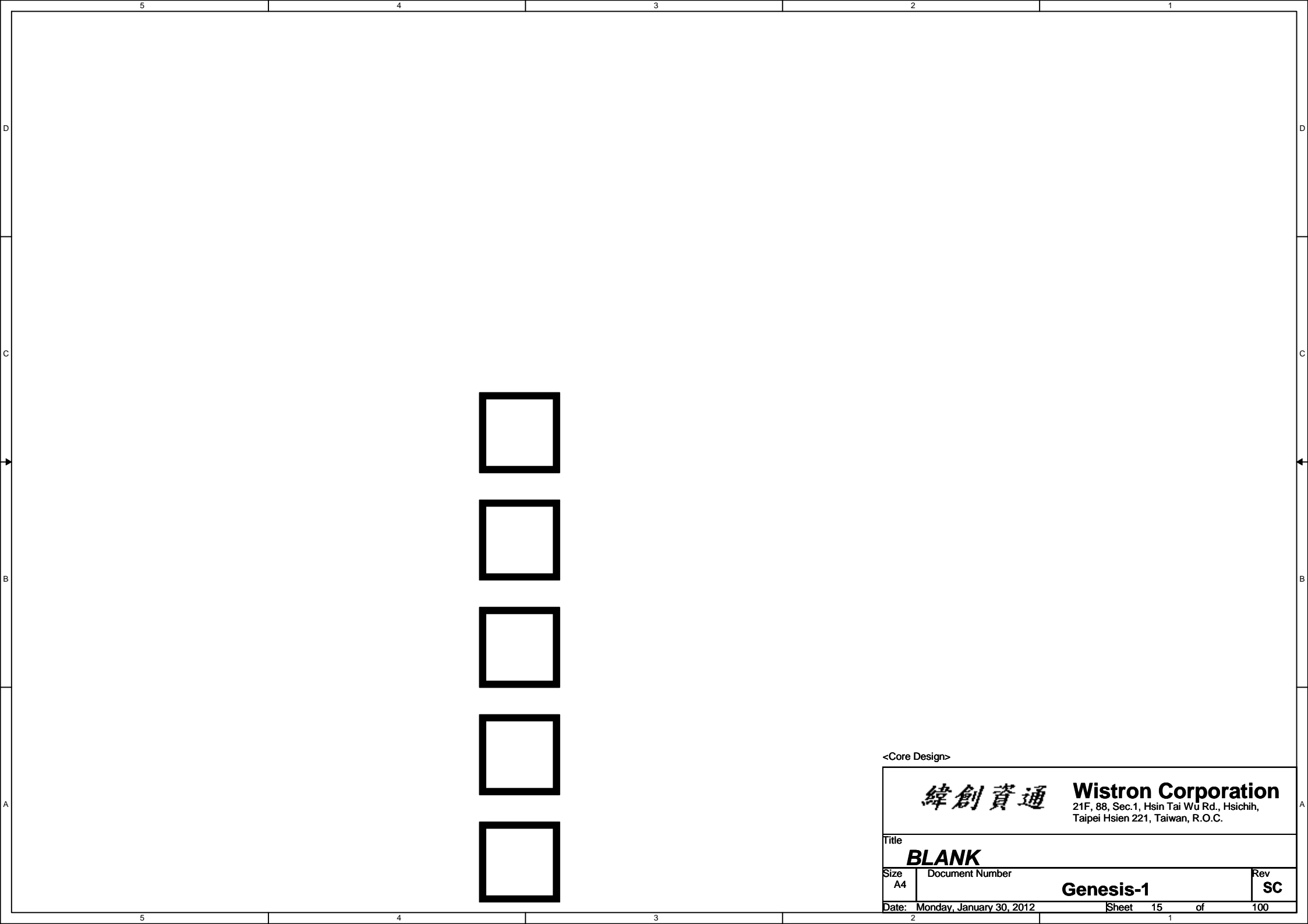
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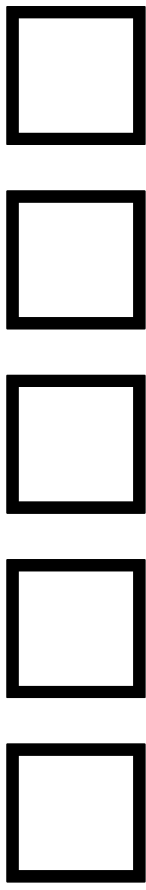
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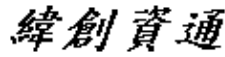
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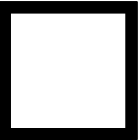
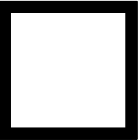
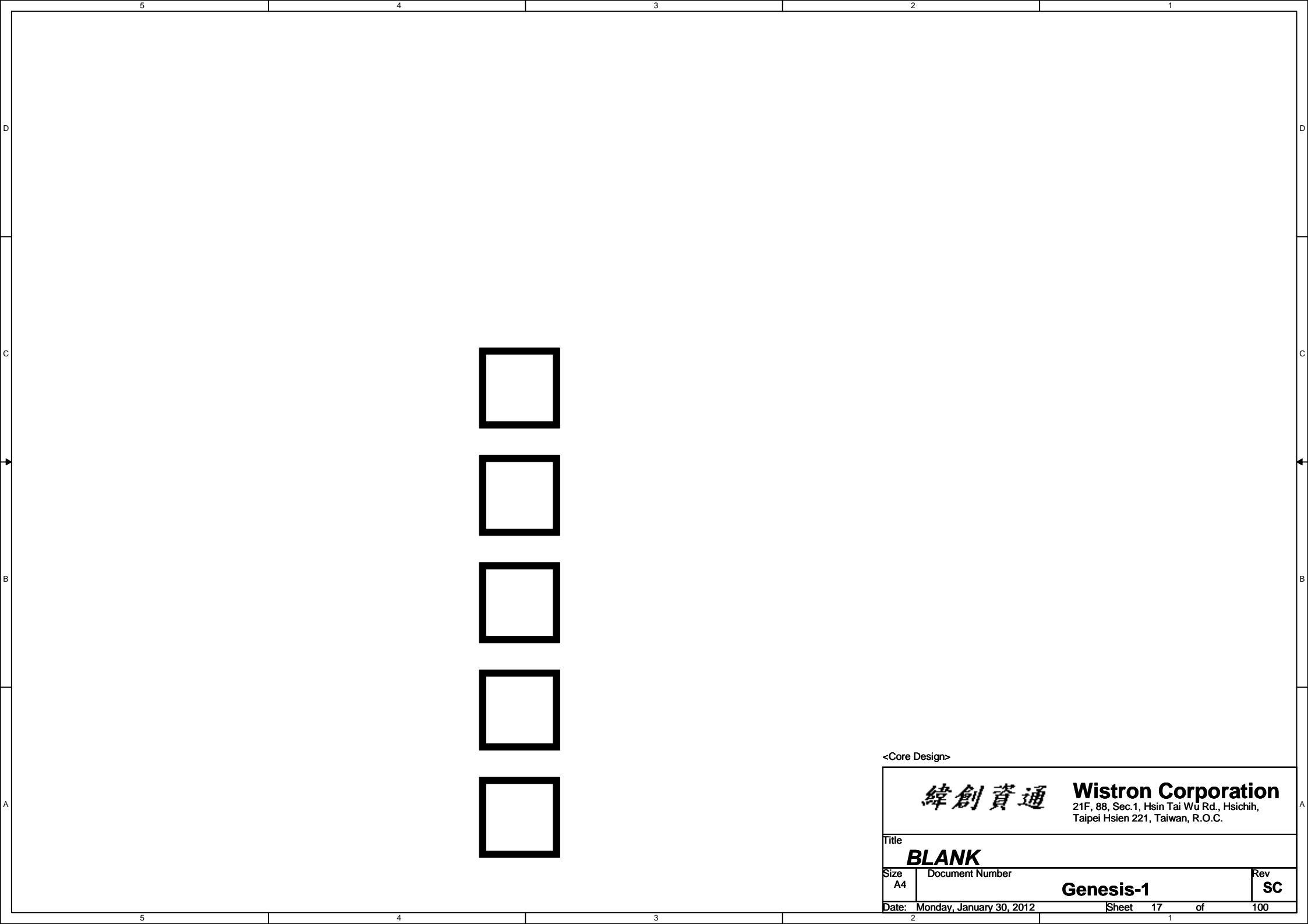
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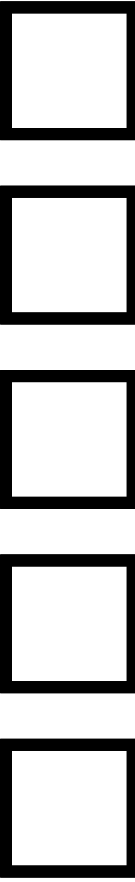
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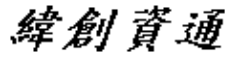
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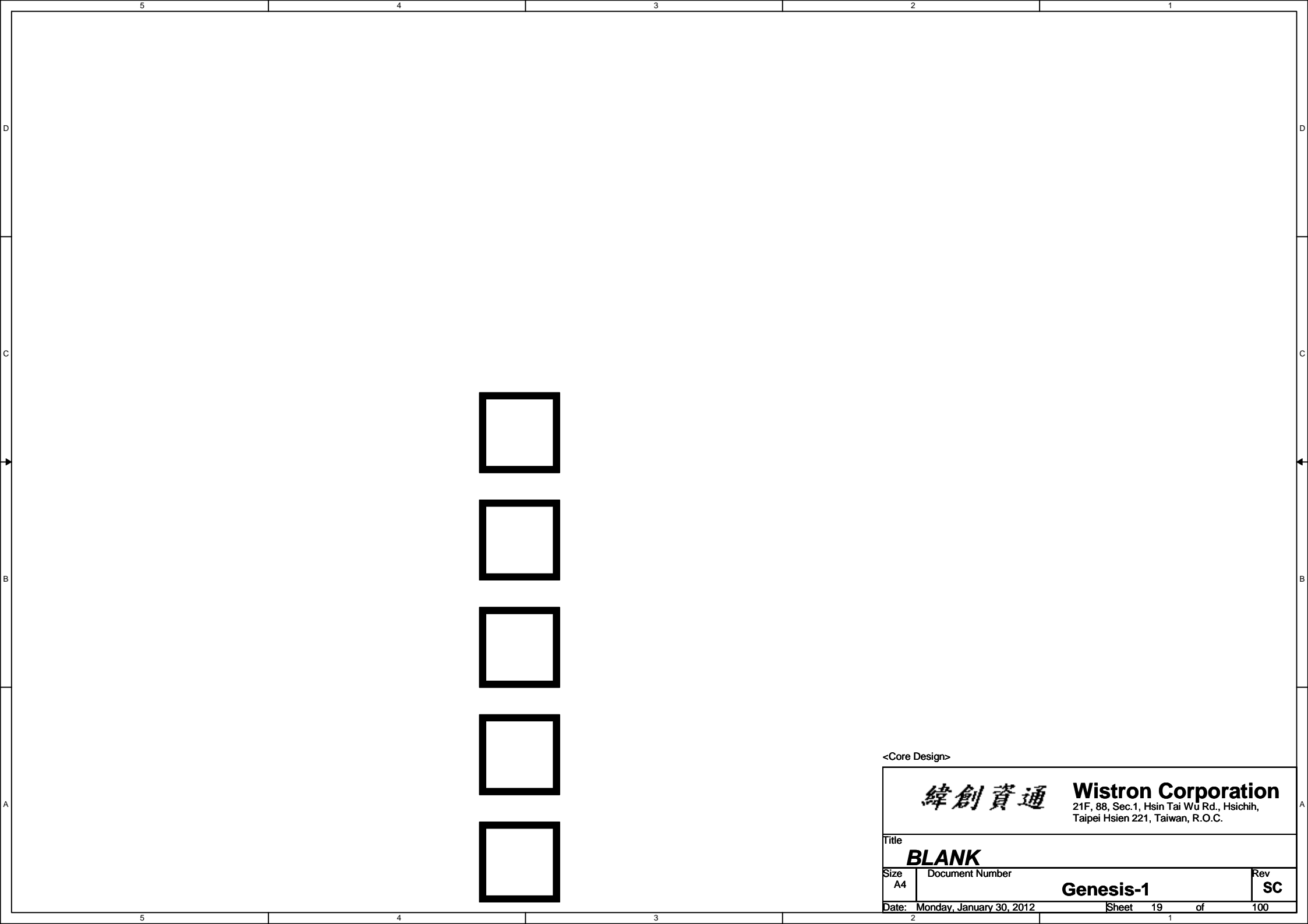
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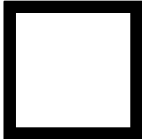
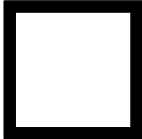
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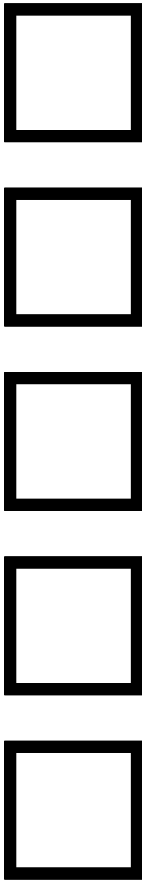
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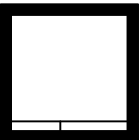
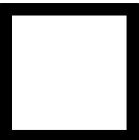
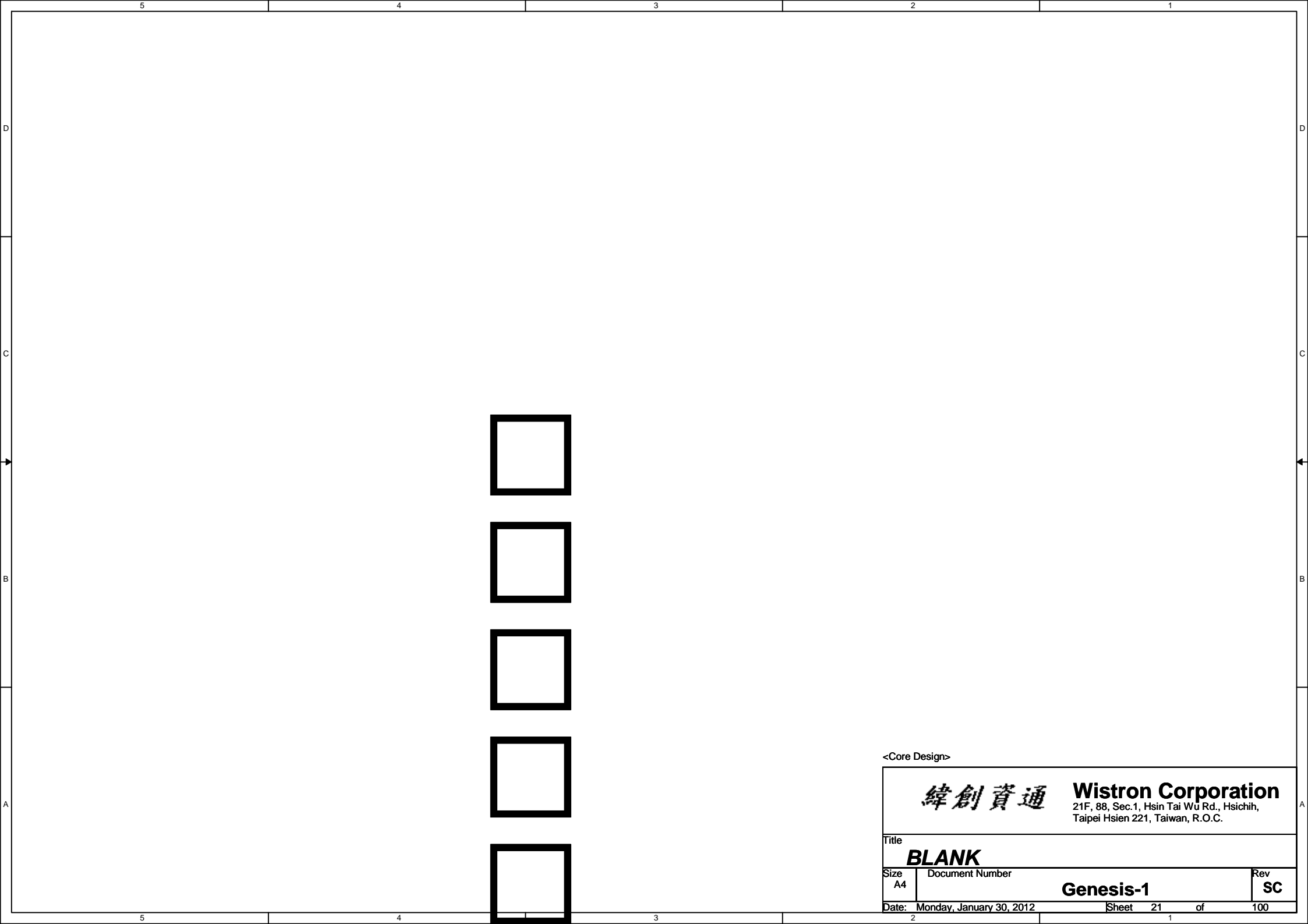
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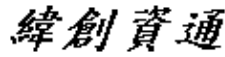
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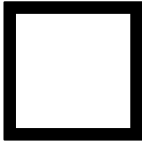
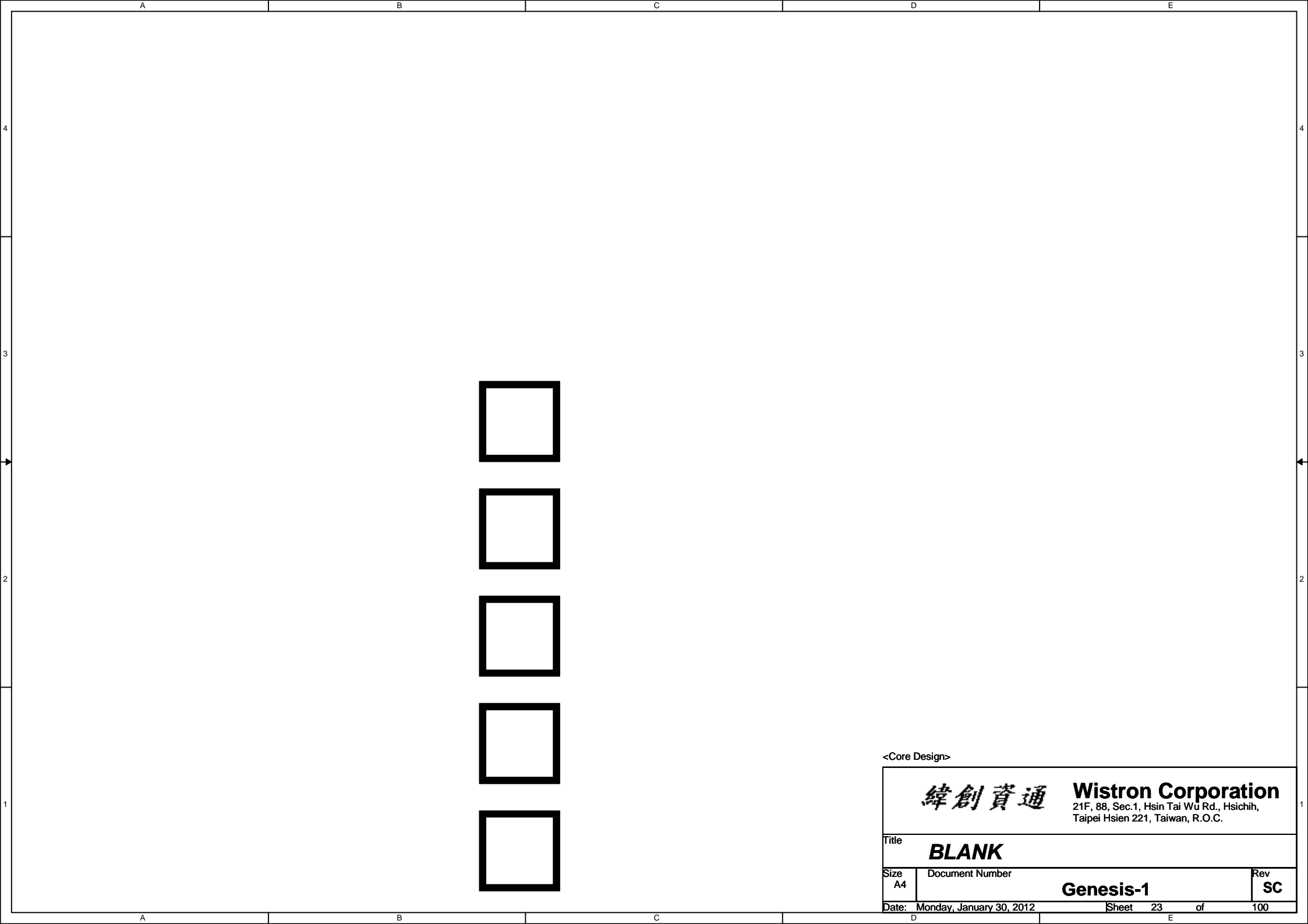
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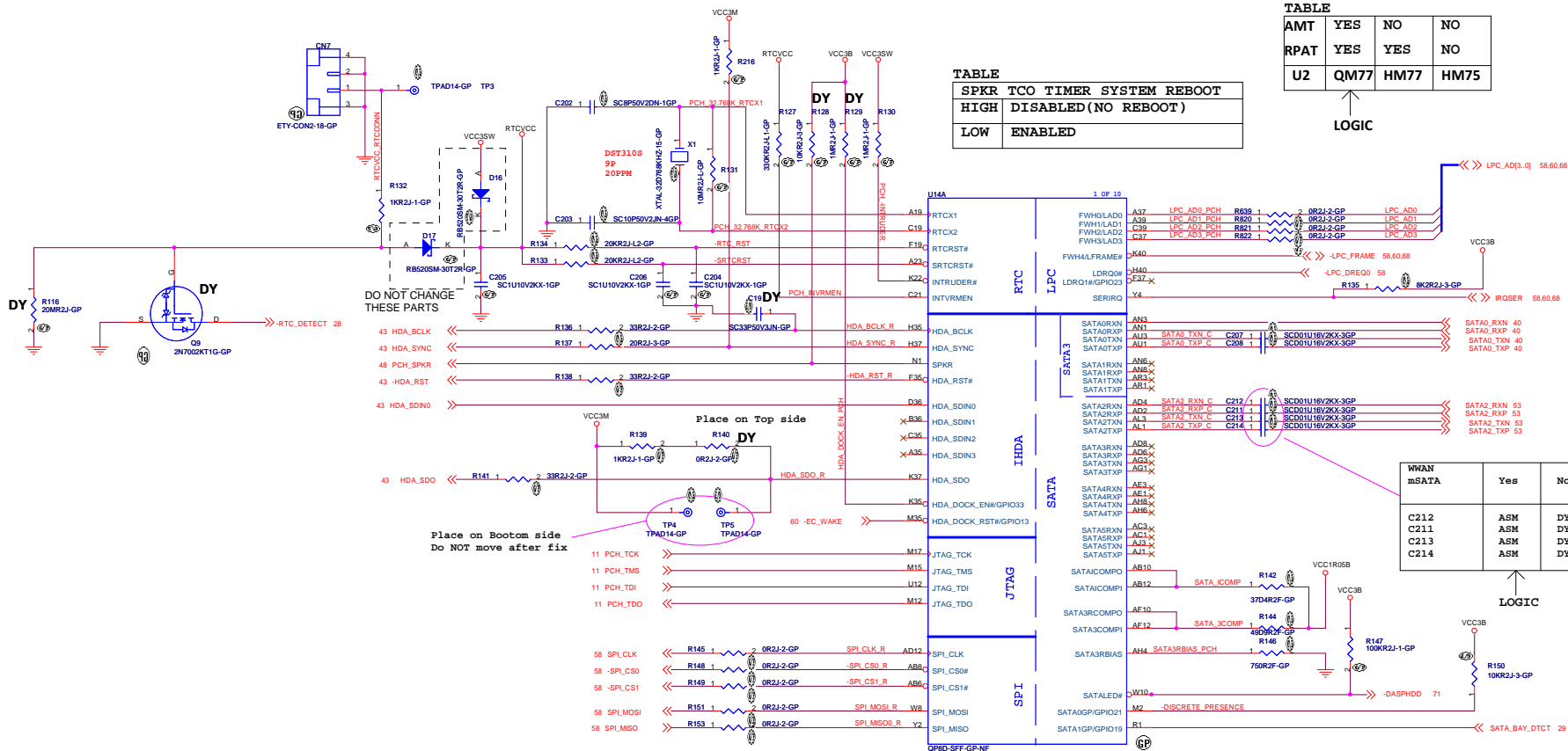
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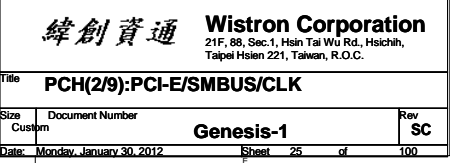
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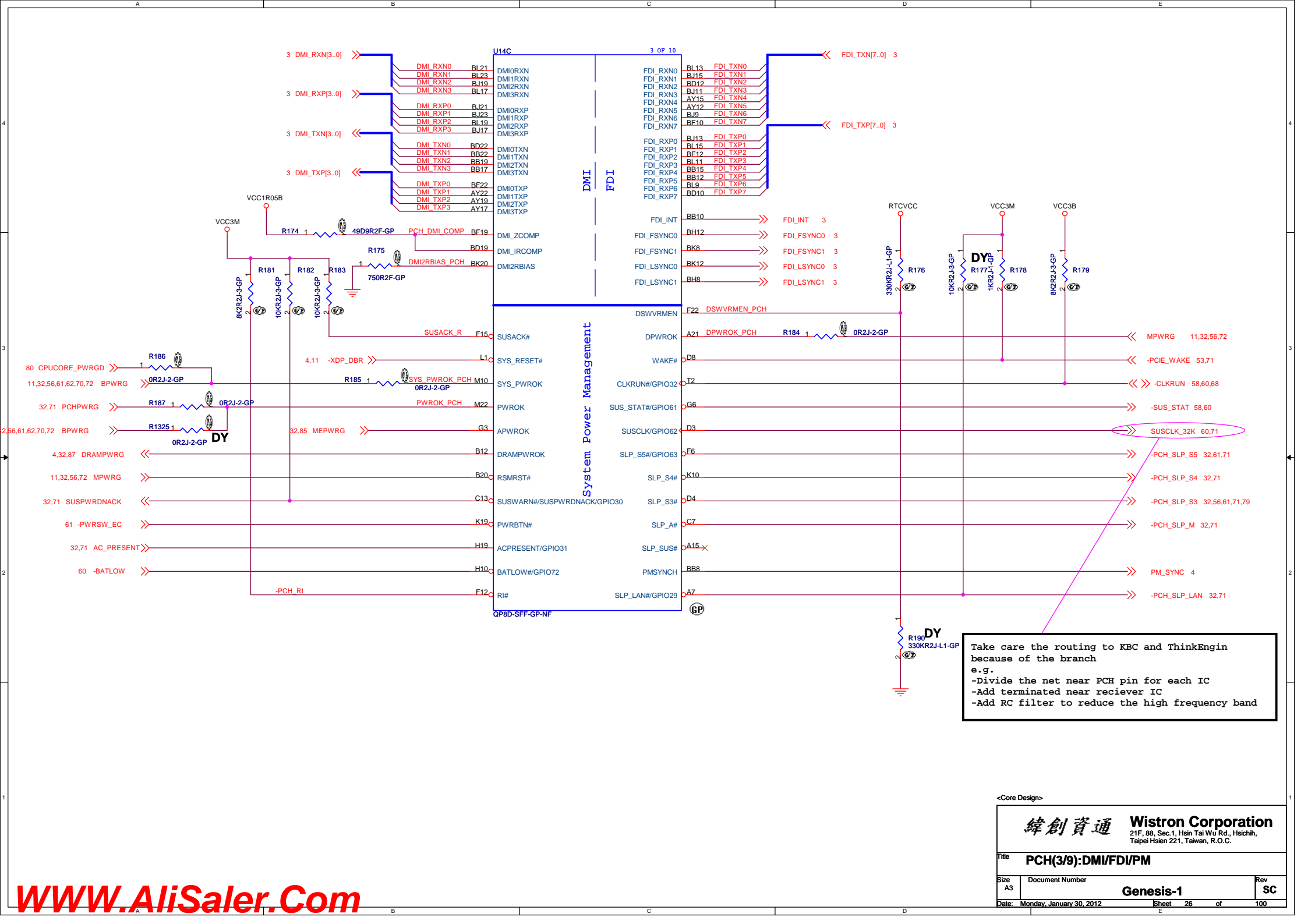
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File PCH(1/9):HDA/JTAG/SPI/SATA

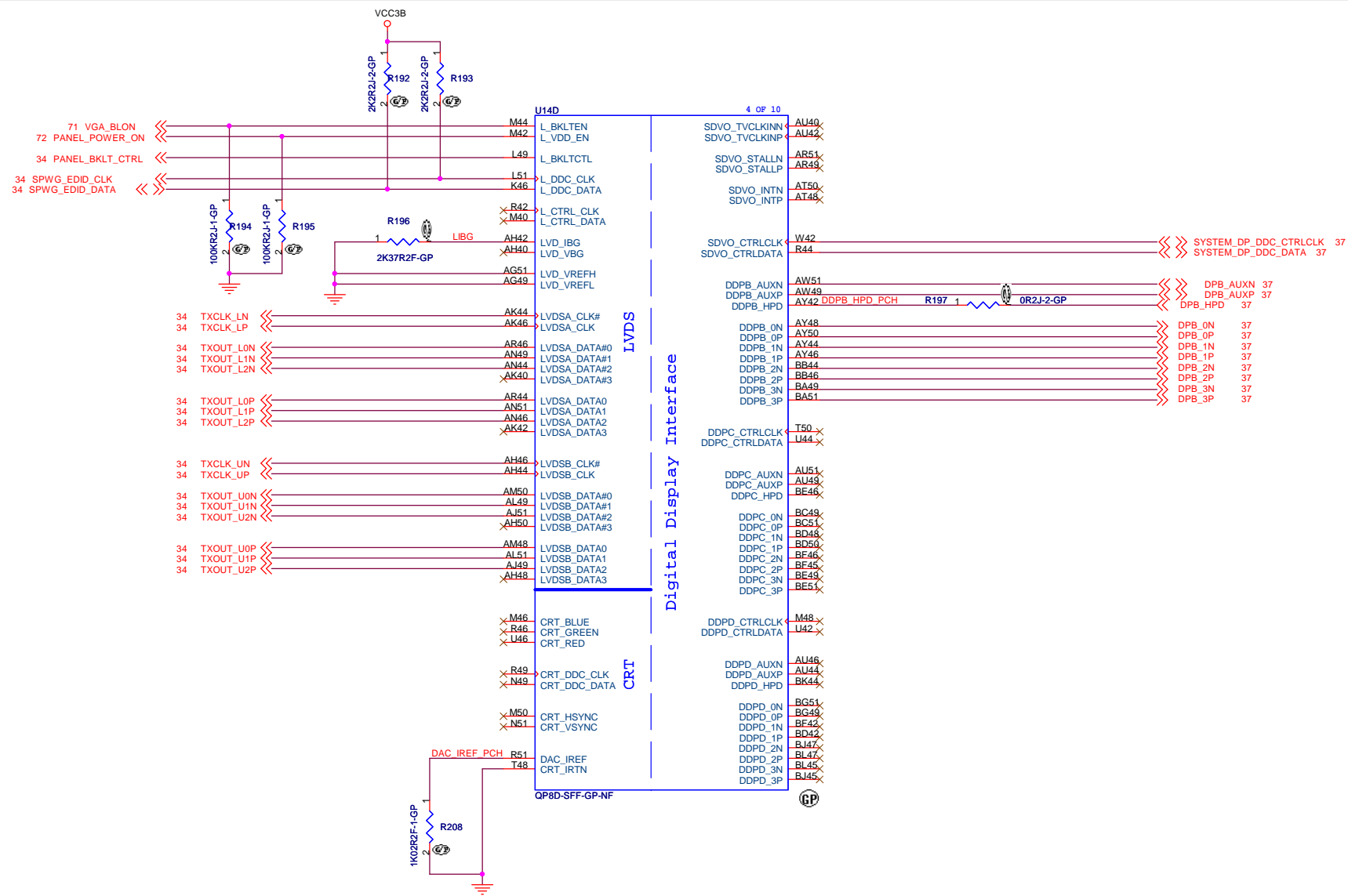
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Take care the routing to KBC and ThinkEngin because of the branch
e.g.
-Divide the net near PCH pin for each IC
-Add terminated near reciever IC
-Add RC filter to reduce the high frequency band

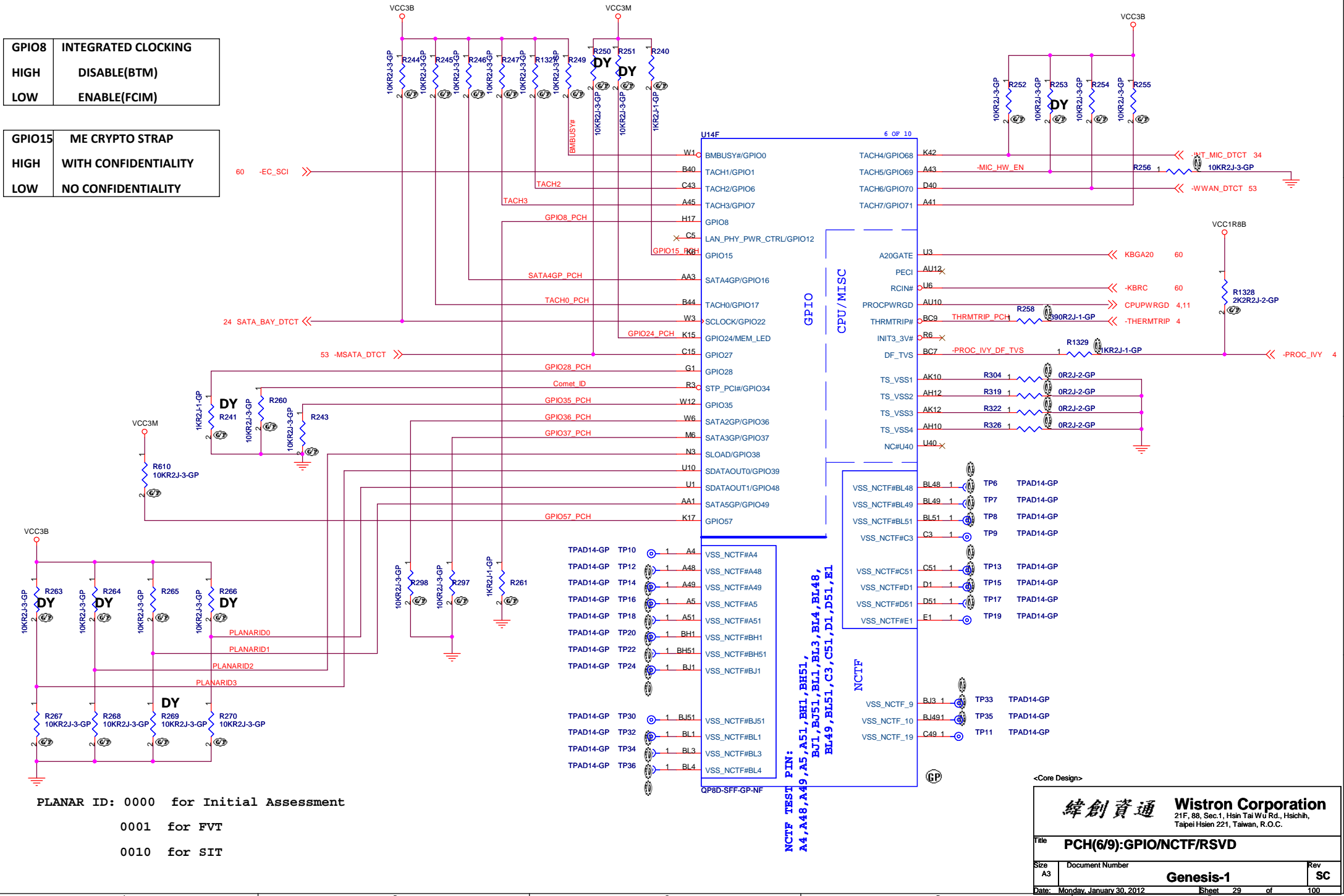


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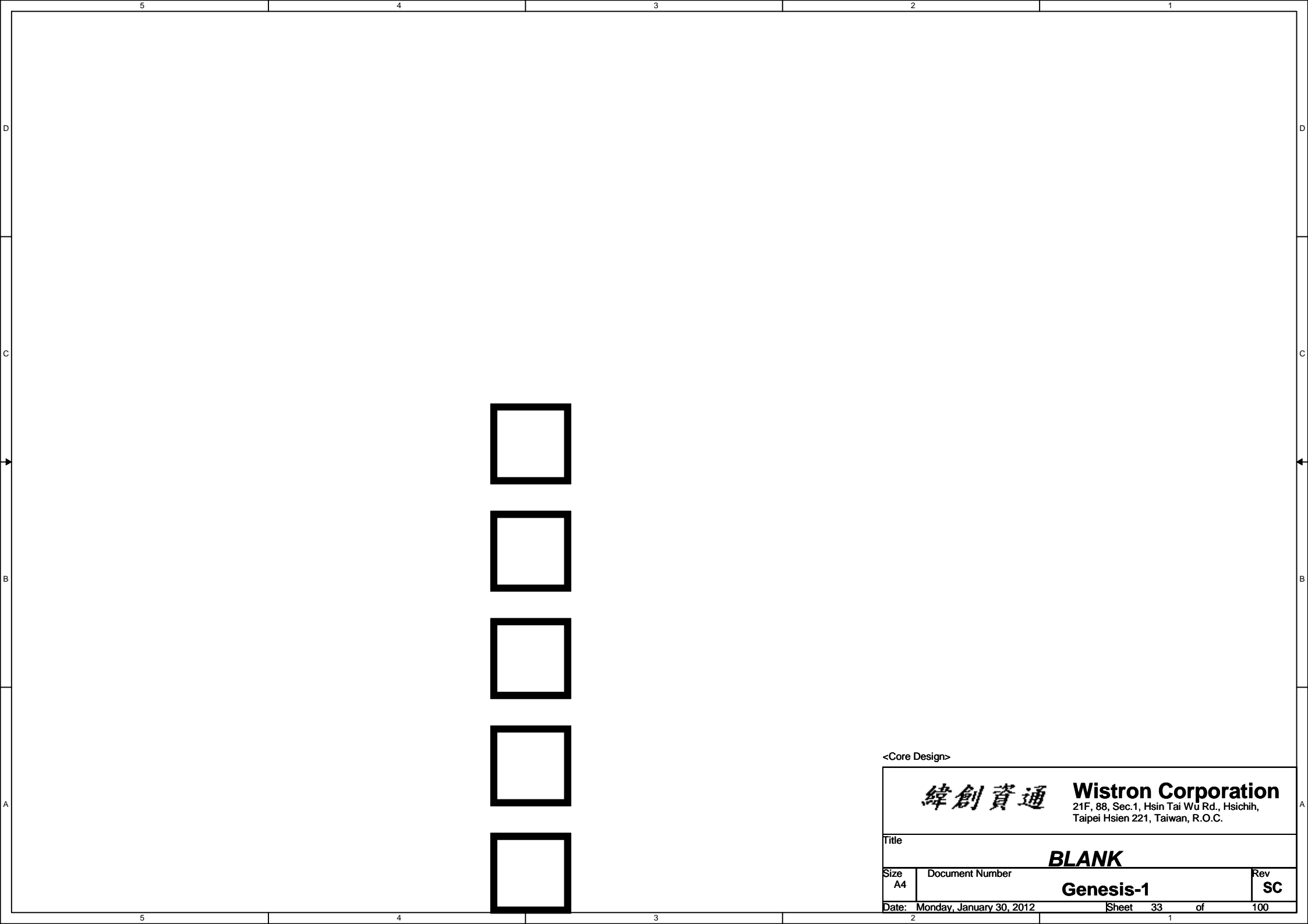
GPIO8	INTEGRATED CLOCKING
HIGH	DISABLE(BTM)
LOW	ENABLE(FCIM)

GPIO15	ME CRYPTO STRAP
HIGH	WITH CONFIDENTIALITY
LOW	NO CONFIDENTIALITY



PLANAR ID: 0000 for Initial Assessment
 0001 for FVT
 0010 for SIT





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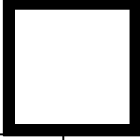
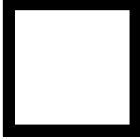
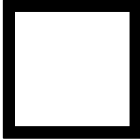
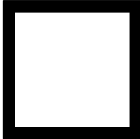
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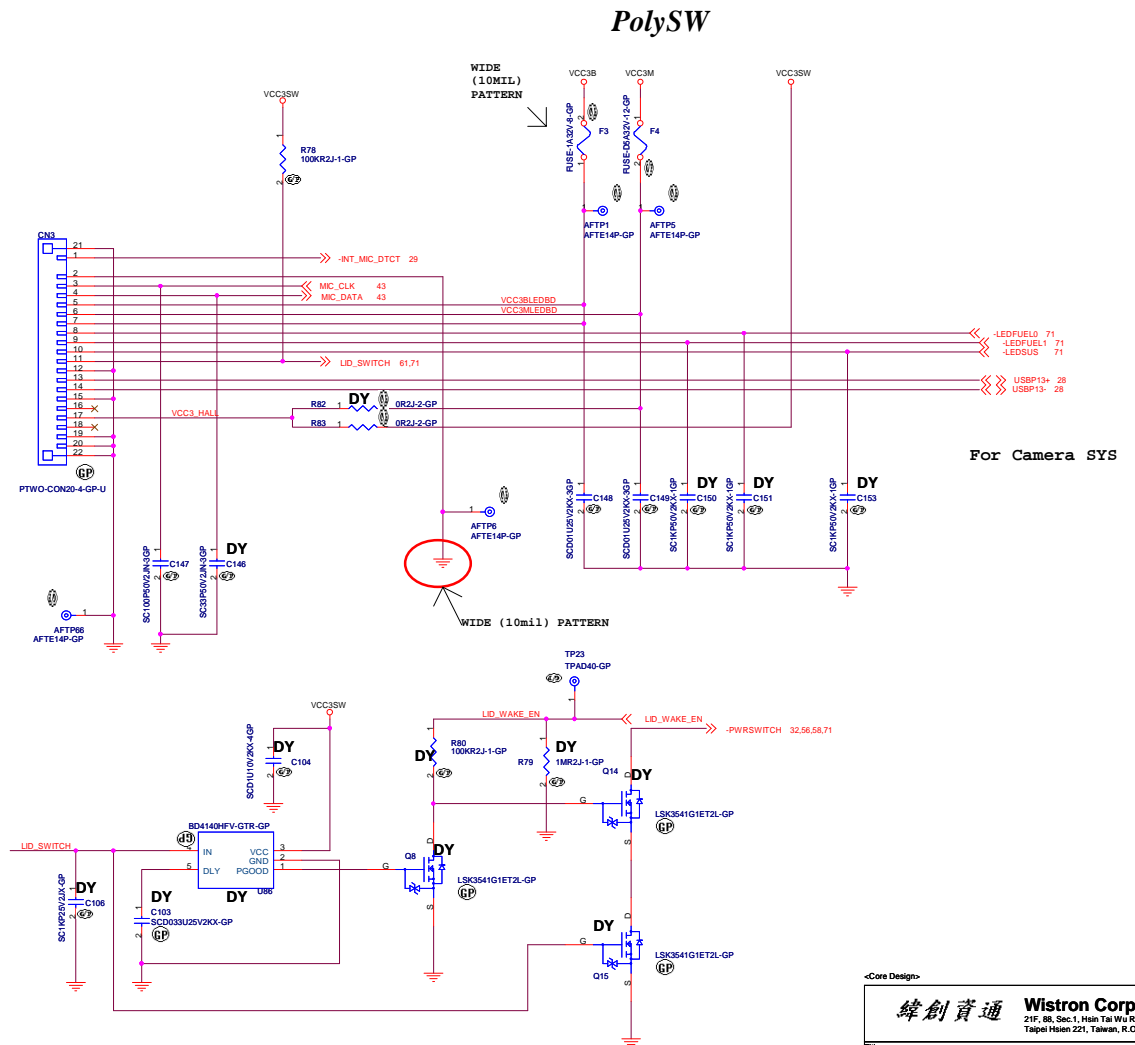
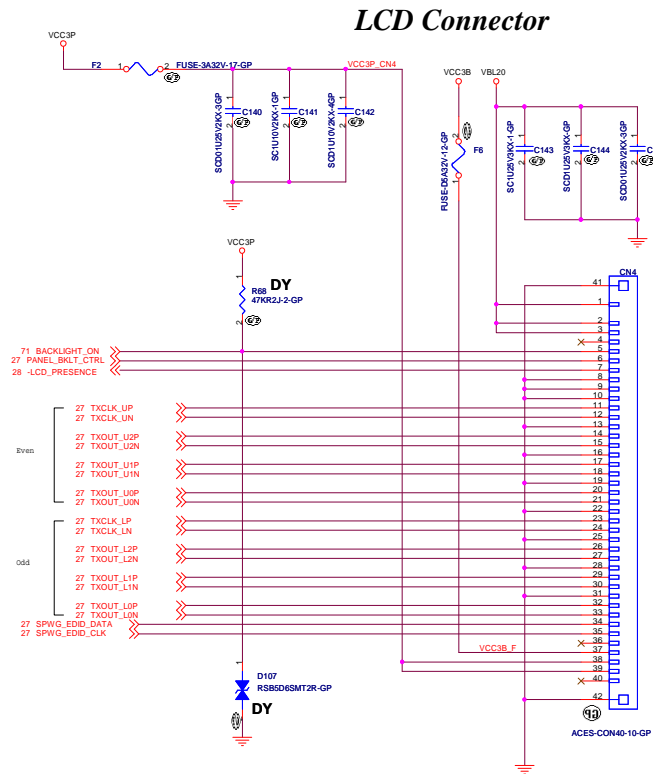
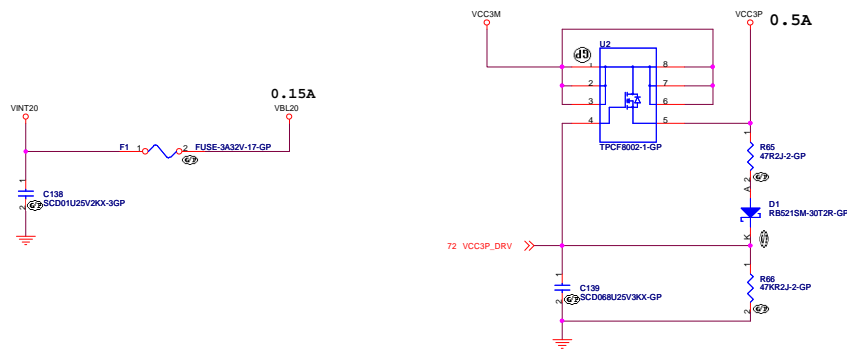
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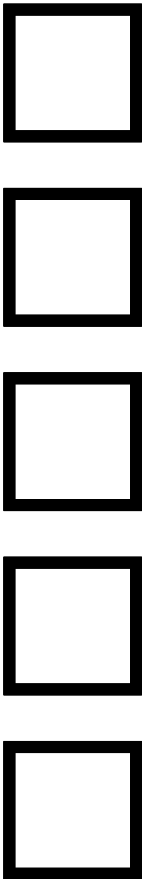
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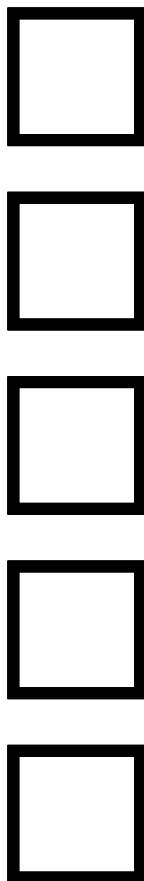
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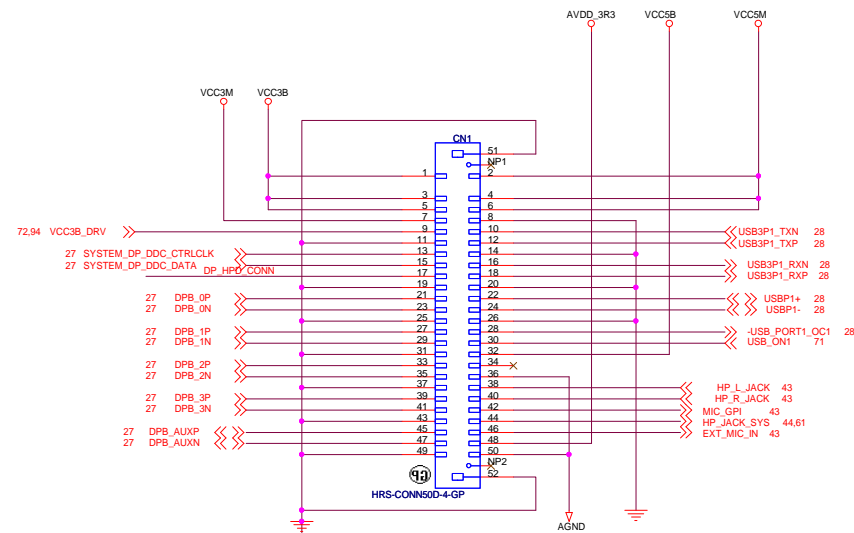
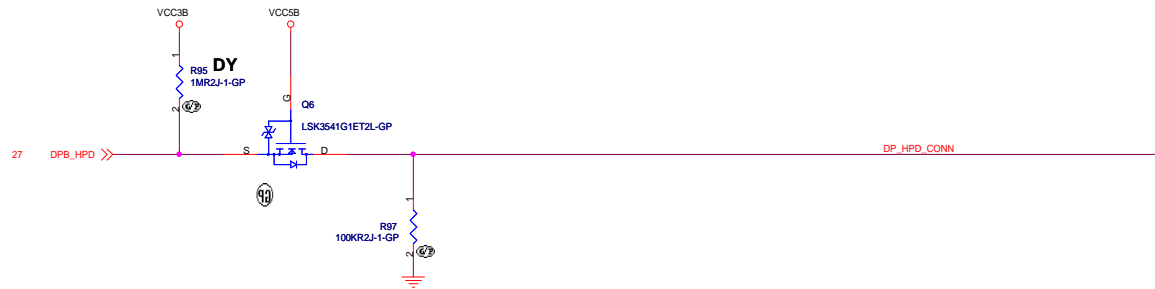
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Size	Document Number	Rev
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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
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Size A4	Document Number Genesis-1		Rev SC
Date: Monday, January 30, 2012		Sheet 36 of	100

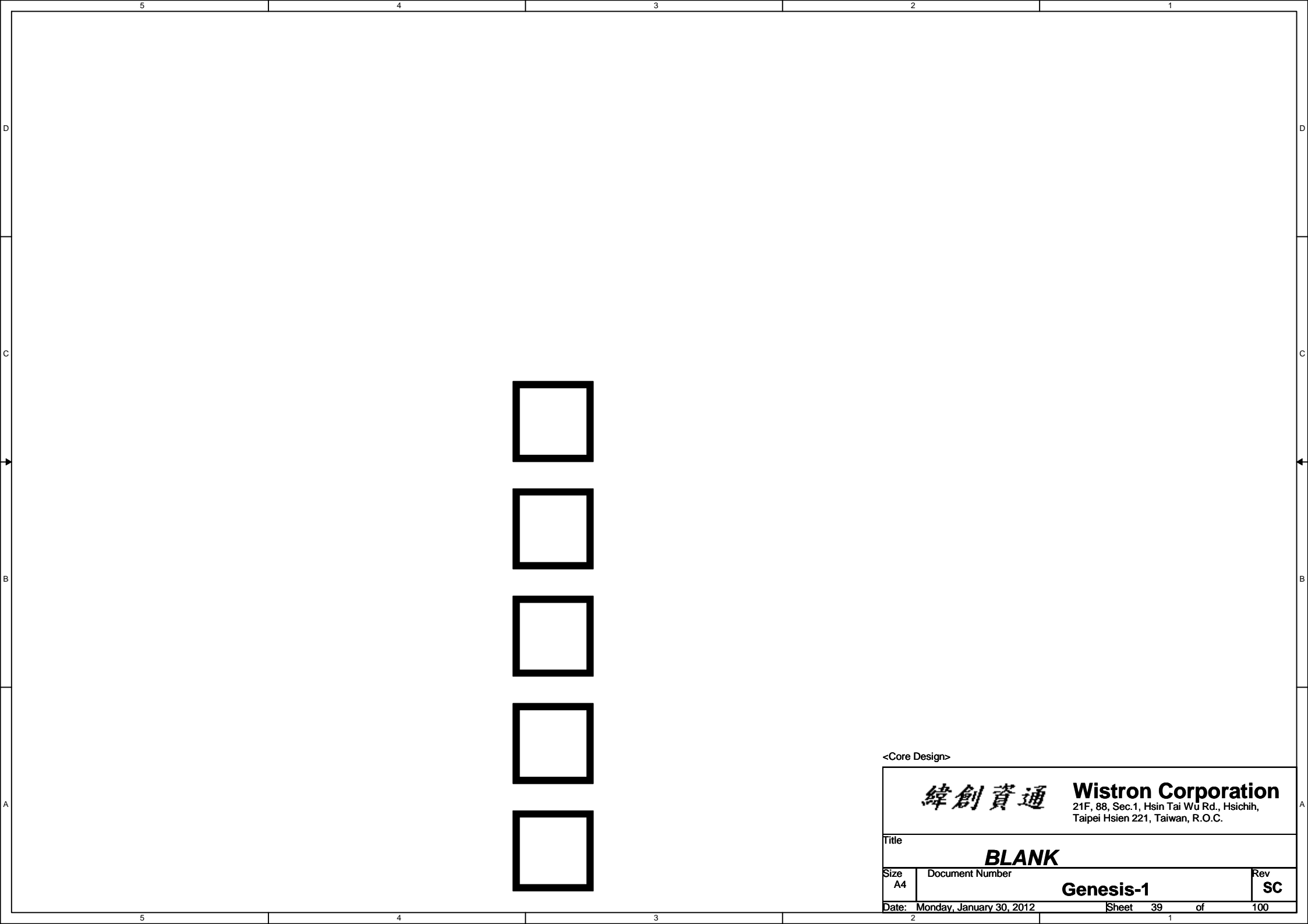


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Title Display Port Connector	
Size Custom	Document Number Genesis-1
Date: Monday, January 30, 2012	Rev SC
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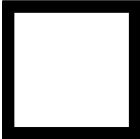
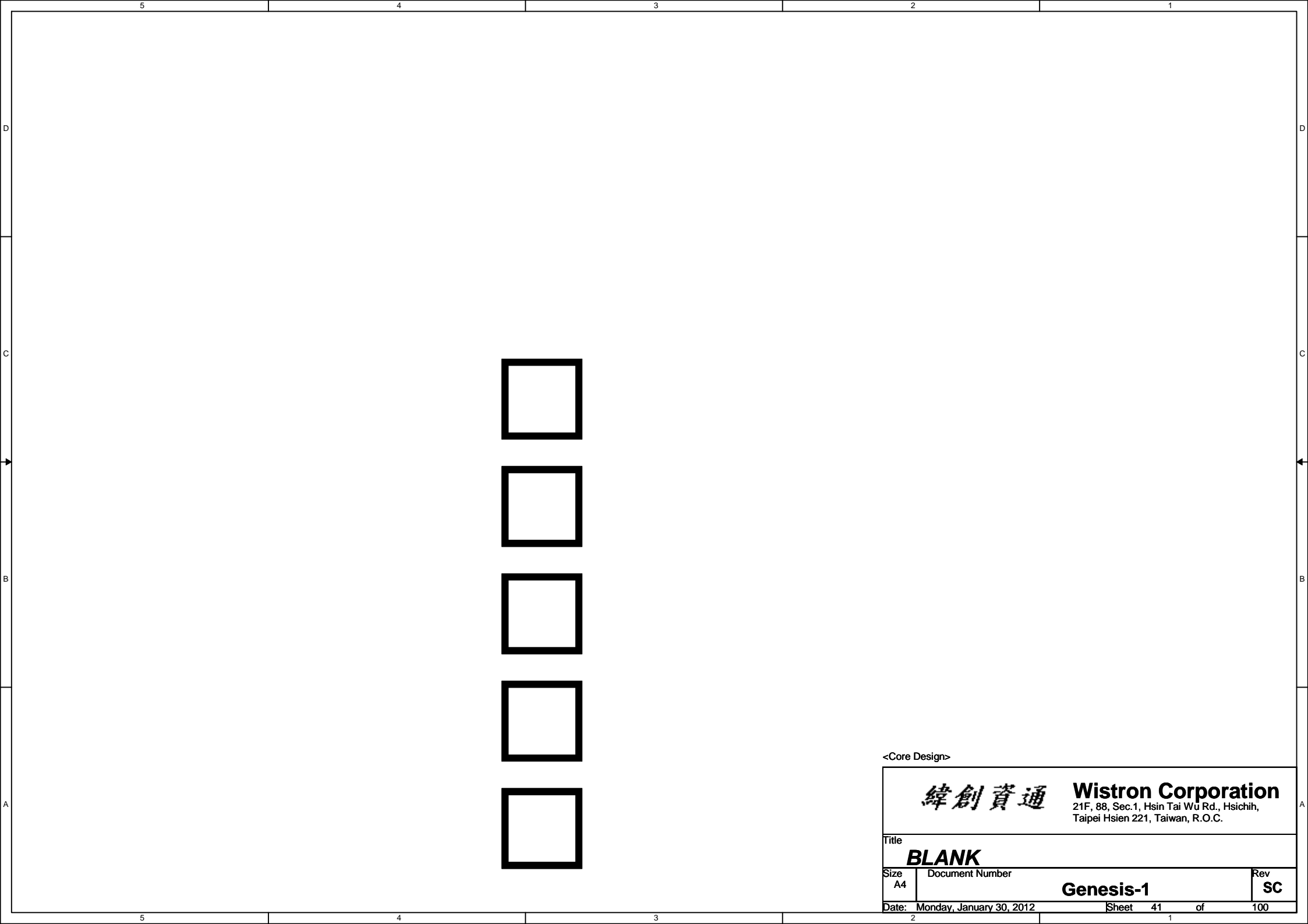
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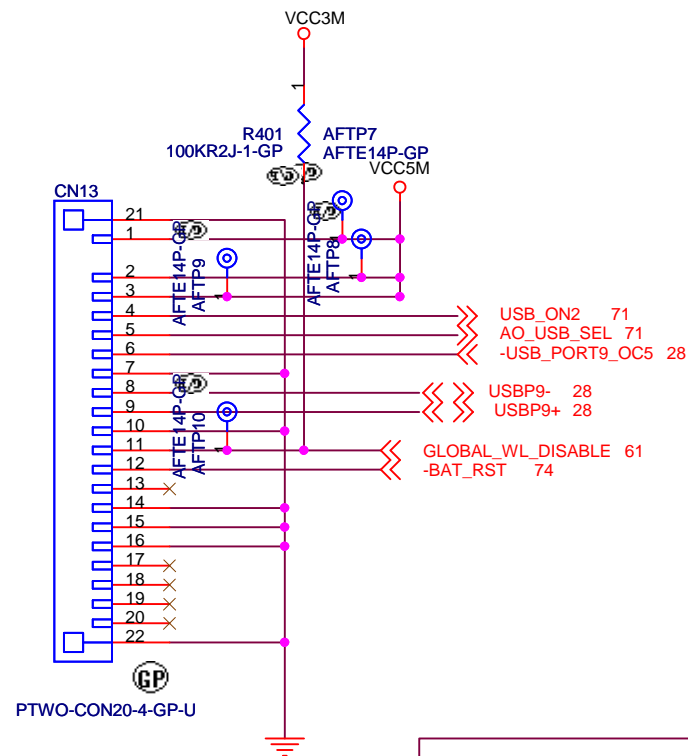
Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

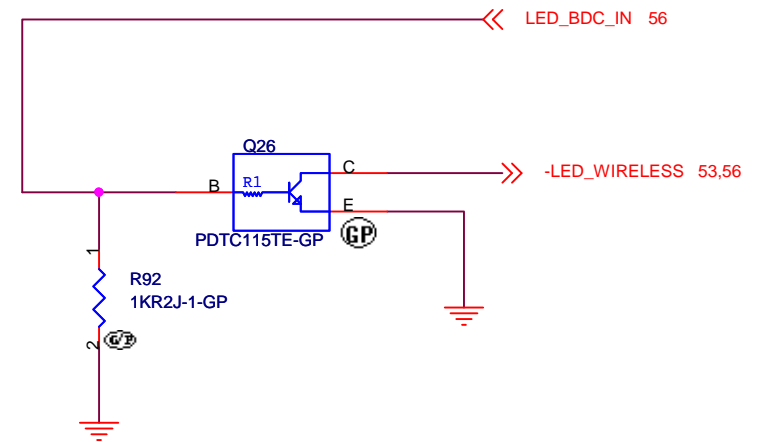
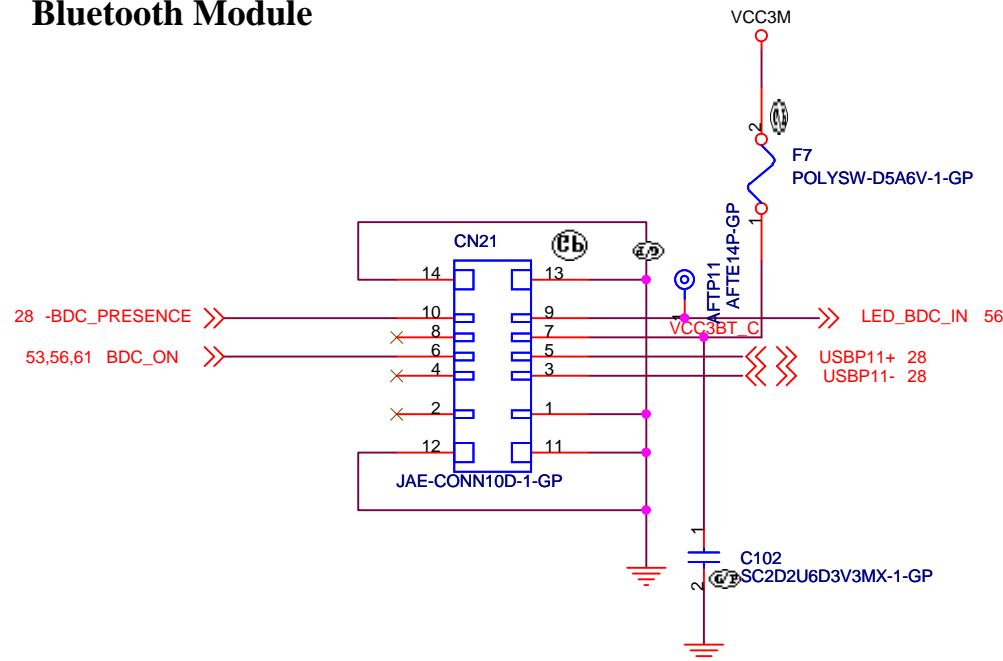
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Size A4	Document Number	Rev SC
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Genesis-1



Bluetooth Module



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Taipei Hsien 221, Taiwan, R.O.C.

Title

USB Connector & BT

Size
A4

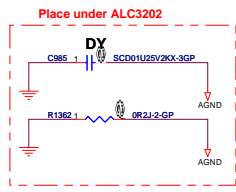
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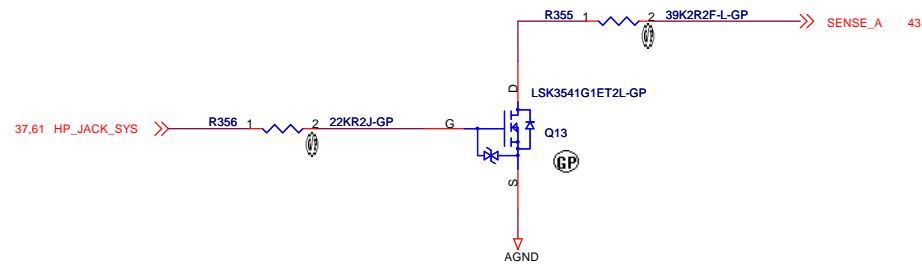
Genesis-1

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SC

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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title			AUDIO JACK SENSE		
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Size

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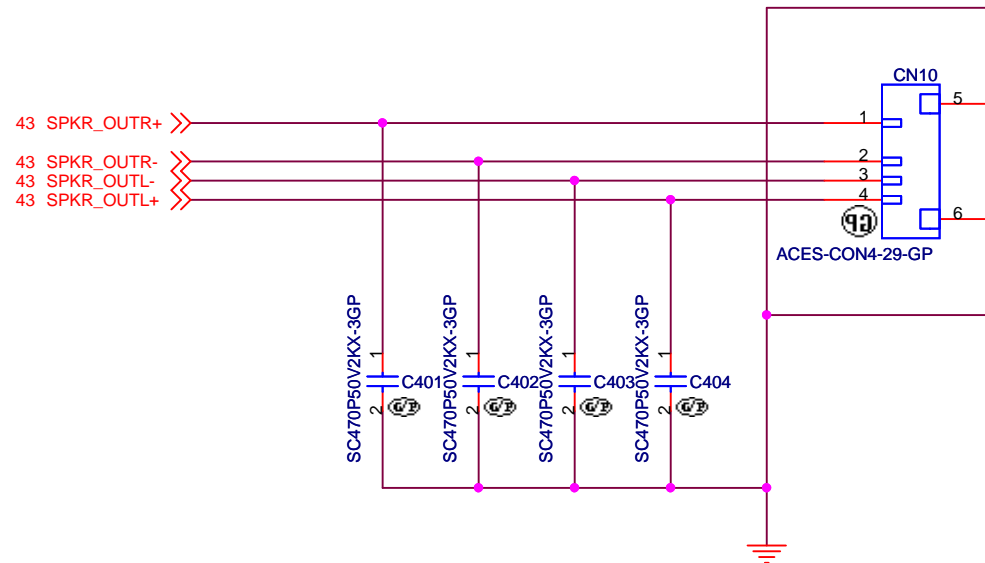
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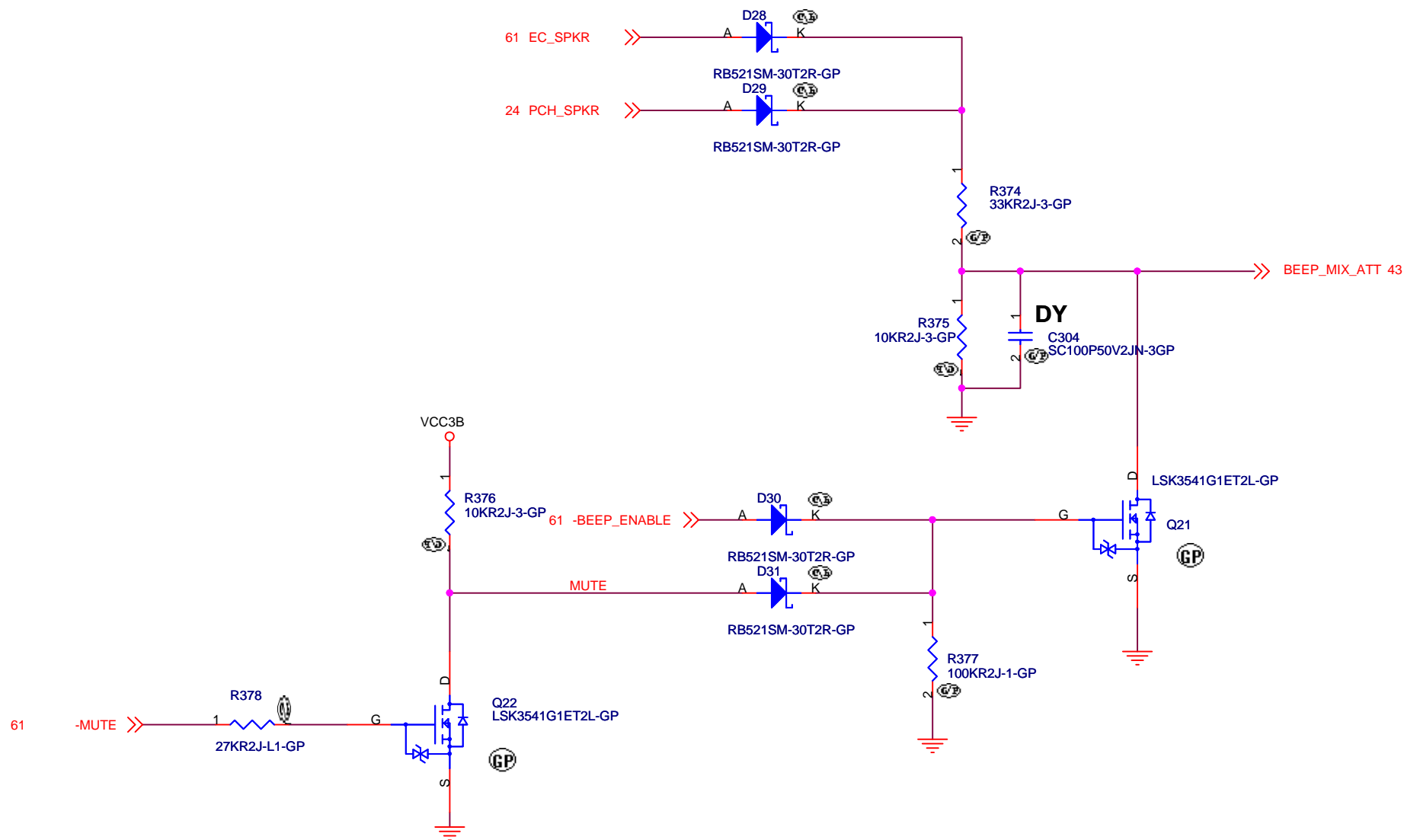
Date: Monday, January 30, 2012

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AUDIO SPEAKER			
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Title

Audio BEEP

Size
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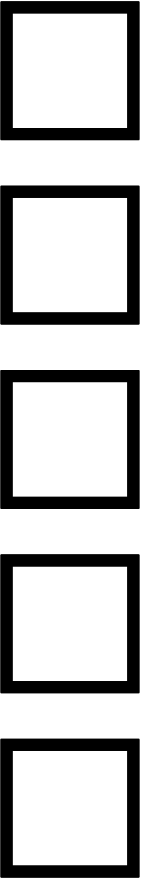
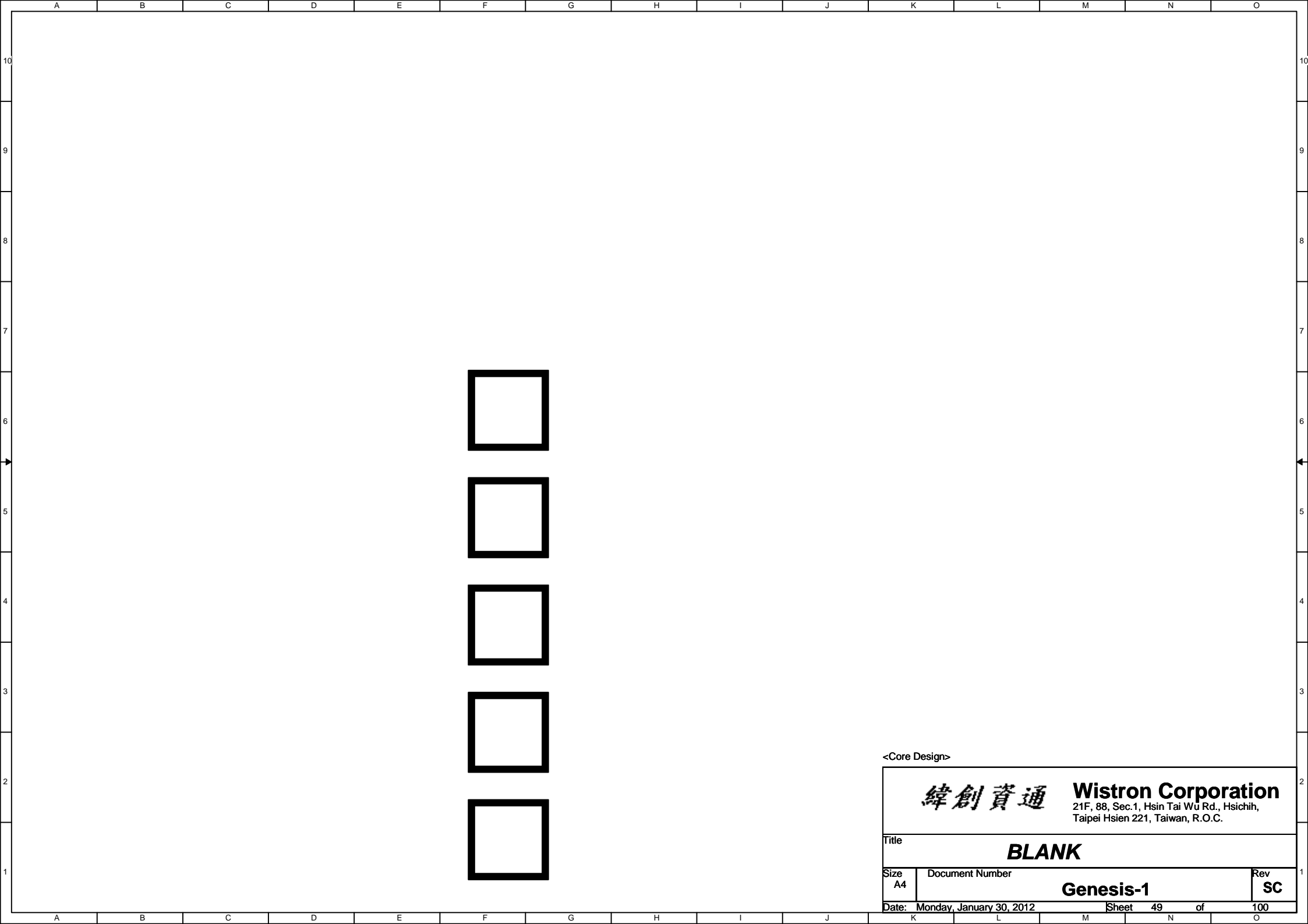
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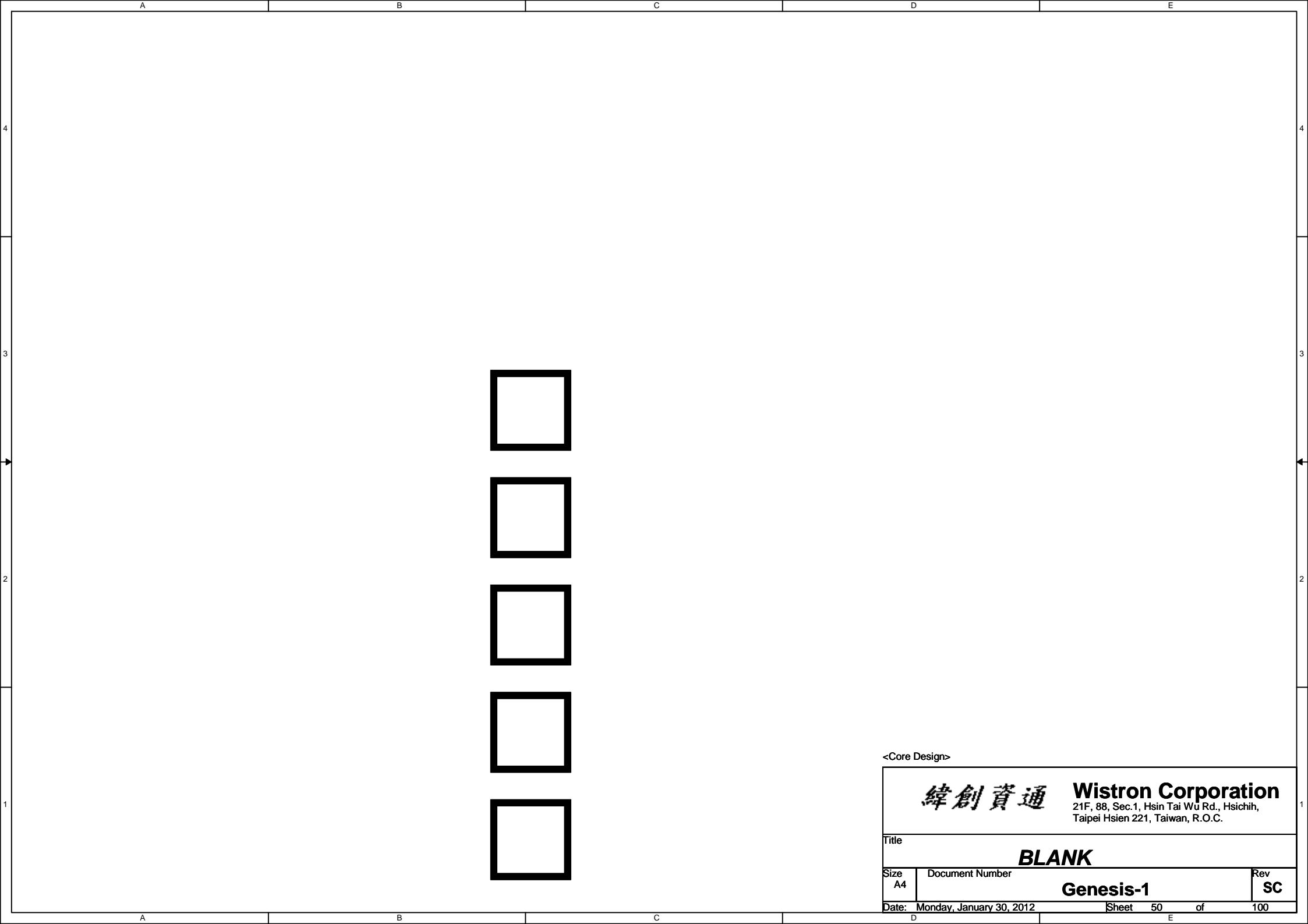
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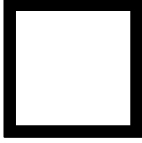
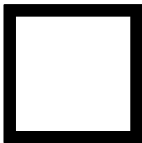
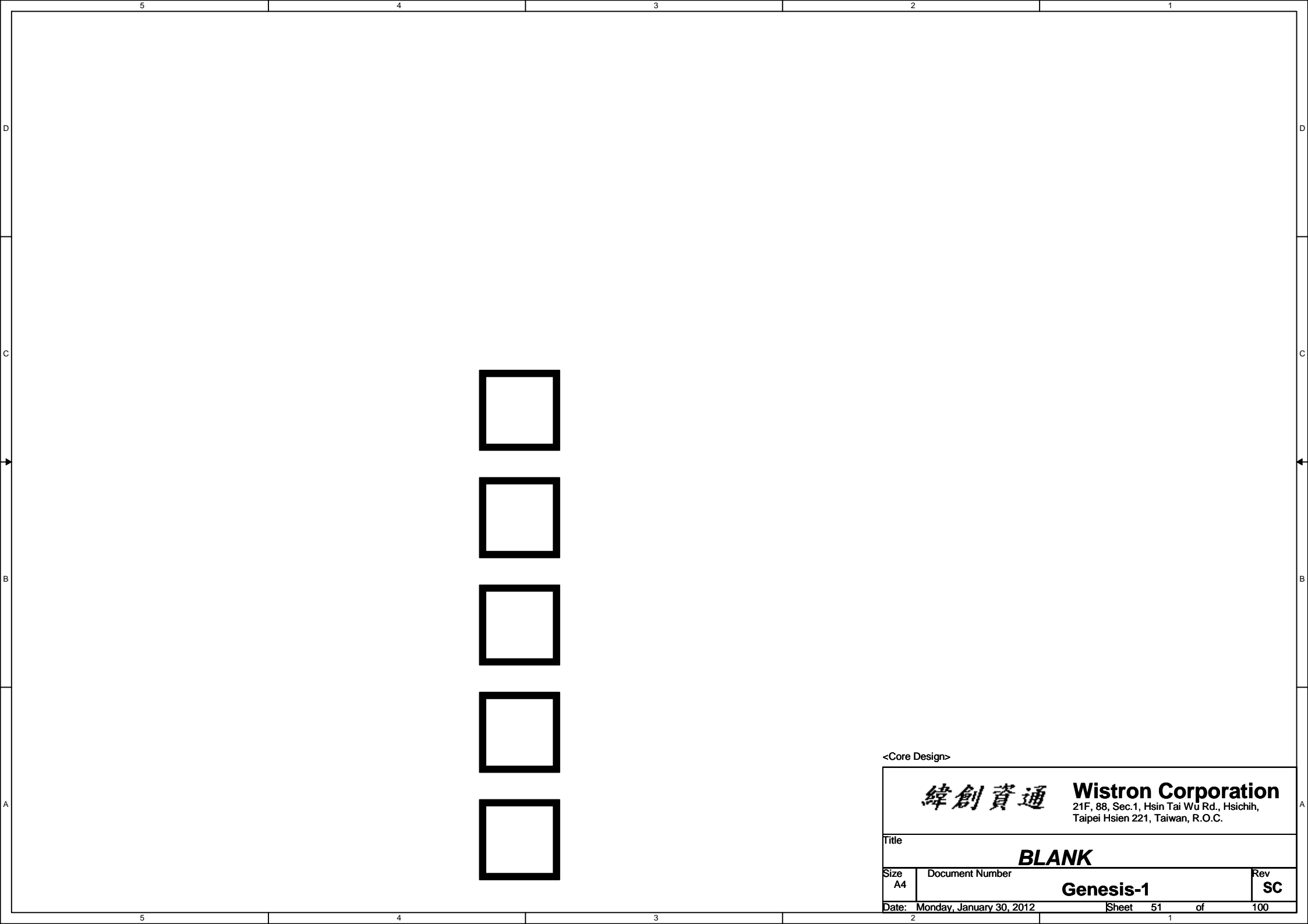
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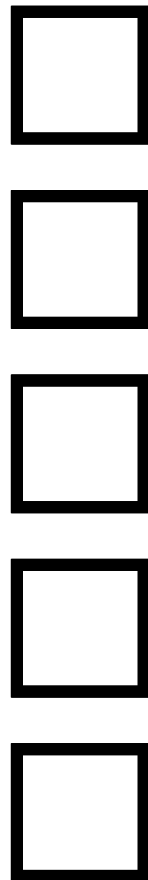
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Taipei Hsien 221, Taiwan, R.O.C.

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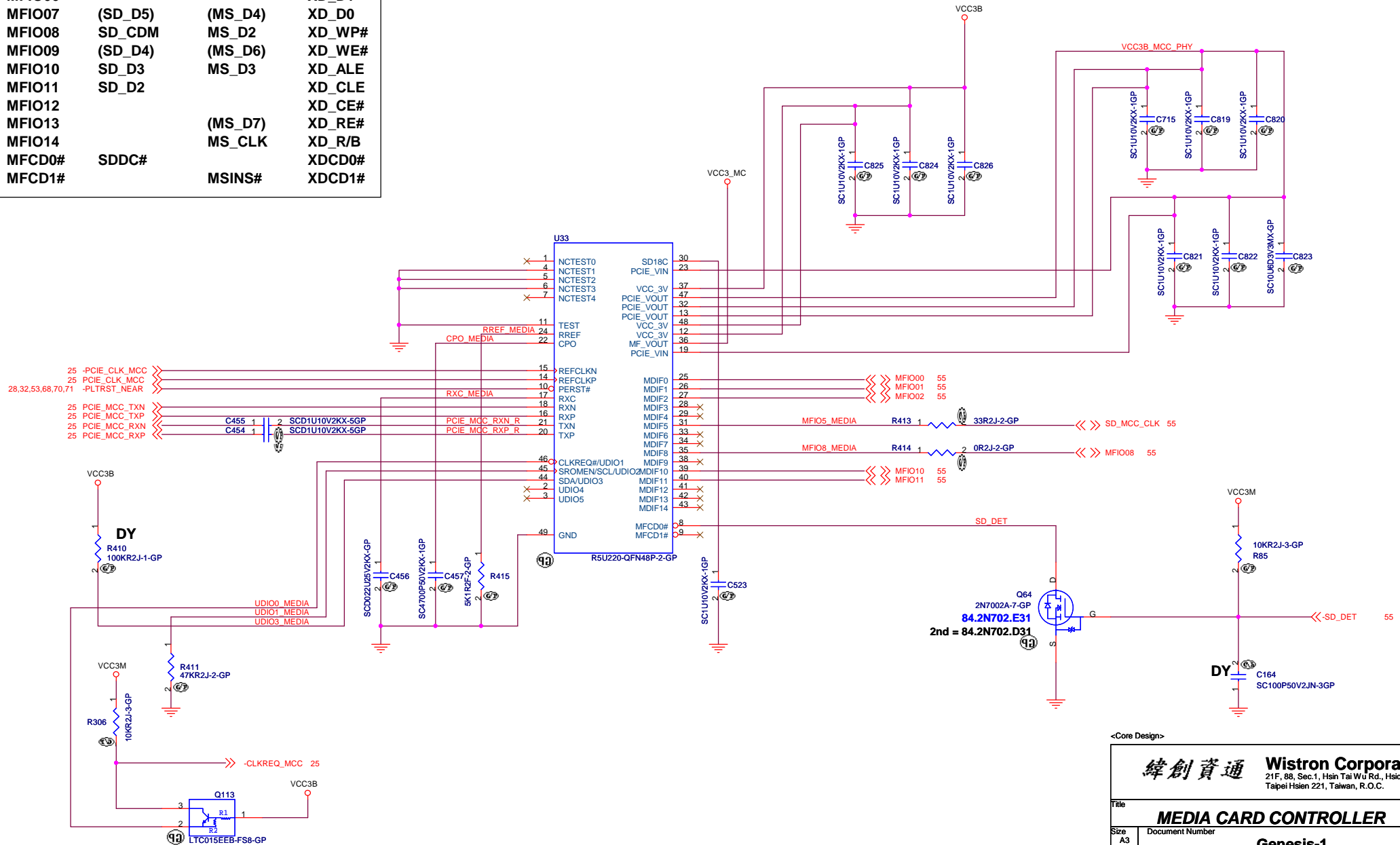
Date: Monday, January 30, 2012 Sheet 51 of 100

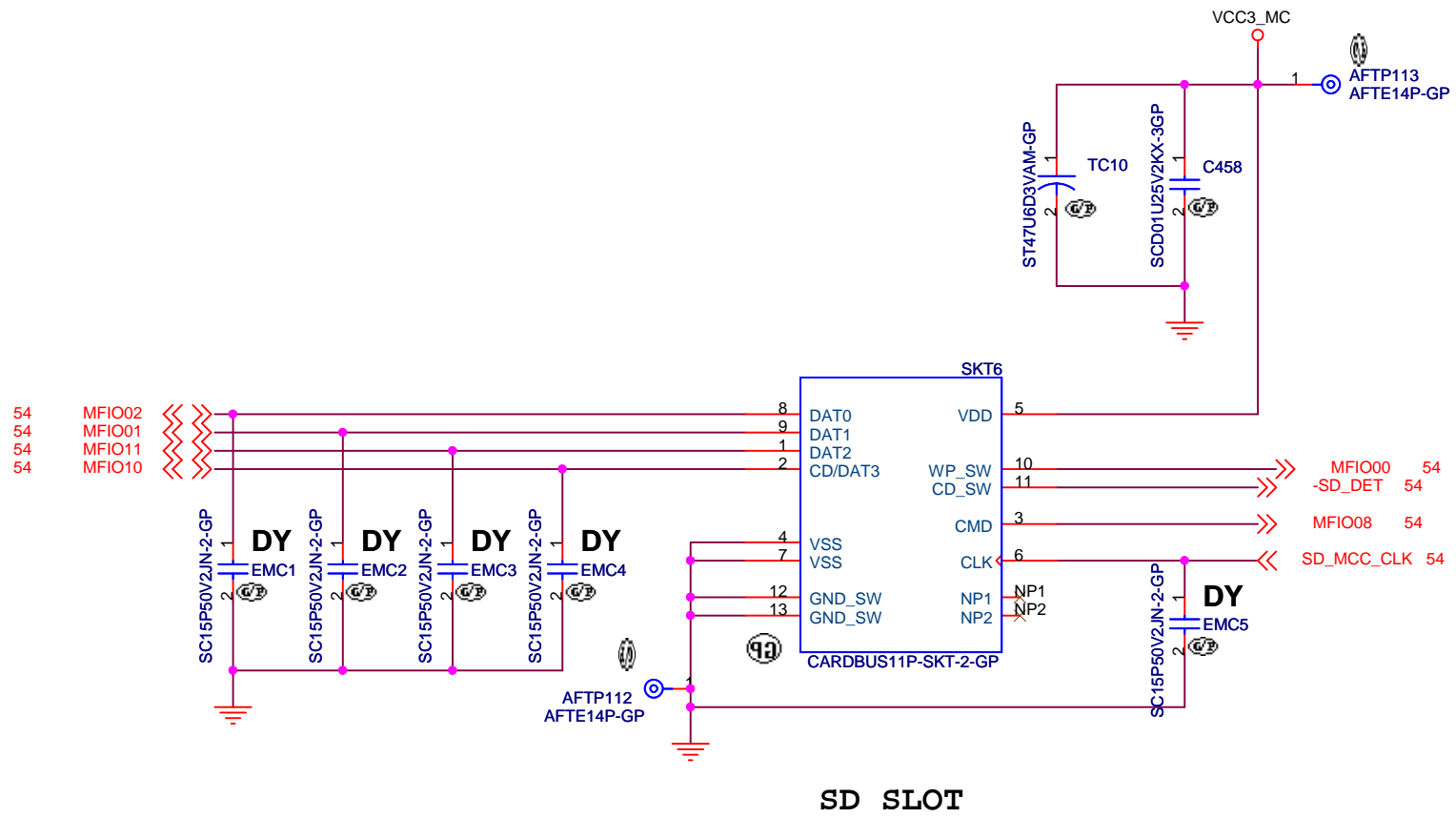


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MEDIA I/F	SD/MMC	MEMORYSTICK	XD
MFIO00	SDWP#	MSBS	XD_D7
MFIO01	SD_D1		XD_D6
MFIO02	SD_D0	MS_D1	XD_D5
MFIO03	(SD_D7)		XD_D4
MFIO04	(SD_D6)	(MS_D5)	XD_D3
MFIO05	SD_CLK	MSD0	XD_D2
MFIO06			XD_D1
MFIO07	(SD_D5)	(MS_D4)	XD_D0
MFIO08	SD_CDM	MS_D2	XD_WP#
MFIO09	(SD_D4)	(MS_D6)	XD_WE#
MFIO10	SD_D3	MS_D3	XD_ALE
MFIO11	SD_D2		XD_CLE
MFIO12			XD_CE#
MFIO13		(MS_D7)	XD_RE#
MFIO14		MS_CLK	XD_R/B
MFCD0#	SDDC#		XDCD0#
MFCD1#		MSINS#	XDCD1#





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Title

Media Card Slot

Size
A4

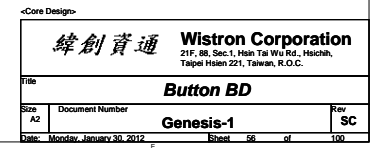
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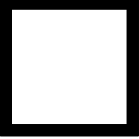
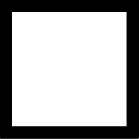
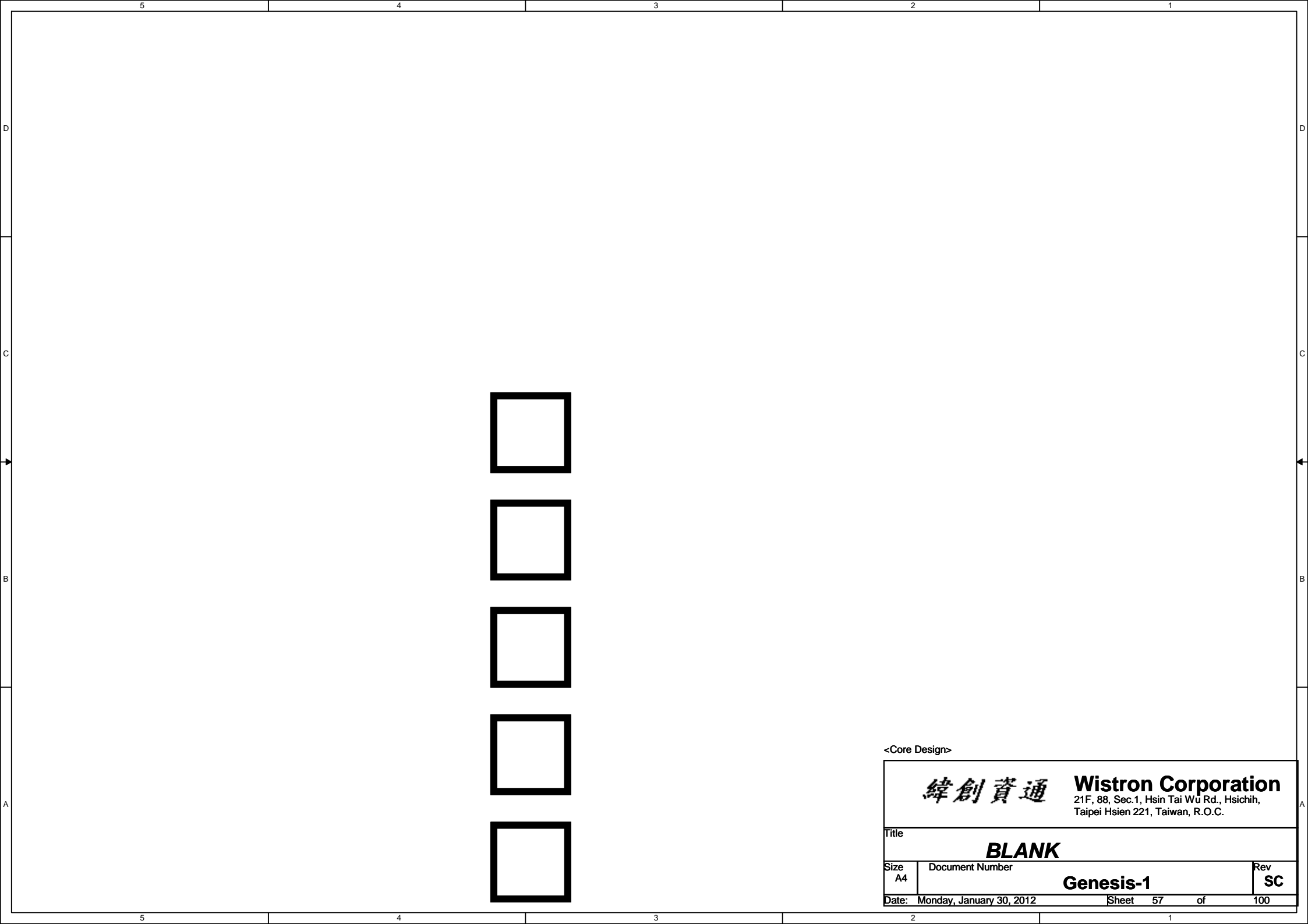
Genesis-1

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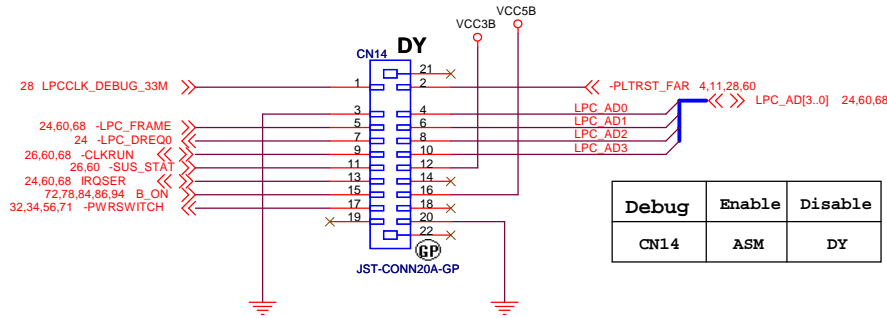




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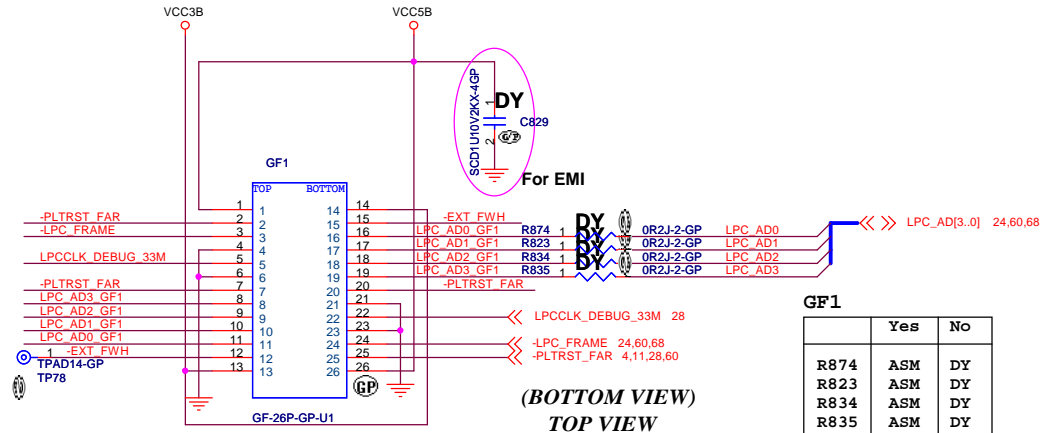
Debug card connector



Put "easy-to -access" place

Debug	Enable	Disable
CN14	ASM	DY

Golden Finger for Debug Board



(BOTTOM VIEW)
TOP VIEW

(26) (25)....(15) (14)
13 12 2 1

GF1	Yes	No
R874	ASM	DY
R823	ASM	DY
R834	ASM	DY
R835	ASM	DY
R235	ASM	DY

Logic

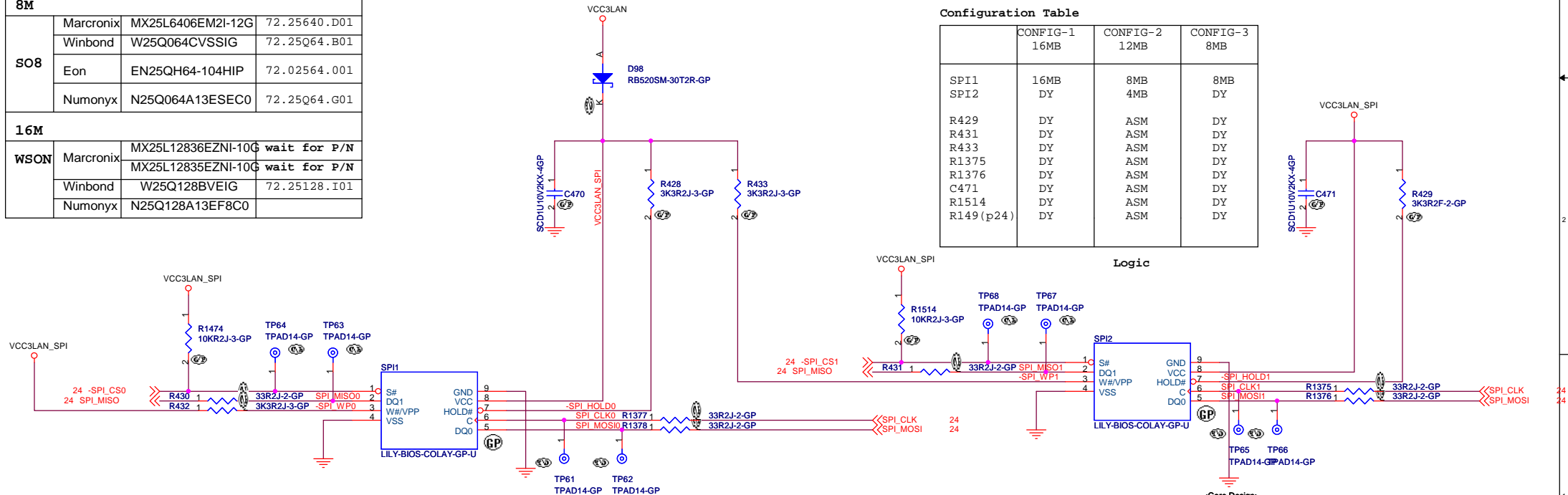
4M

SO8	Marconix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Eon	EN25QH32-104HIP	72.02532.B01
	Numonyx	N25Q032A13ESEC0	72.25Q32.C01
8M			
SO8	Marconix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Eon	EN25QH64-104HIP	72.02564.001
	Numonyx	N25Q064A13ESEC0	72.25Q64.G01
16M			
WSO8	Marconix	MX25L12836EZNI-10G	wait for P/N
	Winbond	MX25L12835EZNI-10G	wait for P/N
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF8C0	

Configuration Table

	CONFIG-1 16MB	CONFIG-2 12MB	CONFIG-3 8MB
SPI1	16MB	8MB	8MB
SPI2	DY	4MB	DY
R429	DY	ASM	DY
R431	DY	ASM	DY
R433	DY	ASM	DY
R1375	DY	ASM	DY
R1376	DY	ASM	DY
C471	DY	ASM	DY
R1514	DY	ASM	DY
R149 (p24)	DY	ASM	DY

Logic



SO8 and WSON8 are both supported!

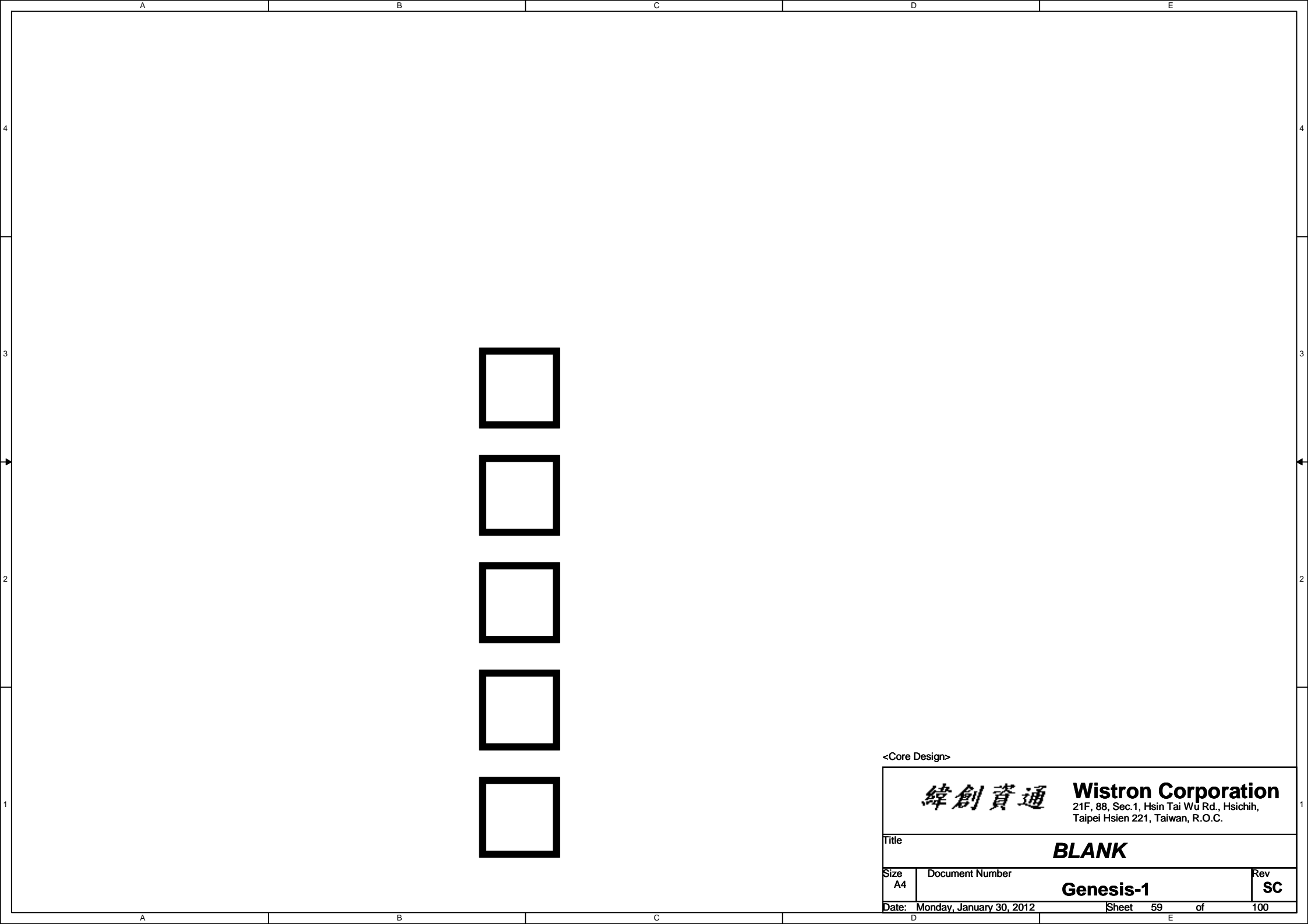
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Title: **SPI&LPC debug card**

Size: A3 Document Number: **Genesis-1** Rev: **SC**

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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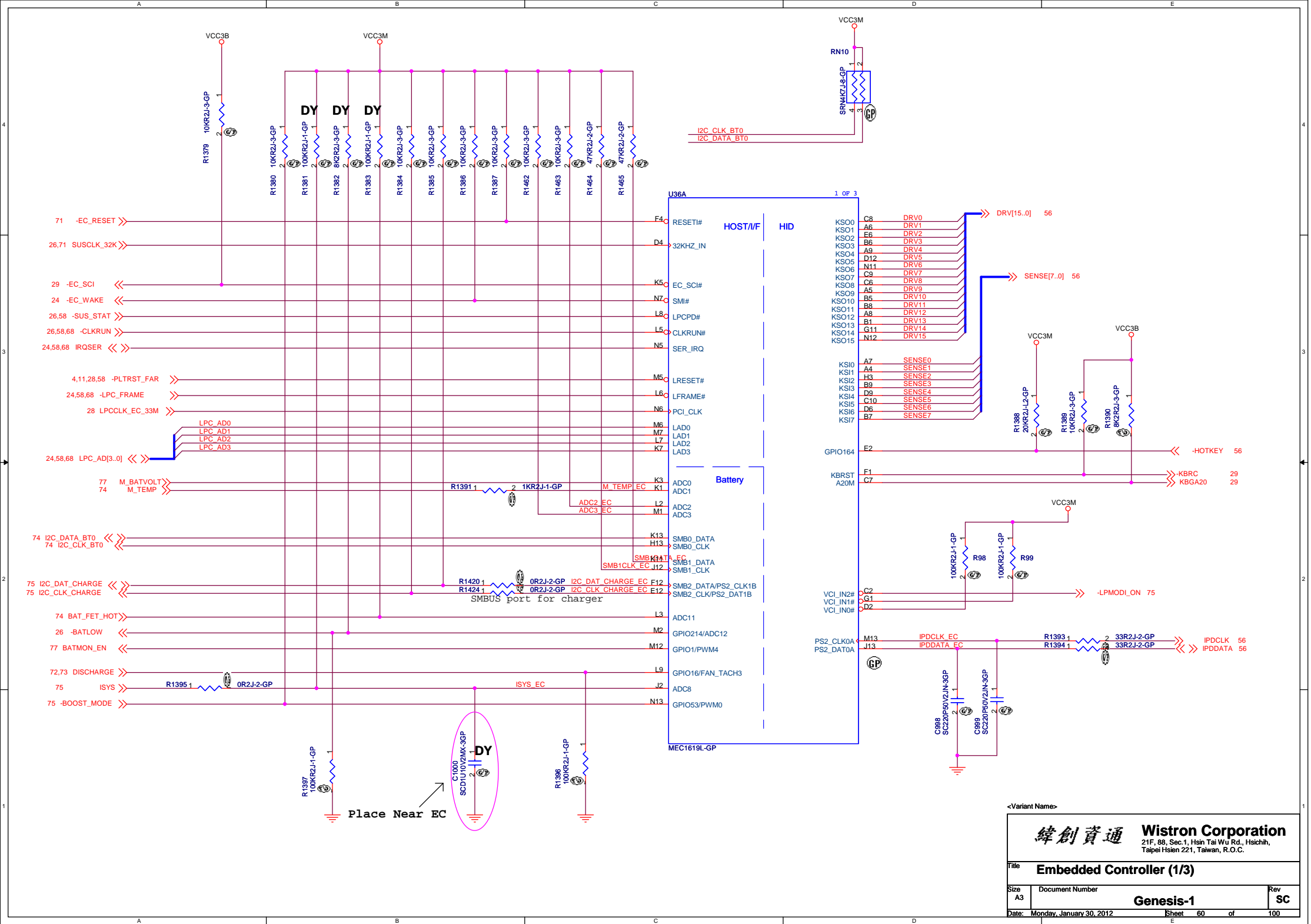
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Rev
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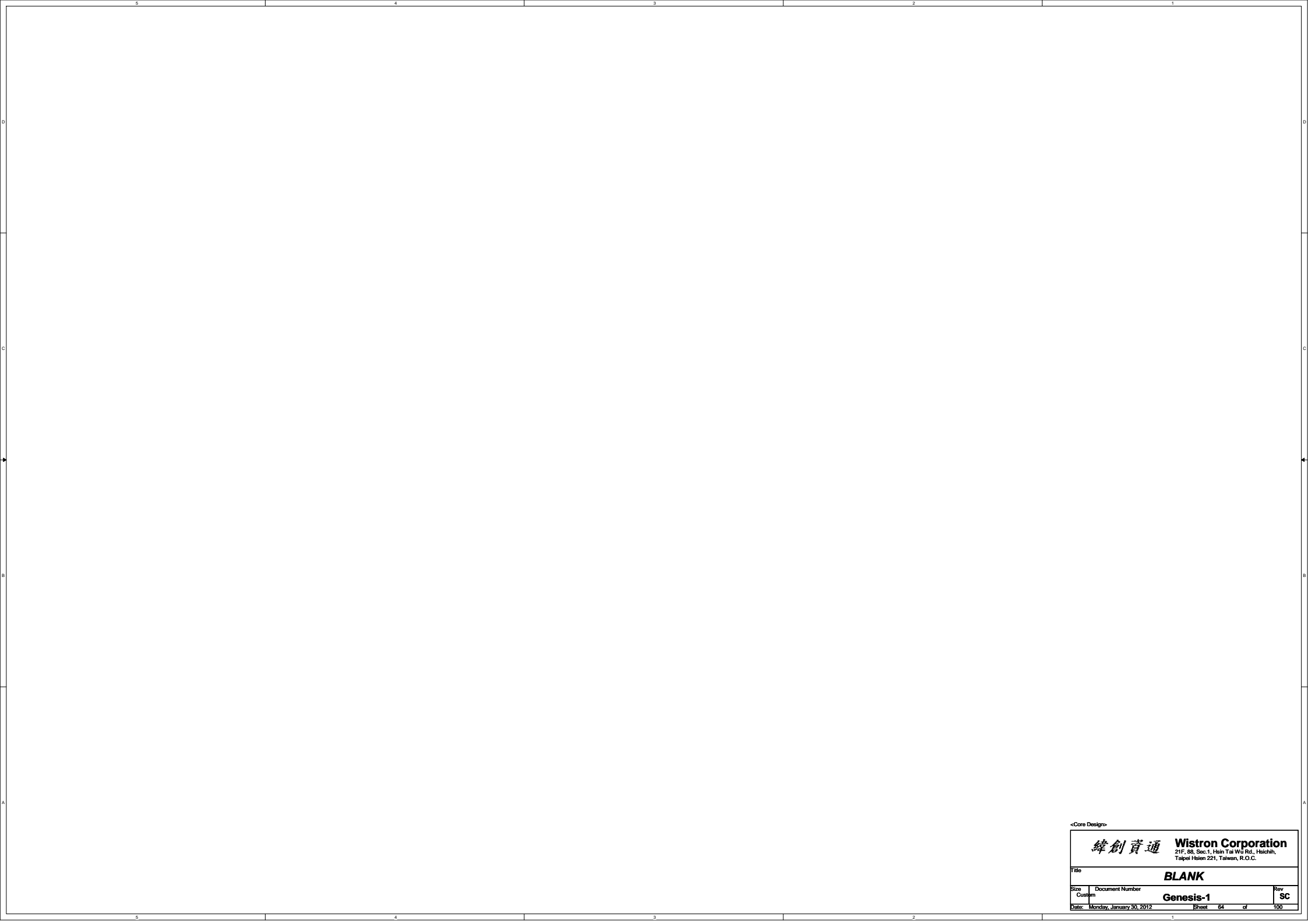
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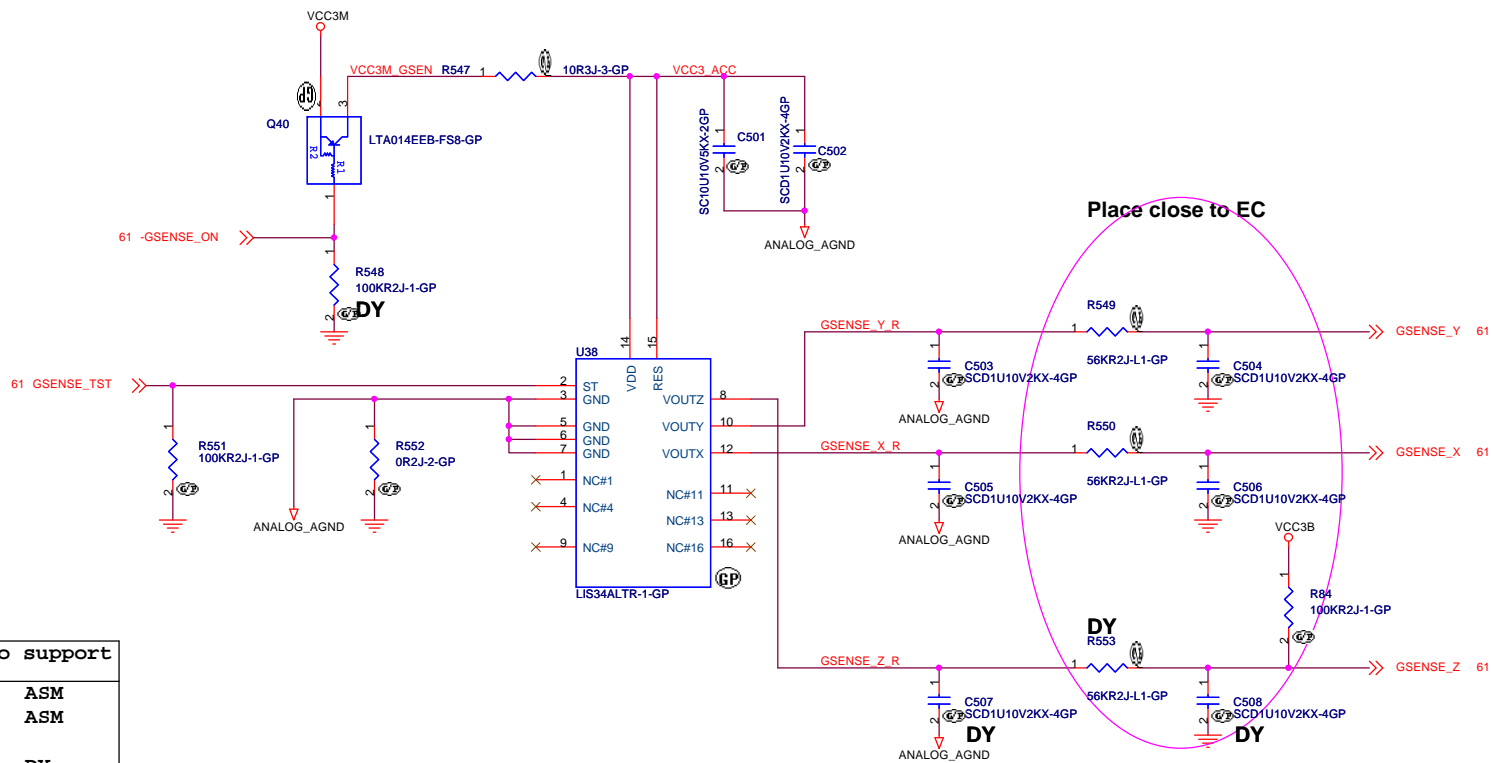
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G-sensor	support	no support
R548	DY	ASM
R551	ASM	ASM
U38	ASM	DY
Q40	ASM	DY
R547	ASM	DY
C501	ASM	DY
C502	ASM	DY
R552	ASM	DY
C503	ASM	DY
R549	ASM	DY
C504	ASM	DY
C505	ASM	DY
R550	ASM	DY
C506	ASM	DY
C507	DY	DY
R553	DY	DY
C508	DY	DY
R84	ASM	ASM

U38

Primary	STMicro LIS34AL	41R0828AA
Second	Kionix KXTC8-2850	74.KXTC8.0BZ
Third		

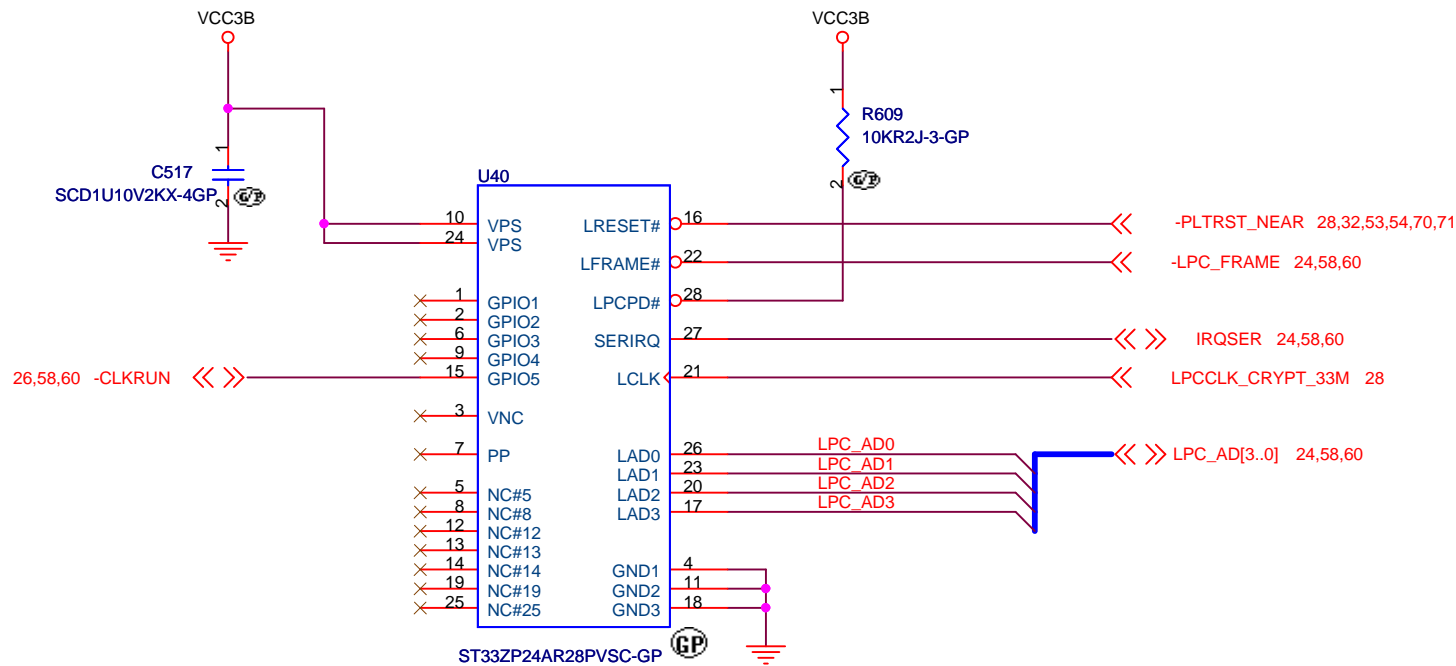
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(1) Avoid routing under DCDC switching area.

Width = 6 mil & Spacing = 10 mil
for three Output traces

<Core Design>

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Title			
G-SENSOR			
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TPM P/N		Firmware
SDV / FVT	ST33ZP24AR28PVRC	1.2.C.0
SIT	ST33ZP24AR28PVSC	1.2.D.0

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

TPM

Size
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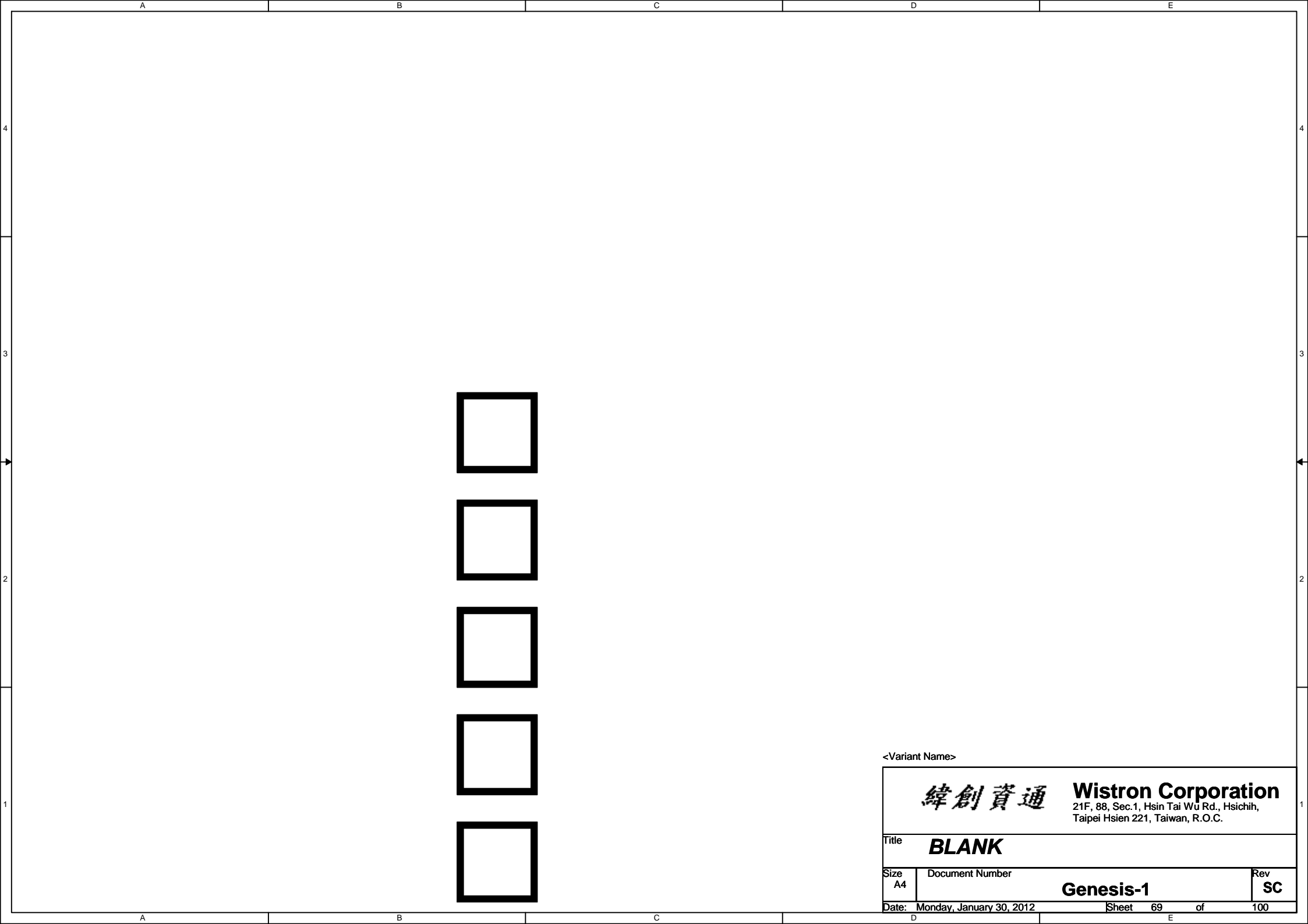
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A

B

C

D

E

4

4

3

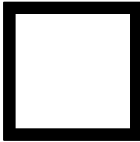
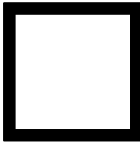
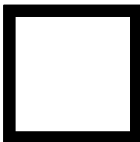
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2

2

1

1



<Variant Name>

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Taipei Hsien 221, Taiwan, R.O.C.

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Document Number

Genesis-1

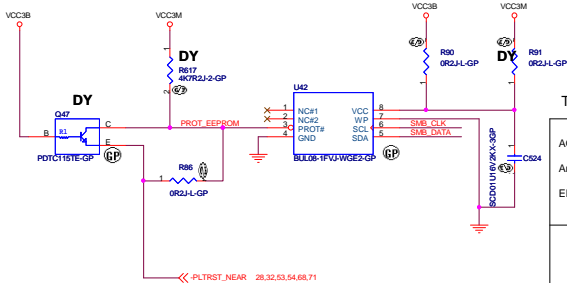
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EEPROM

EEPROM	U42	U36
U42	ASM	DY
C524	ASM	DY
Q47	ASM	DY
R617	ASM	DY

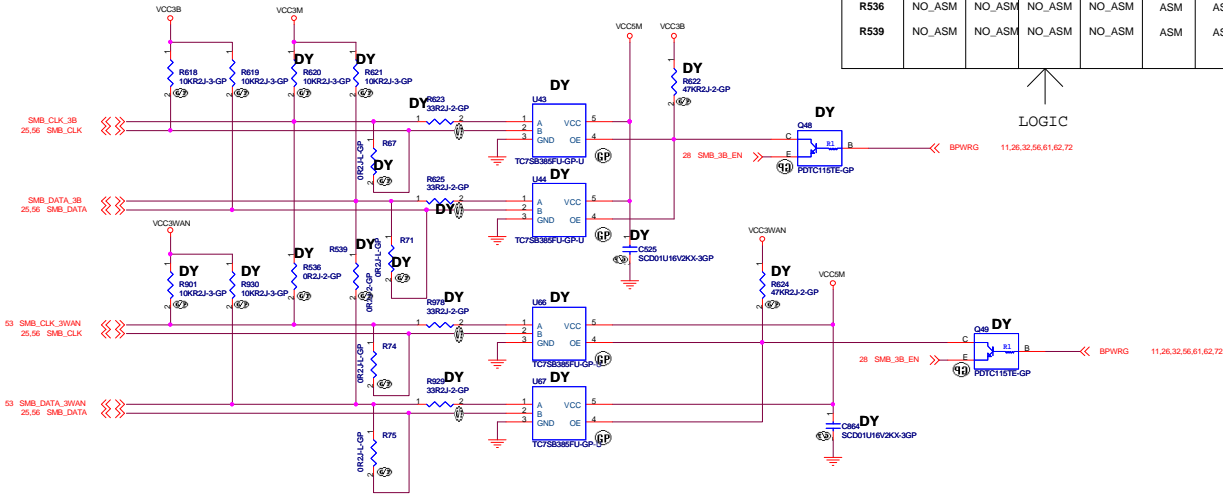


	Vendor	U42	Part Number
1st	ROHM	BUL08-1FVJ-W	72.BUL08.A0Q
2nd	PHILIPS	PCA24S08ADP	72.24S08.A0Q
3rd	Sanyo	LE26CAP08TT	72.26C08.00R

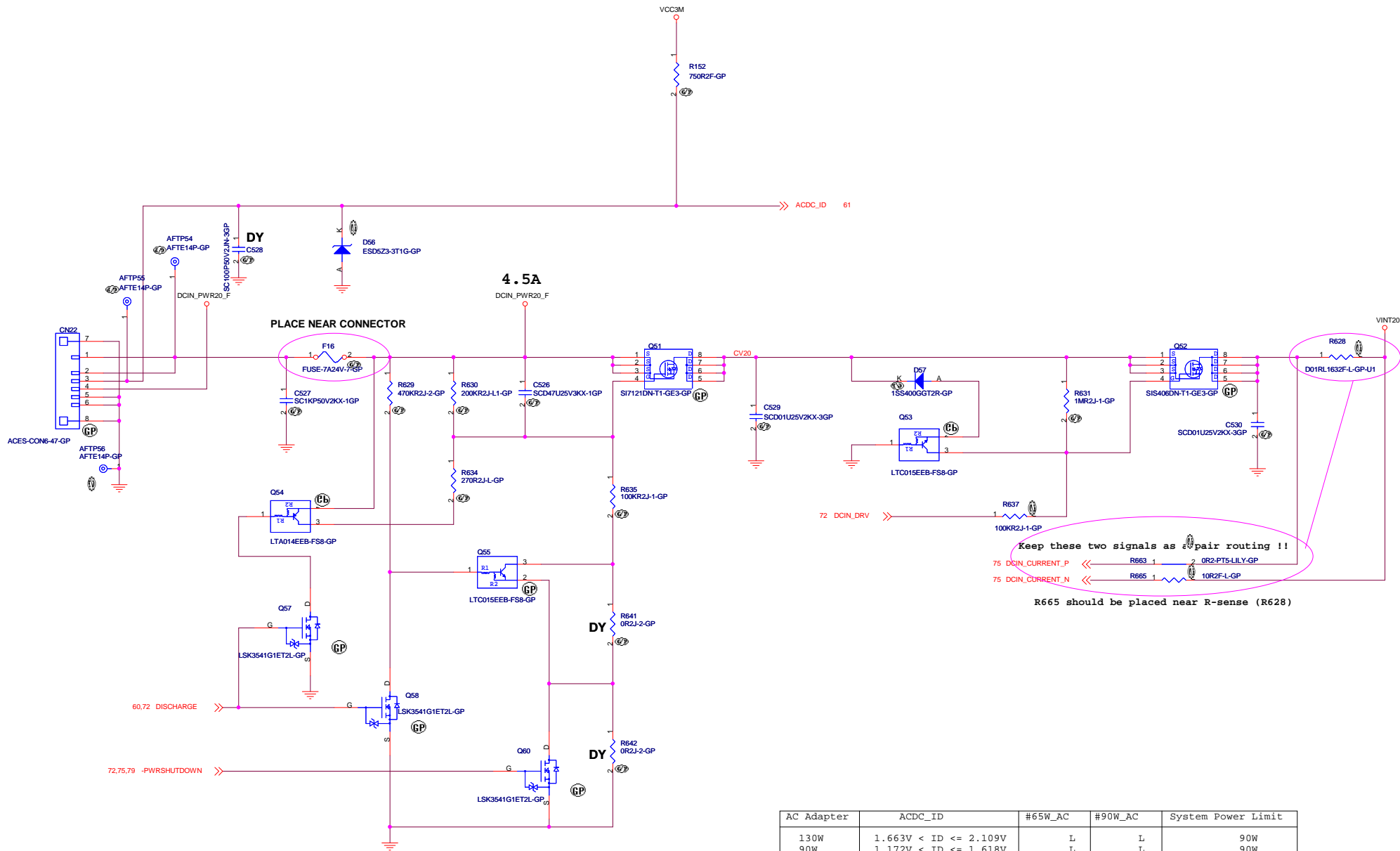
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Anti Theft	YES	YES	NO	NO	YES	YES	NO	NO
EEPROM	U42	U36	U42	U36	U42	U36	U42	U36
U66	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
U67	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
C864	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R978	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R929	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R901	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R930	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
R624	ASM	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
Q49	ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM	NO_ASM
Q48	ASM	NO_ASM	ASM	NO_ASM	ASM	NO_ASM	ASM	NO_ASM
R536	NO_ASM	NO_ASM	NO_ASM	NO_ASM	ASM	NO_ASM	NO_ASM	NO_ASM
R539	NO_ASM	NO_ASM	NO_ASM	NO_ASM	ASM	ASM	NO_ASM	NO_ASM

LOGIC







PEAK SHIFT	YES	NO
R641	NO-ASM	ASM
R629	ASM	NO-ASM
Q58	ASM	NO-ASM
Q55	ASM	NO-ASM

Logic

AC Adapter	ACDC_ID	#65W_AC	#90W_AC	System Power Limit
130W	1.663V < ID <= 2.109V	L	L	90W
90W	1.172V < ID <= 1.618V	L	L	90W
65W	0.693V < ID <= 1.134V	L	H	65W
45W	0.234V < ID <= 0.663V	H	H	45W

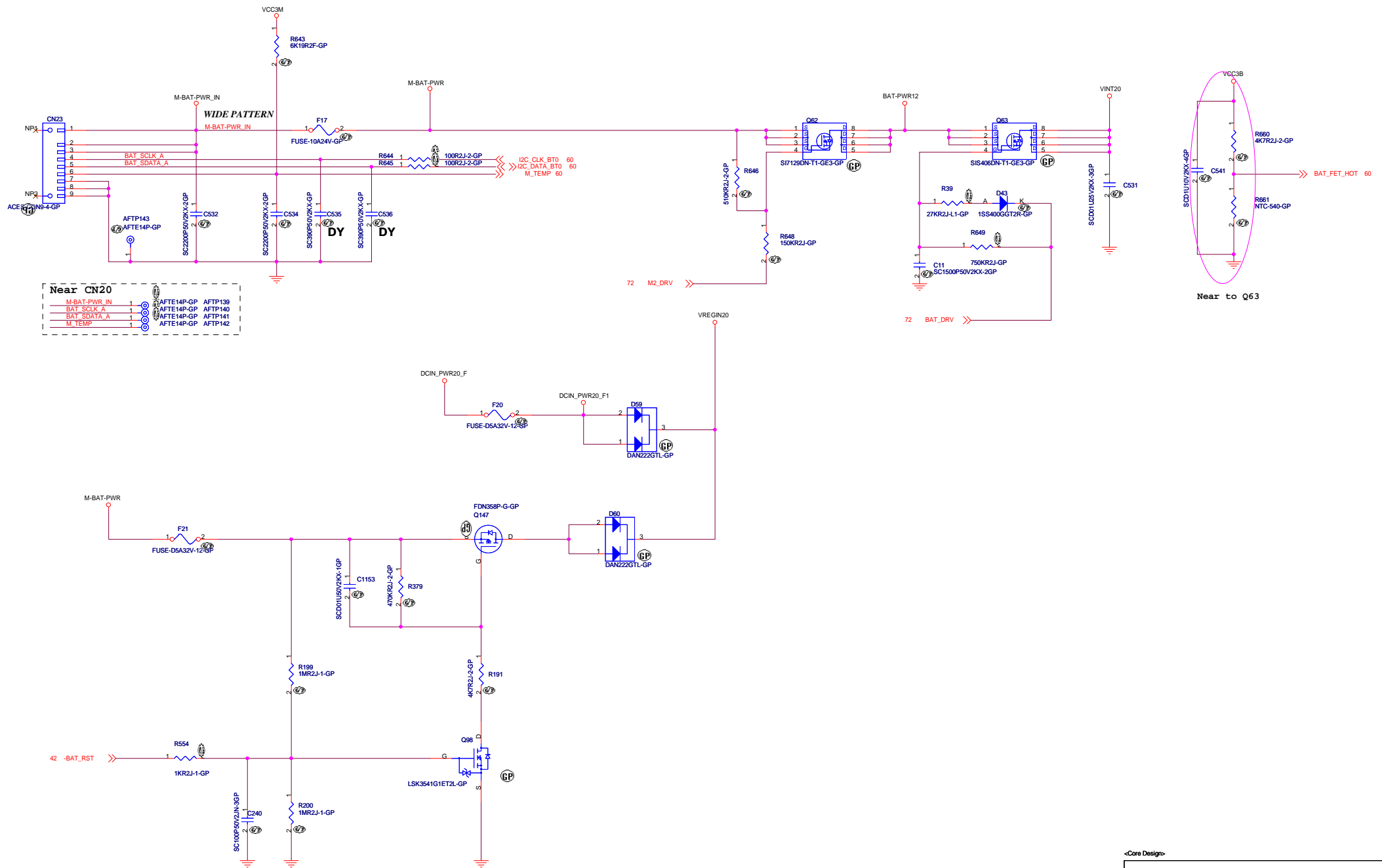
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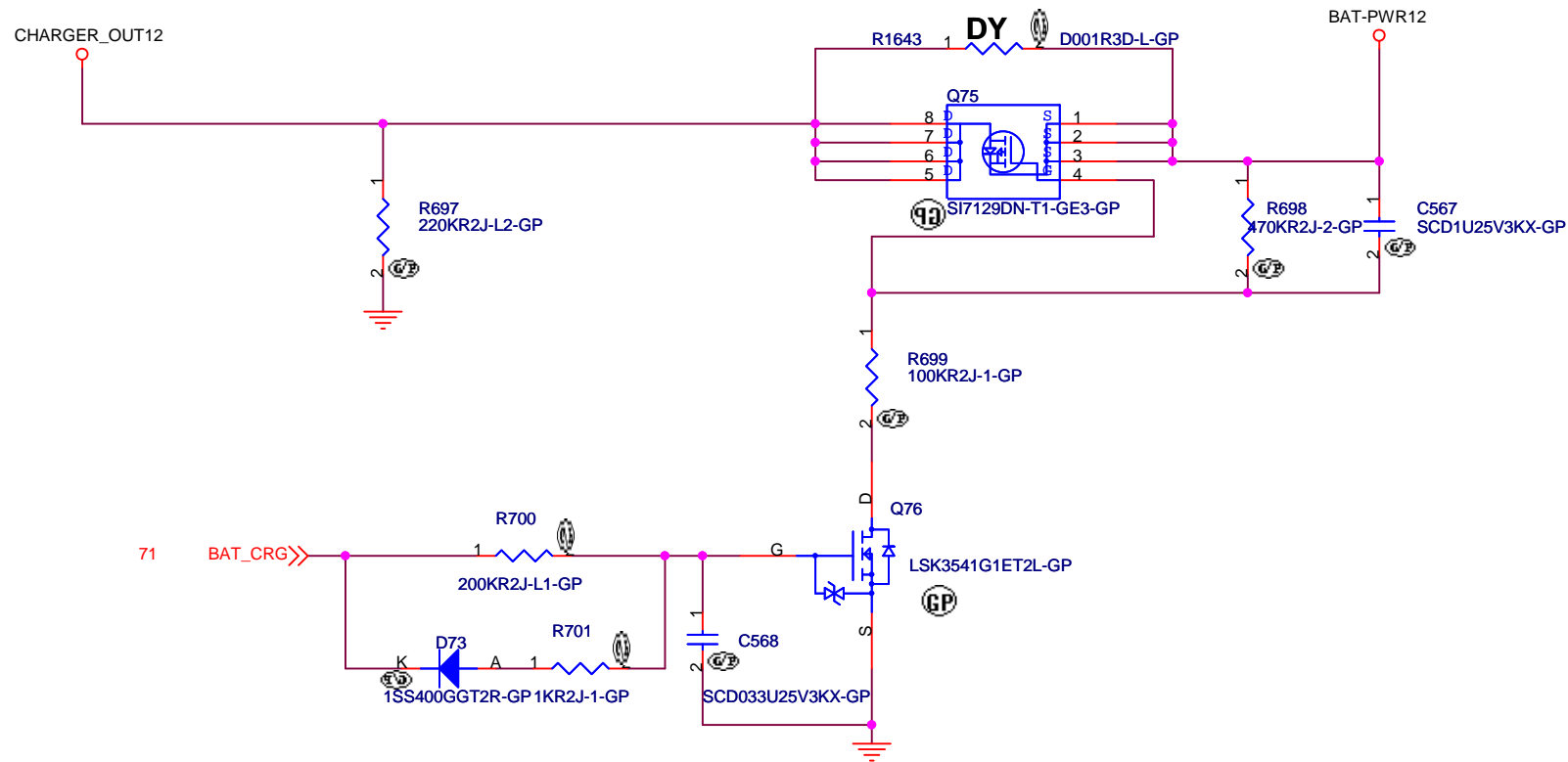
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Size: Custom Document Number: **Genesis-1** Rev: **SC**

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<Core Design>



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

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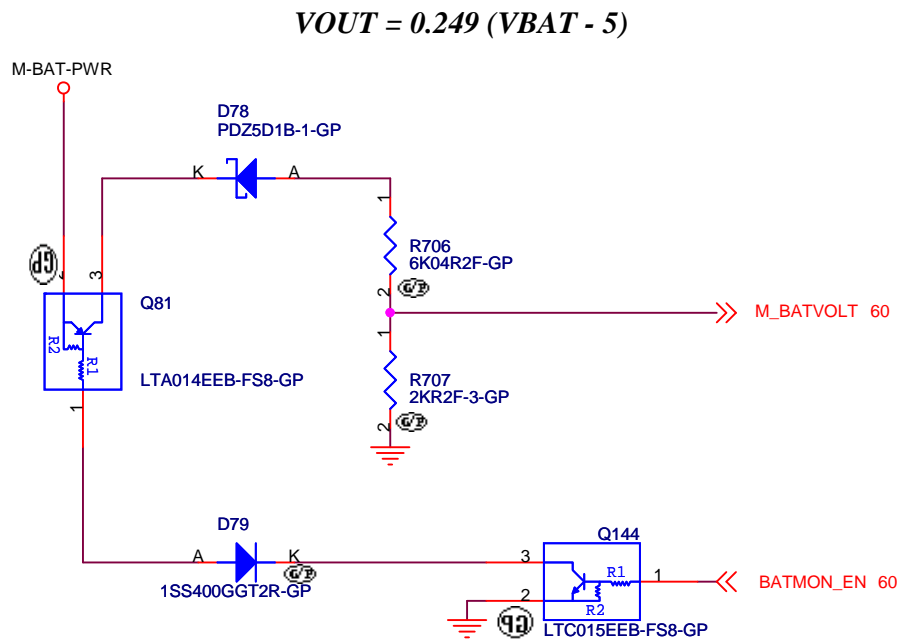
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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

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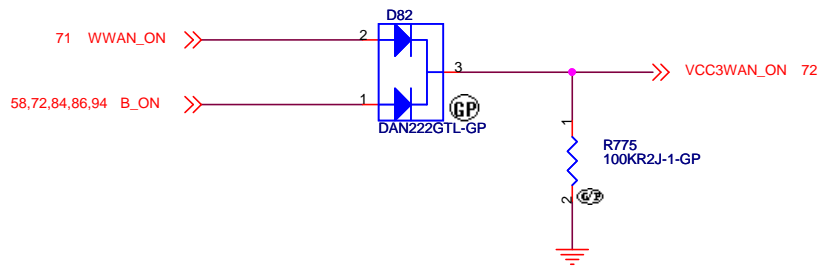
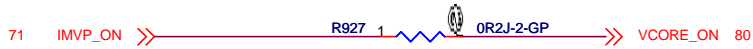
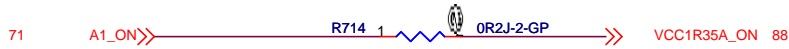
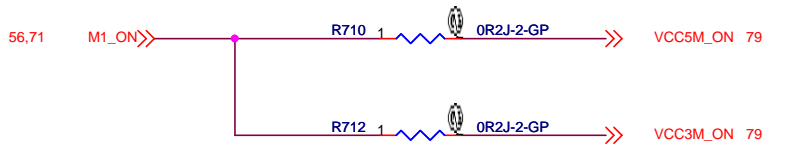
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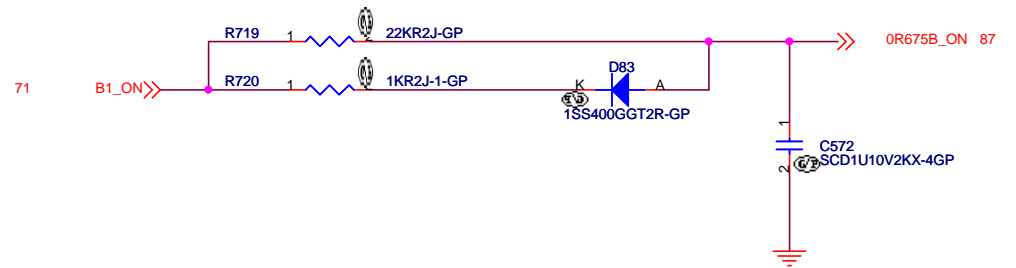
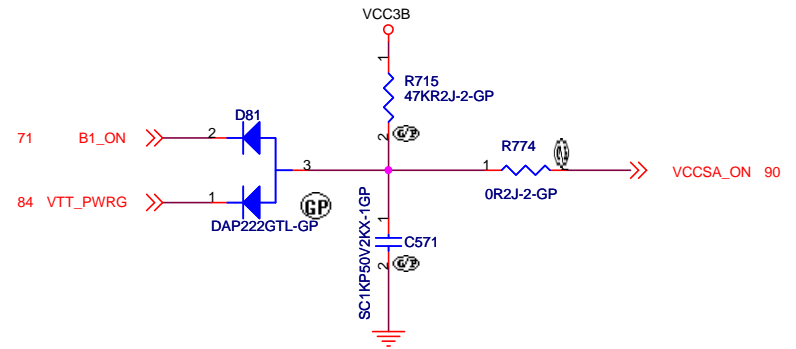
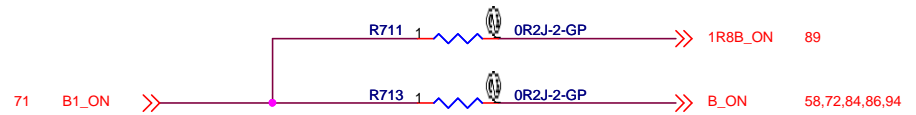
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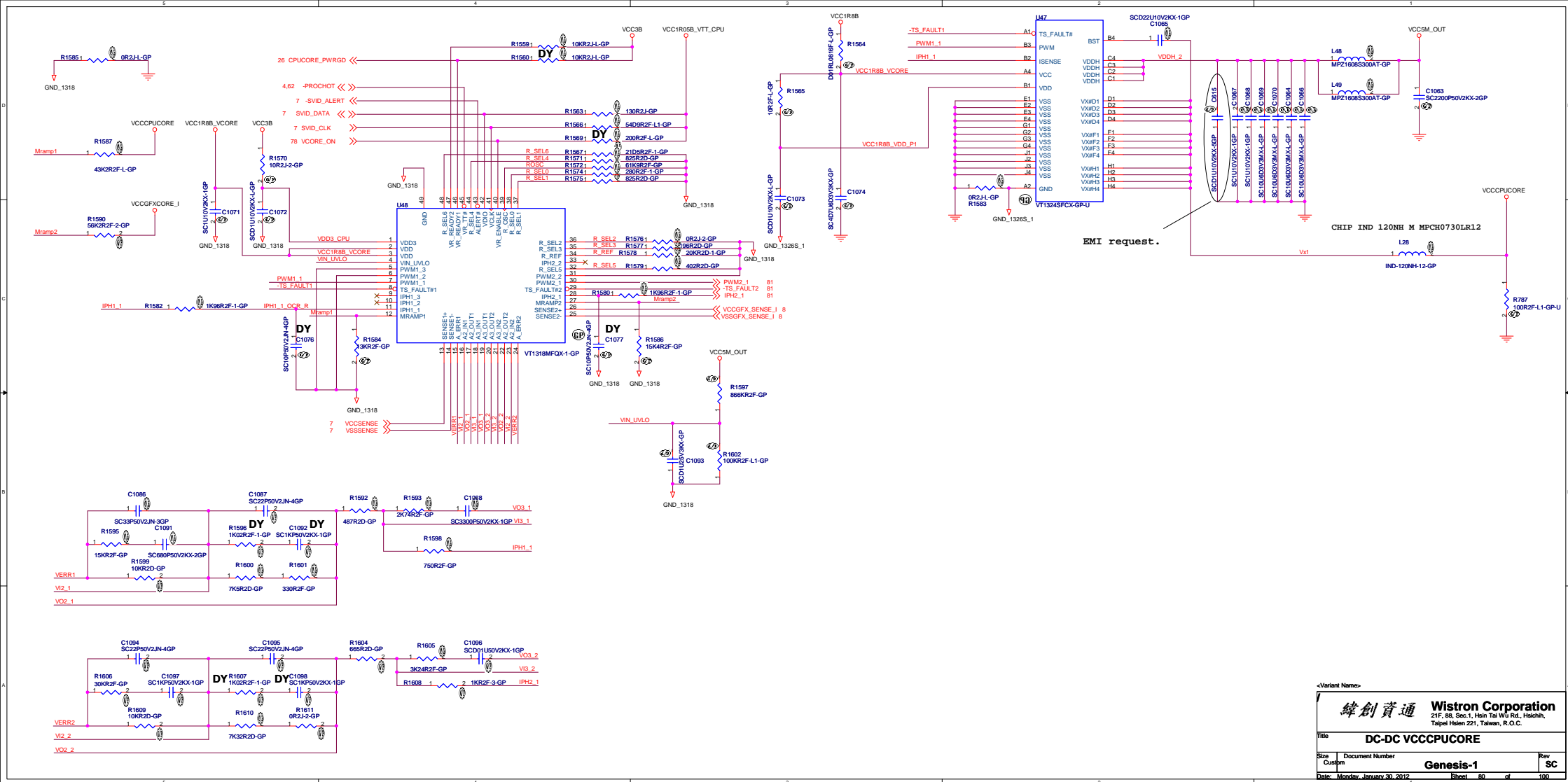
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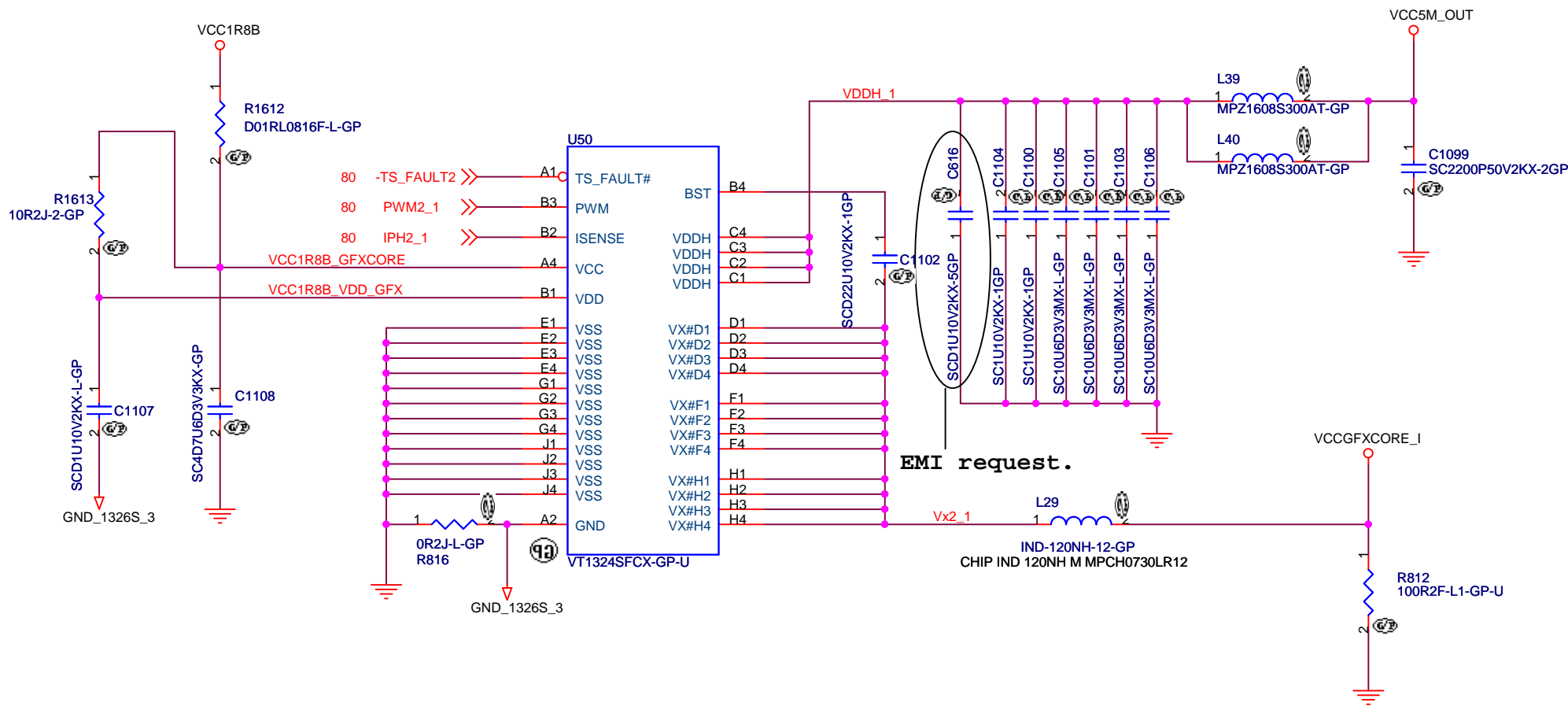
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

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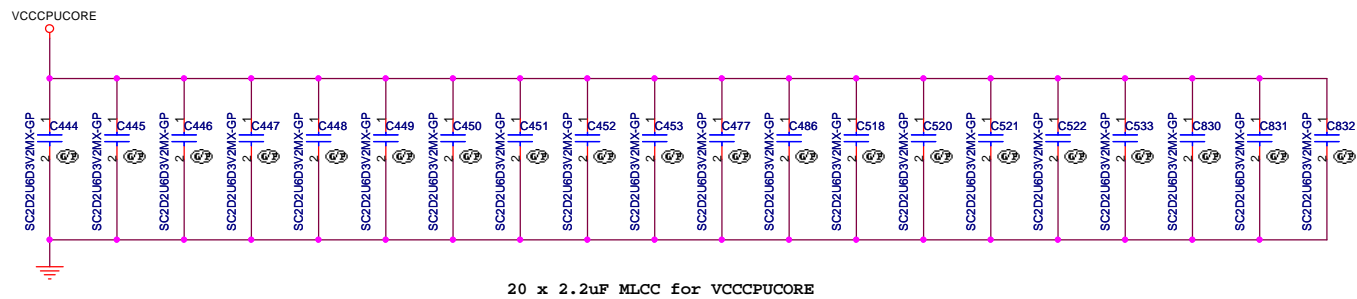
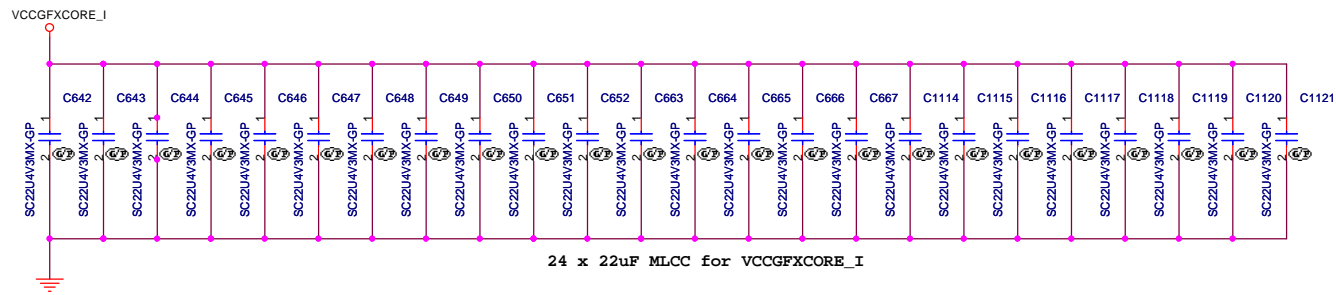
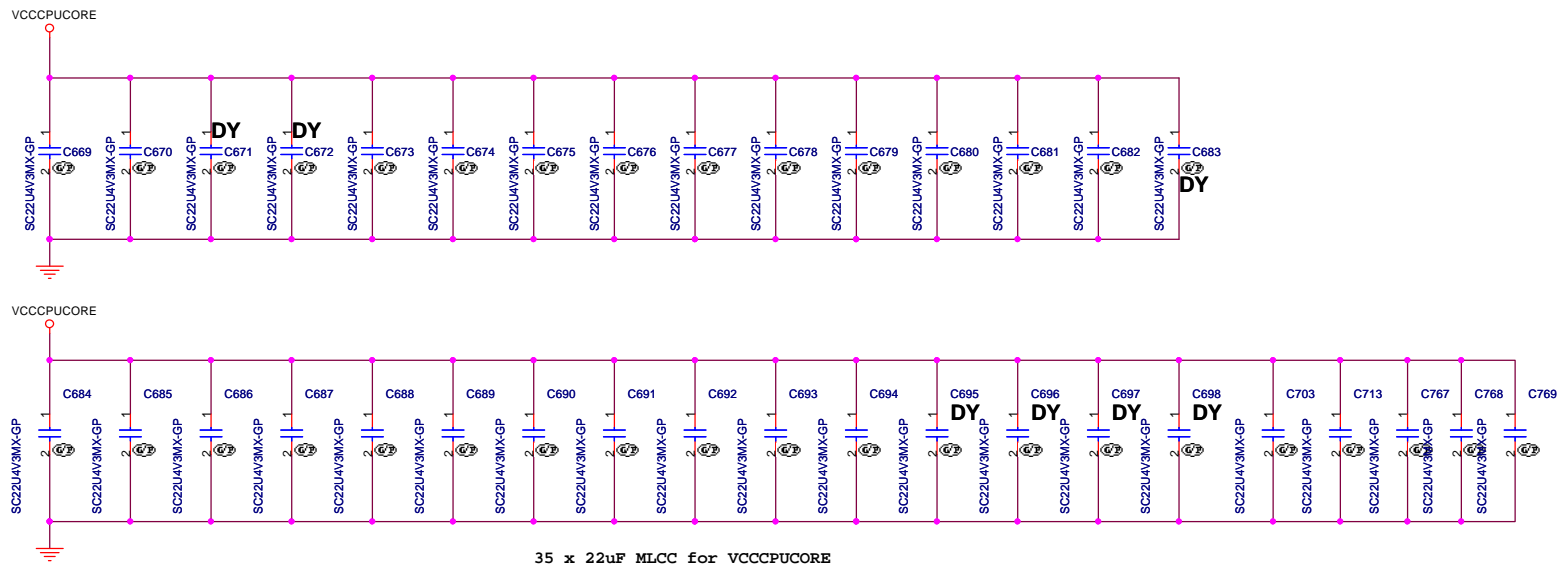
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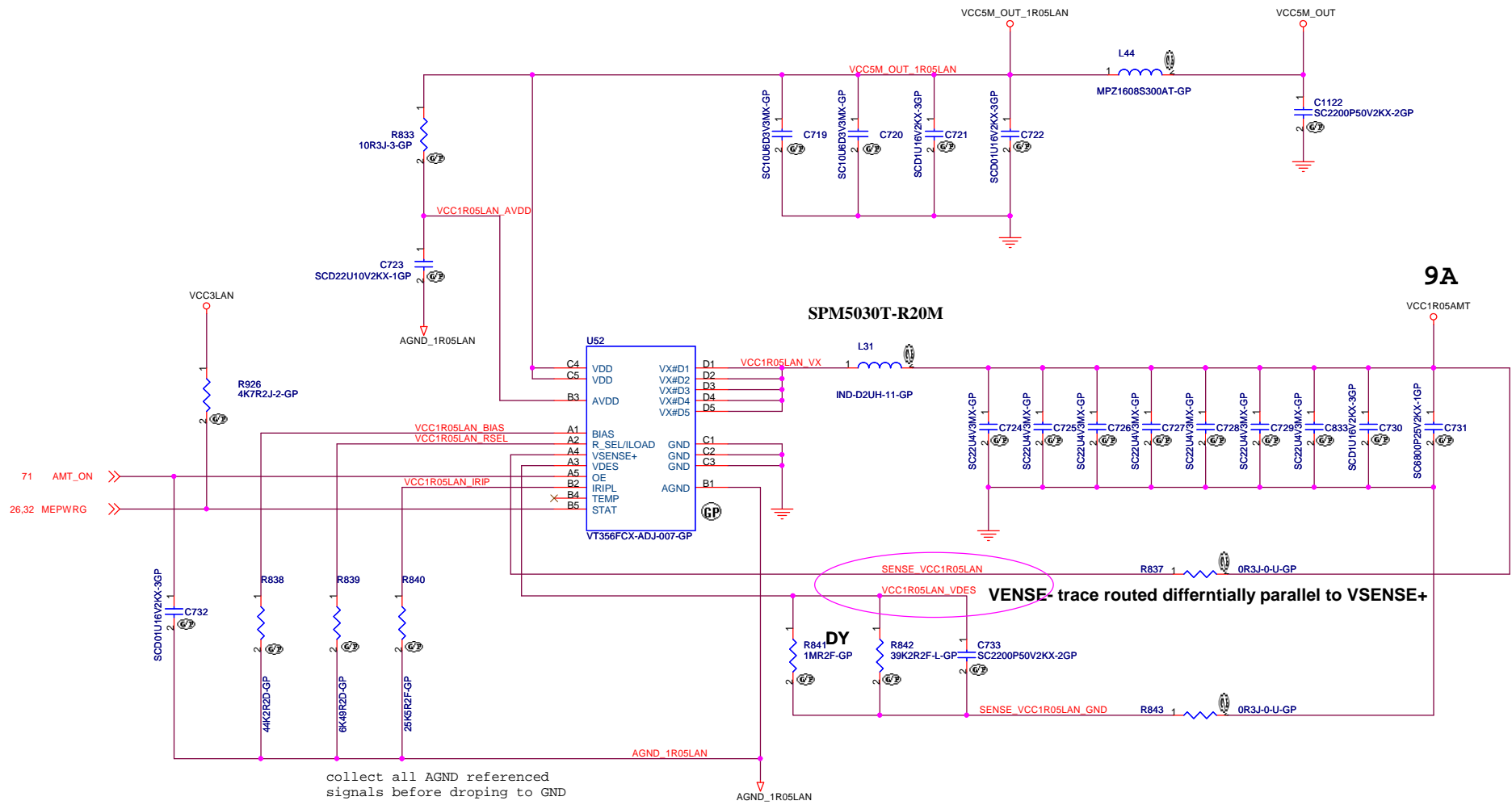
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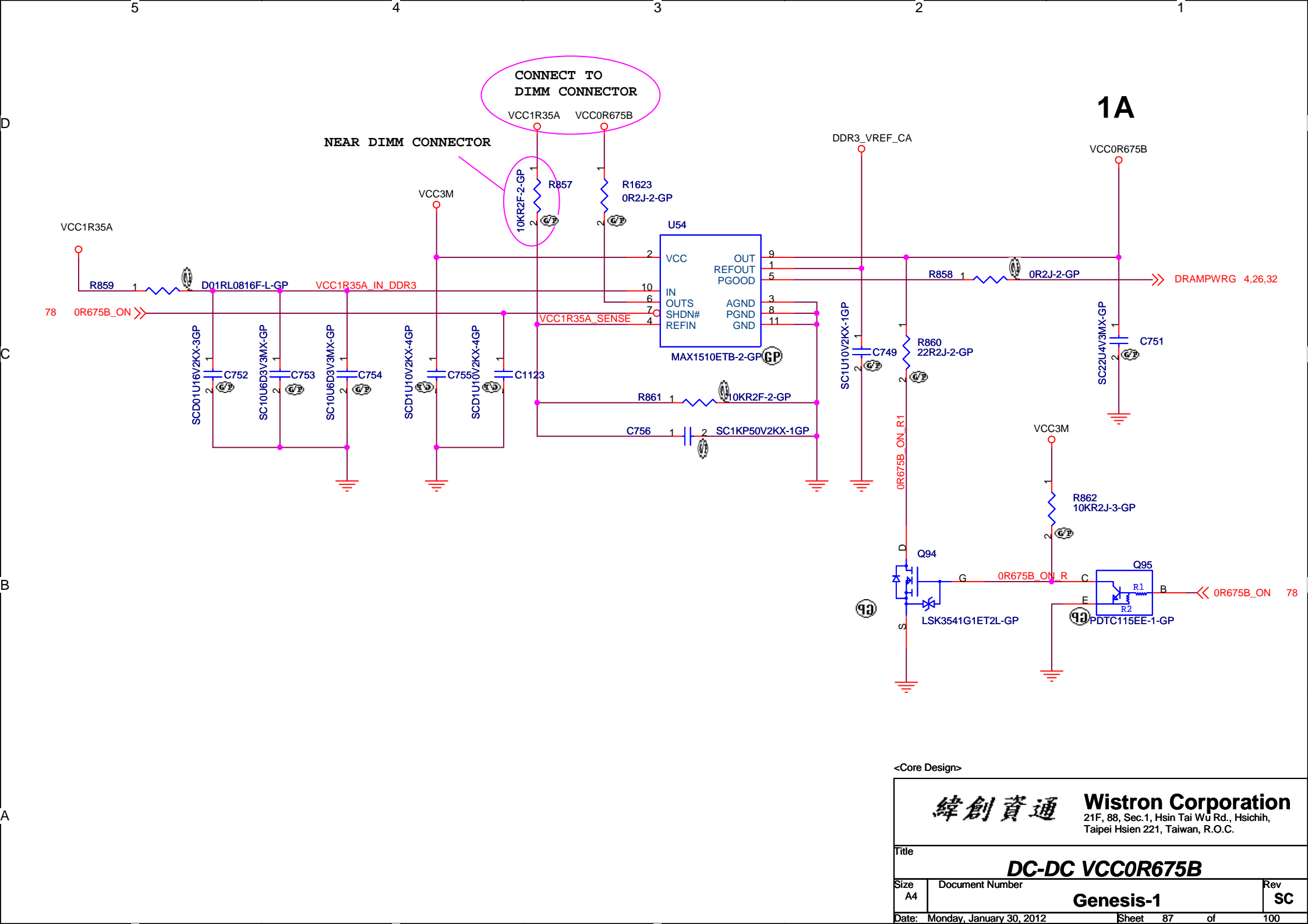
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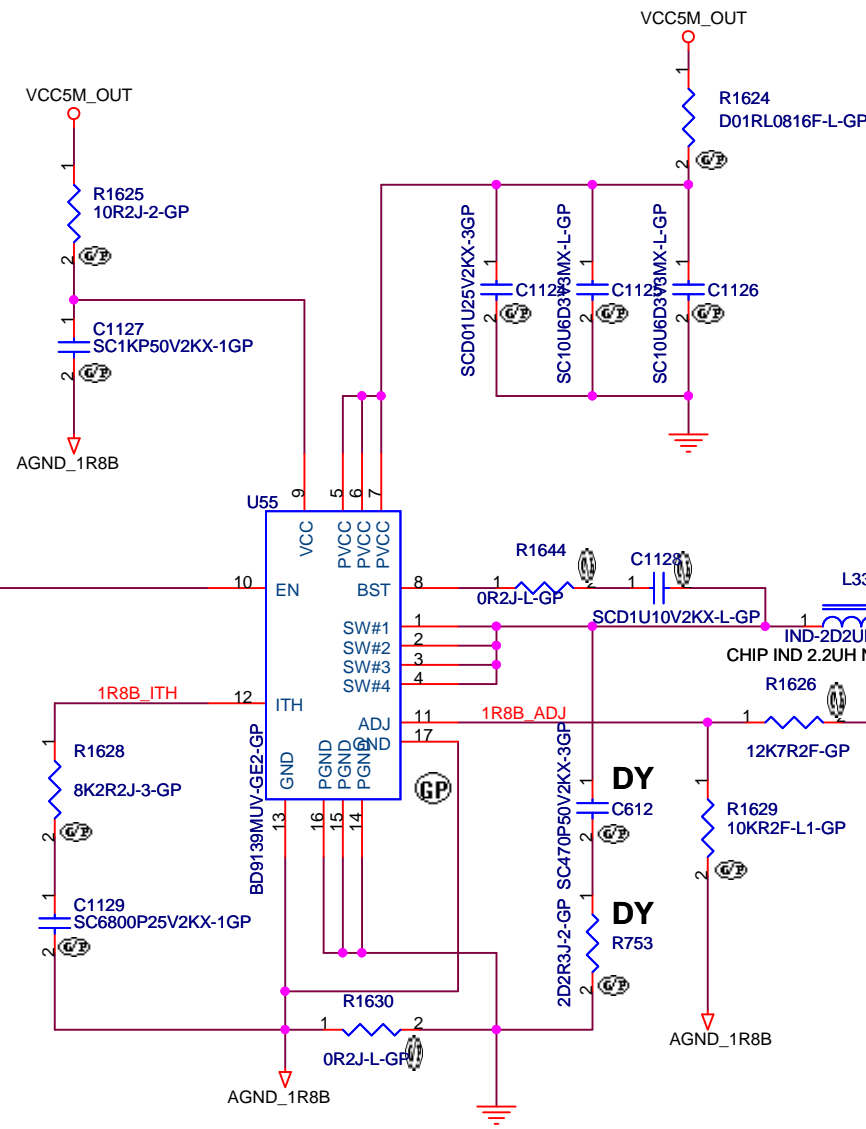
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L33

supplier	Vendor P/N	Wistron P/N
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Taiyo-Yuden	NRS5024T-2R2NMGJ	68.2R21E.10F

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Taipei Hsien 221, Taiwan, R.O.C.

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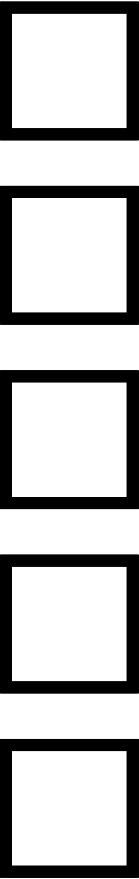
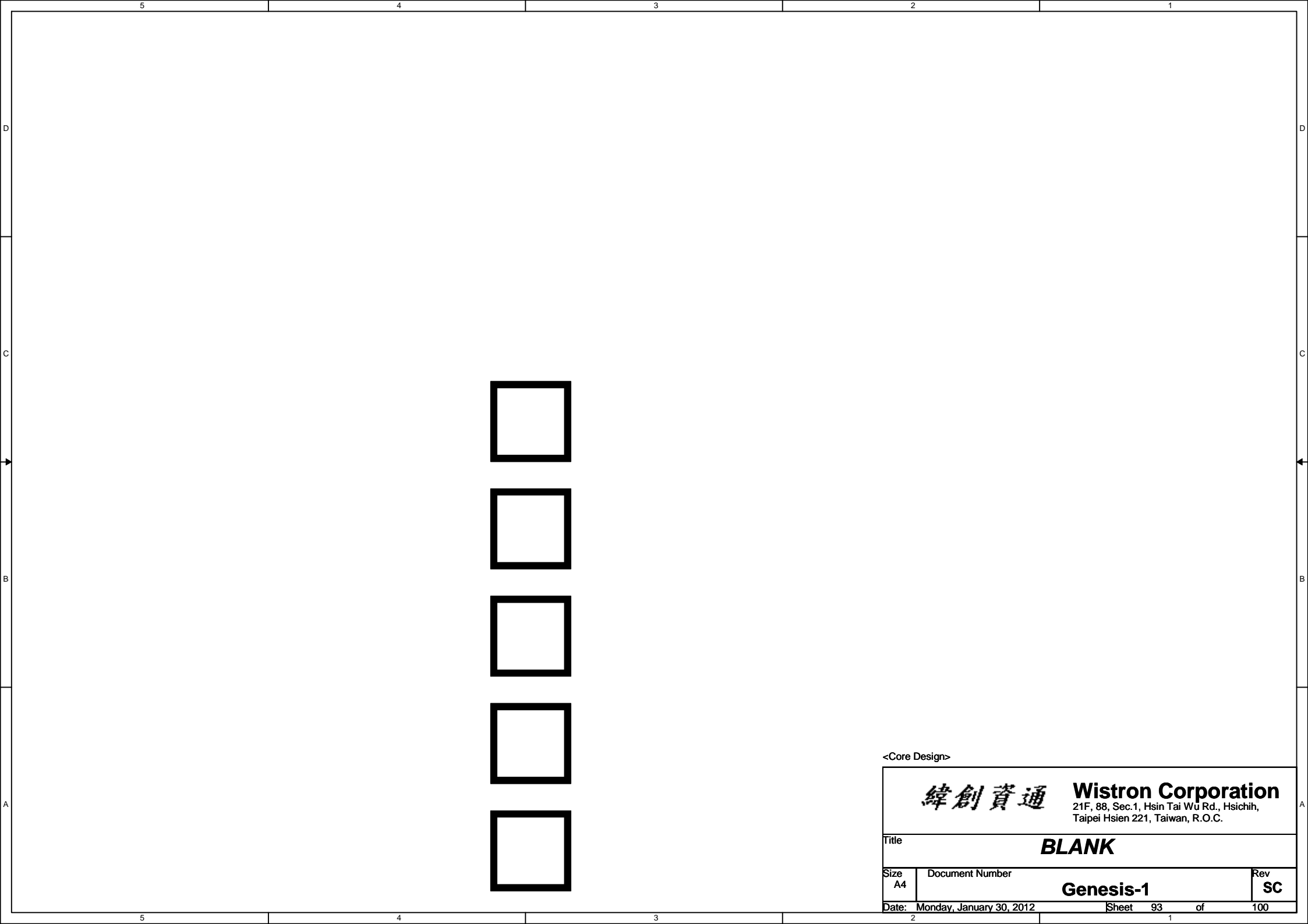
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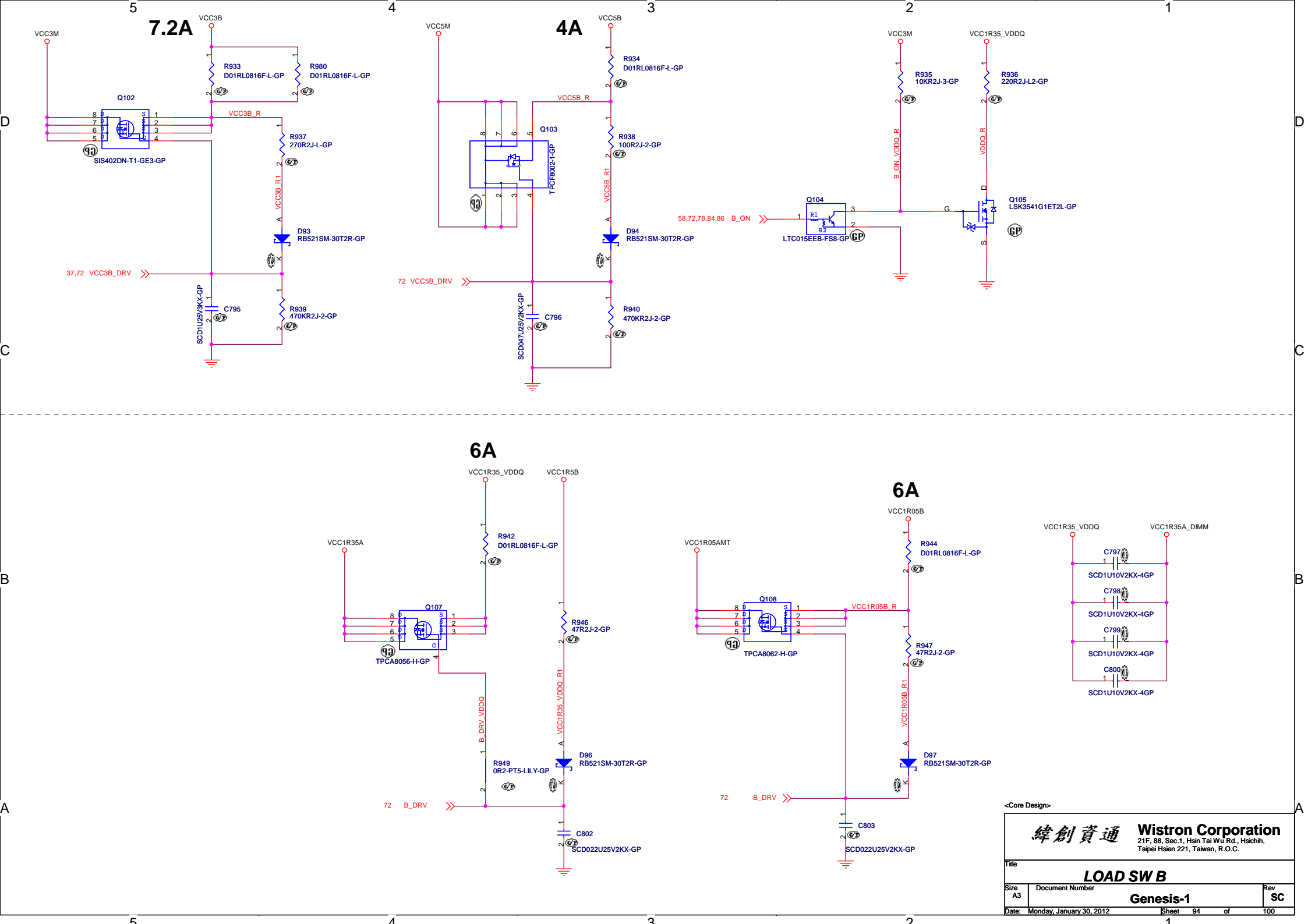
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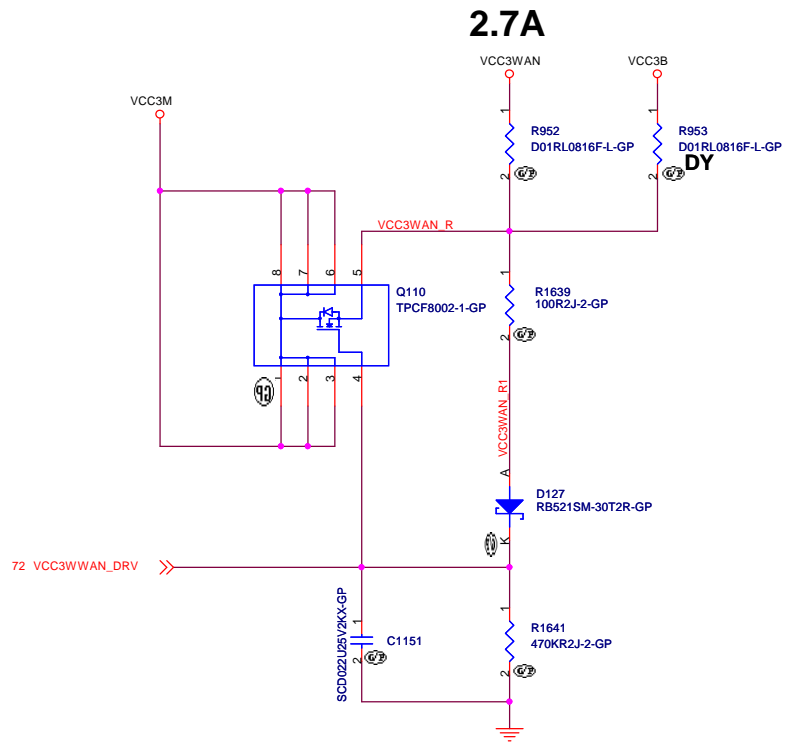
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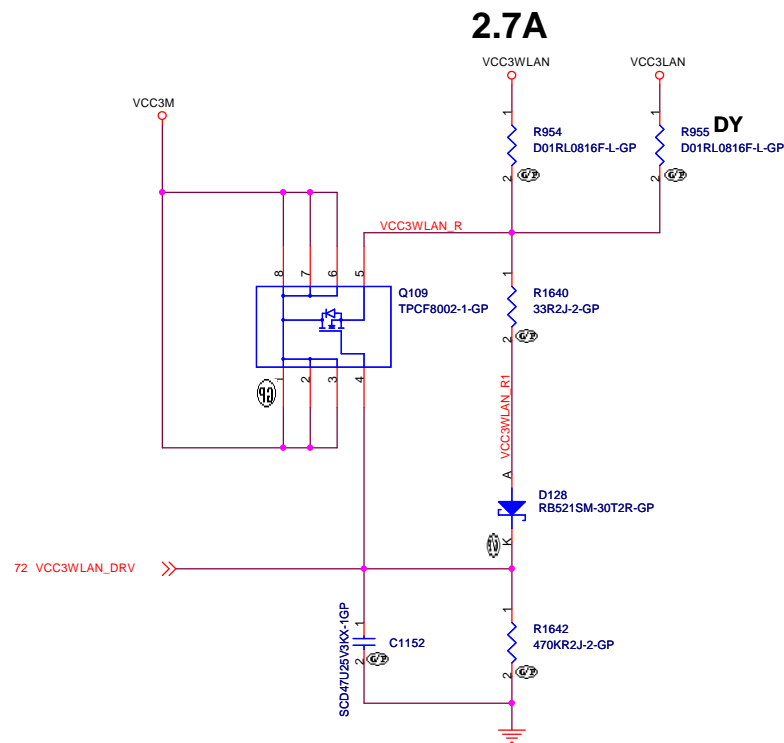
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D127	ASM	DY
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Logic



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Taipei Hsien 221, Taiwan, R.O.C.

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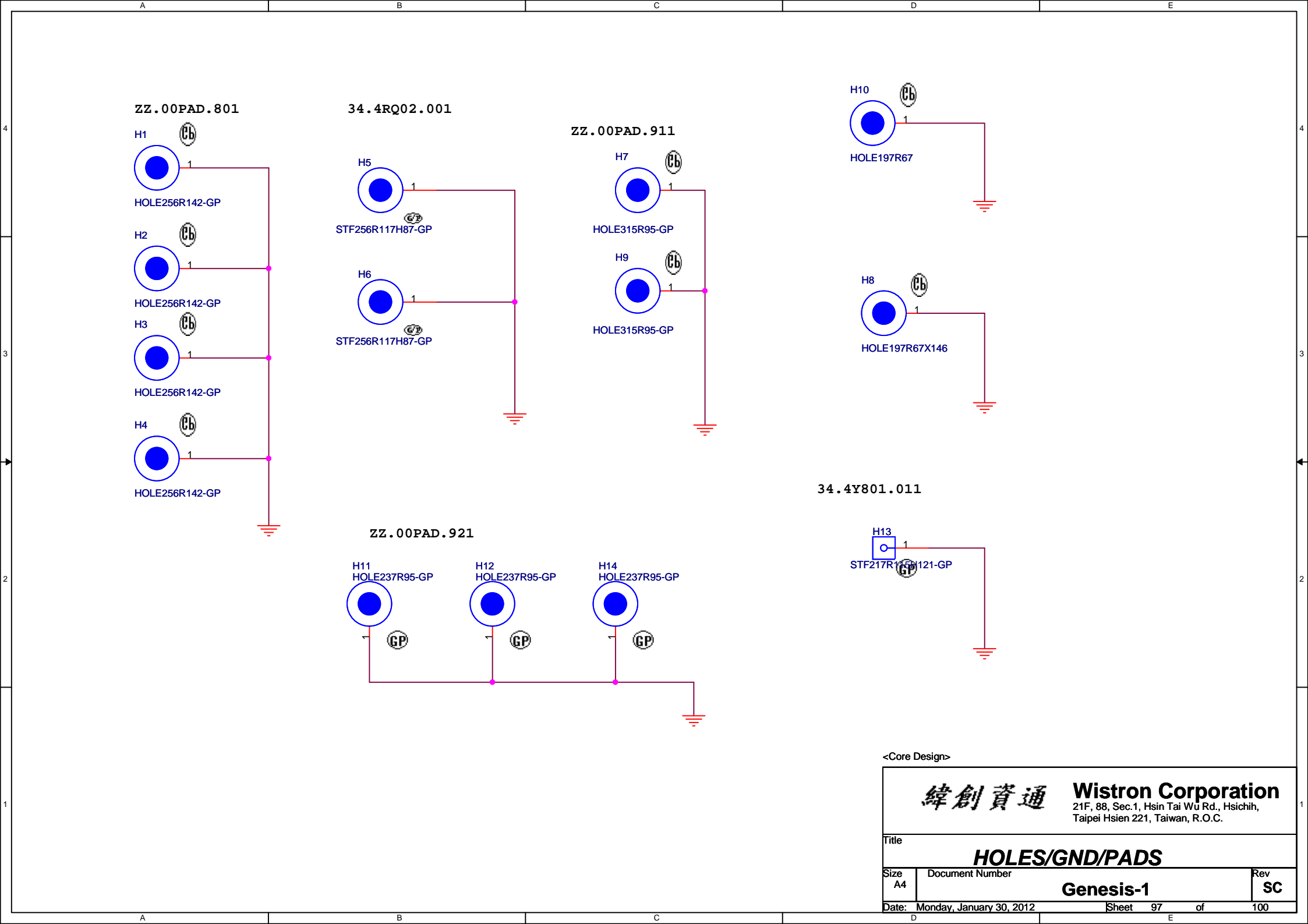
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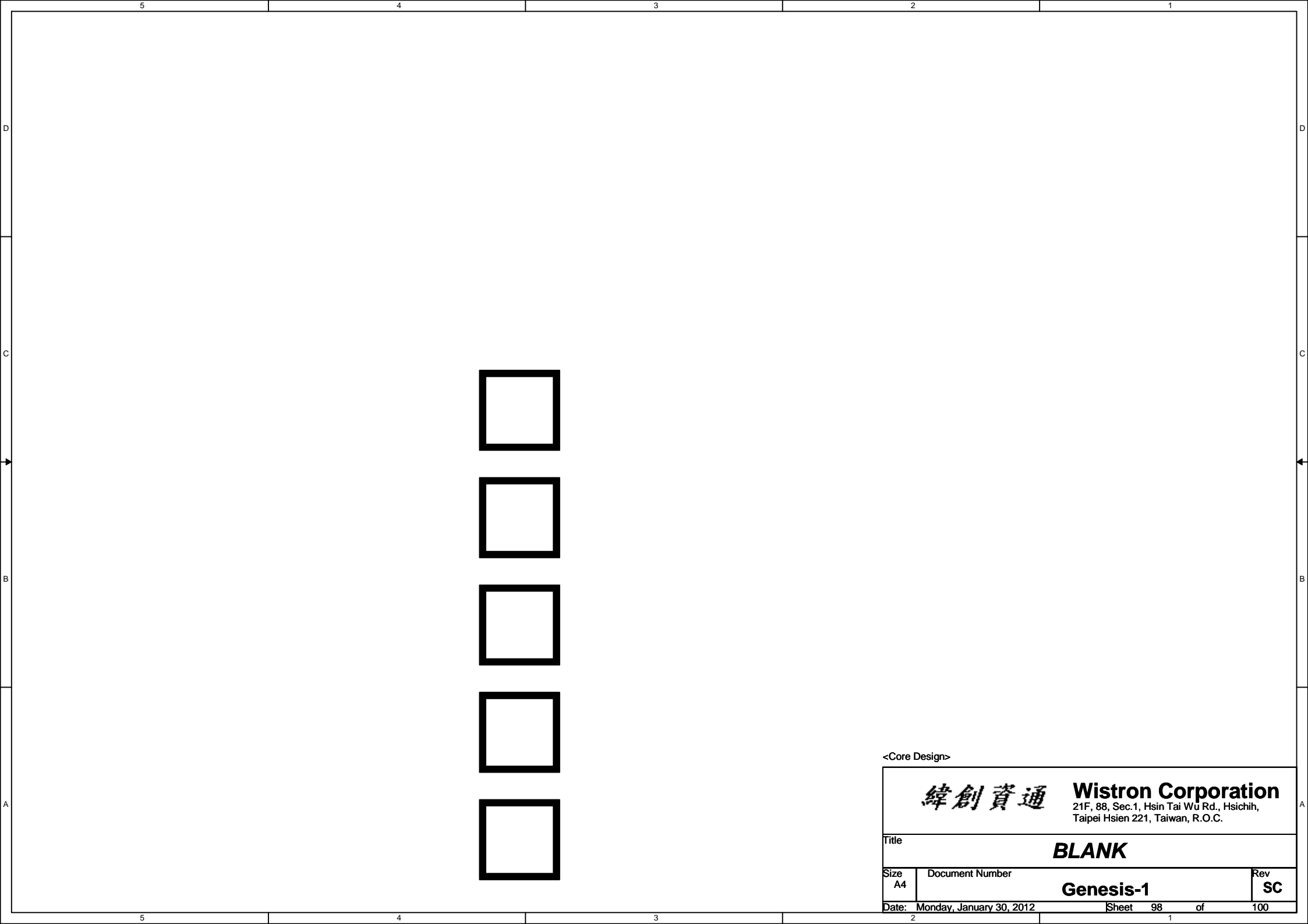
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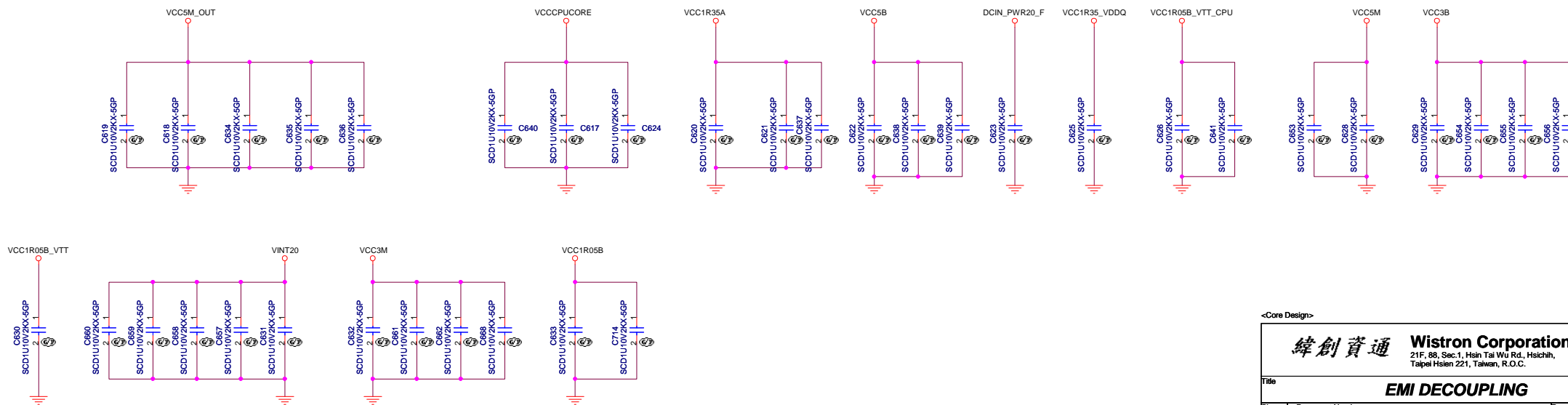
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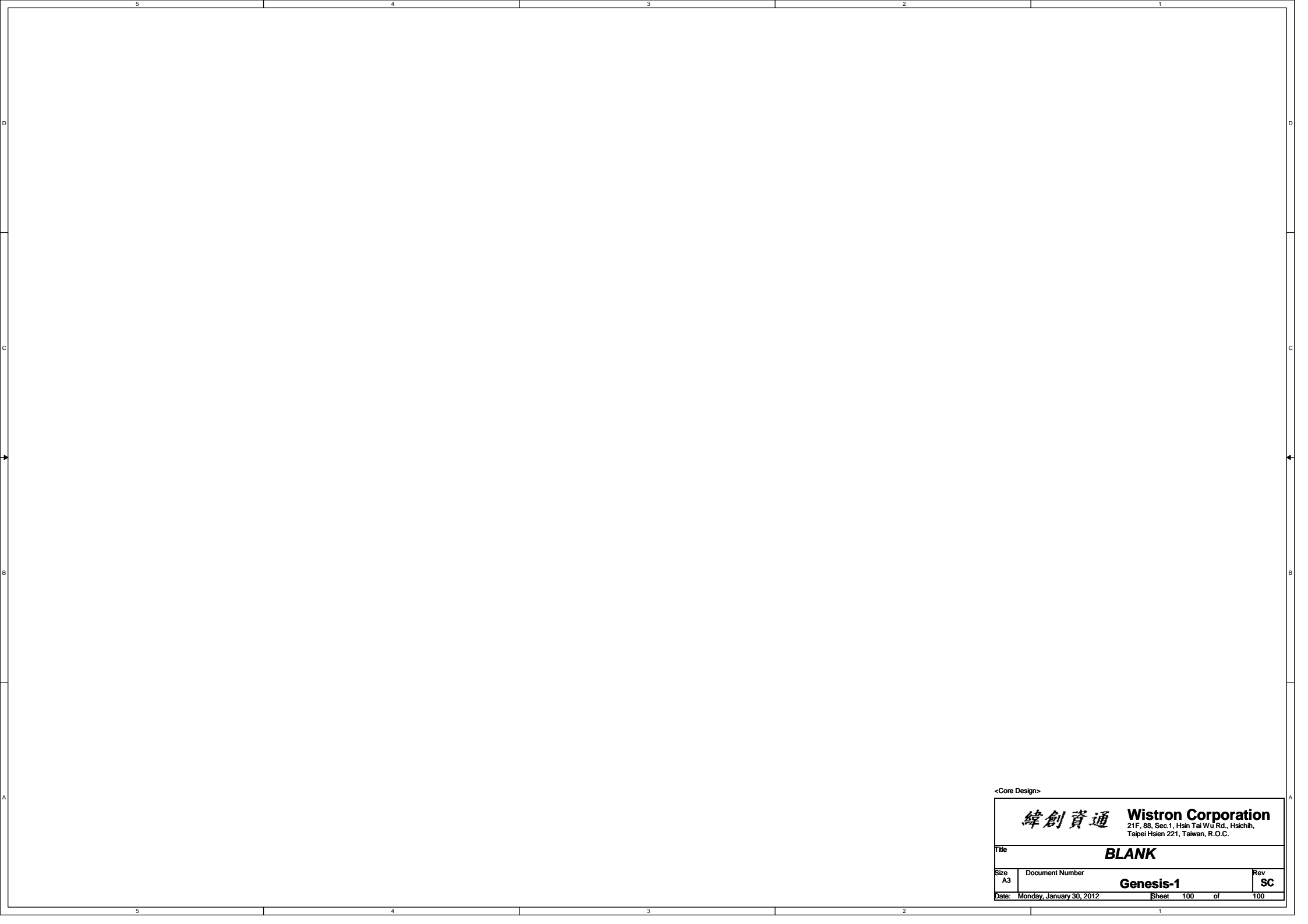
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RF decoupling caps

named as RFCxxx

Long power trace EMI decoupling caps





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