

Compal Confidential

Model Name : VIUS1

File Name : LA-9611P

BOM P/N:

# Compal Confidential

## M/B Schematics Document

Intel Ivy Bridge Processor with DDRIII + Panther Point PCH

GPU AMD

2012-02-18

REV:0.4

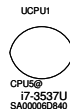
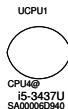
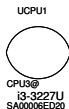
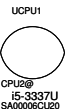
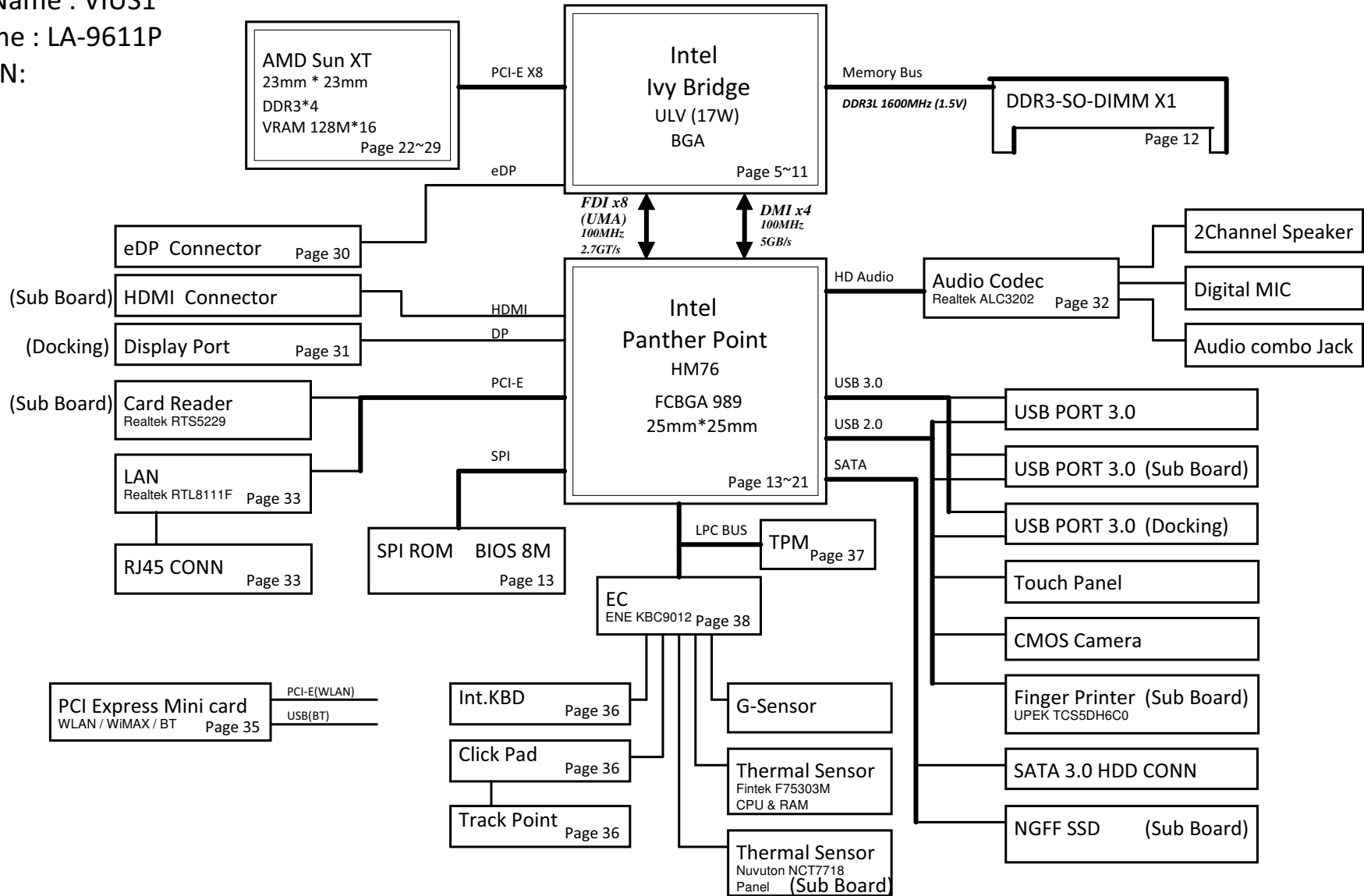
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				Rev	0.4

State	power plane	+B	+5VALW  +3VALW	+1.5V	+5VS +3VS +1.5VS +VCCP +CPU_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS	+3VM  +1.05VM- (SBA Only)
S0		O	O	O	O	O M3 Supported
S3		O	O	O	X	O M3 Supported
S5 S4/AC		O	O	X	X	O M3 Supported
S5 S4/ Battery only		X	X	X	X	
S5 S4/AC & Battery don't exist		X	X	X	X	

SIGNAL STATE	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID	PCB Revision
0	0.1
1	0.2
2	0.3
3	
4	
5	
6	
7	

	USB 2.0	Port	3 External USB Port
EHCI1 USB3.0	UHCI0	0	USB 3.0 Port (I/O Board)
		1	USB 3.0 Port (MB)
	UHCI1	2	USB 3.0 Port (Docking)
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	Touch Panel
		9	(Test point)
	UHCI5	10	Mini Card (WLAN/BT)
		11	FPR
	UHCI6	12	
		13	

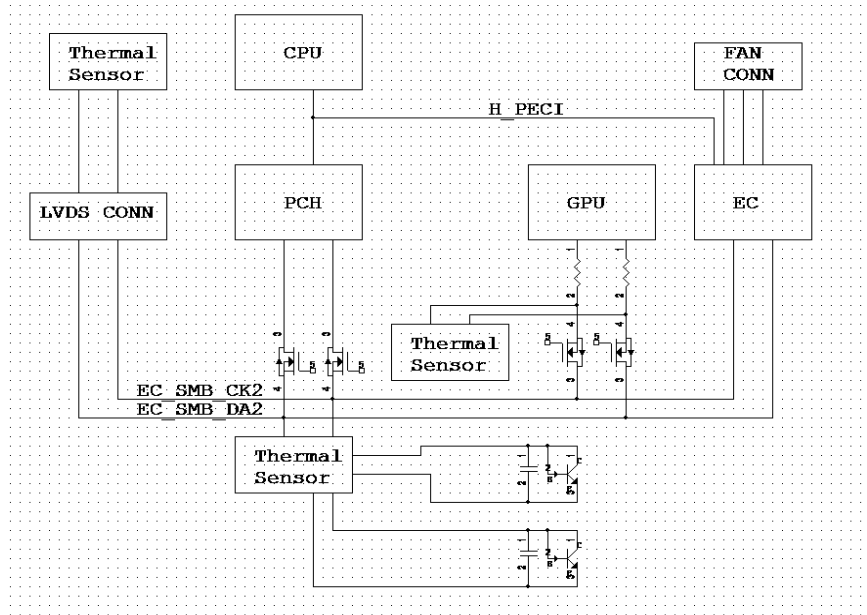
[illegible]

Device	Address	Device	Address
Smart Battery	0001_011X b	Thermal Sensor Fintek F75303M	1001_101xb

Device	Address
Thermal Sensor Fintek F75303M	1001_101xb

Device	Address
DDR DIMM0	1001 000Xb
DDR DIMM2	1001 010Xb

	SOURCE	VGA	BATT	KE9012	SODIMM	WLAN WWAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VALW	X	X	X	X	X	X	V +3VS
SMBCLK SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
SML0CLK SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VS	X	V +3VS	X	X	V +3VS	X



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# MB Bottom view

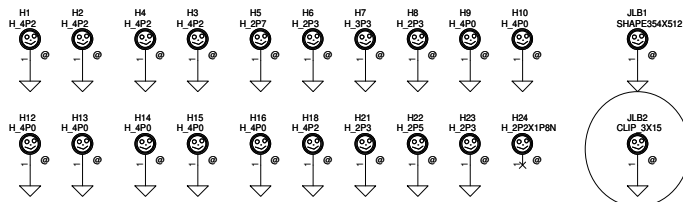


PCH

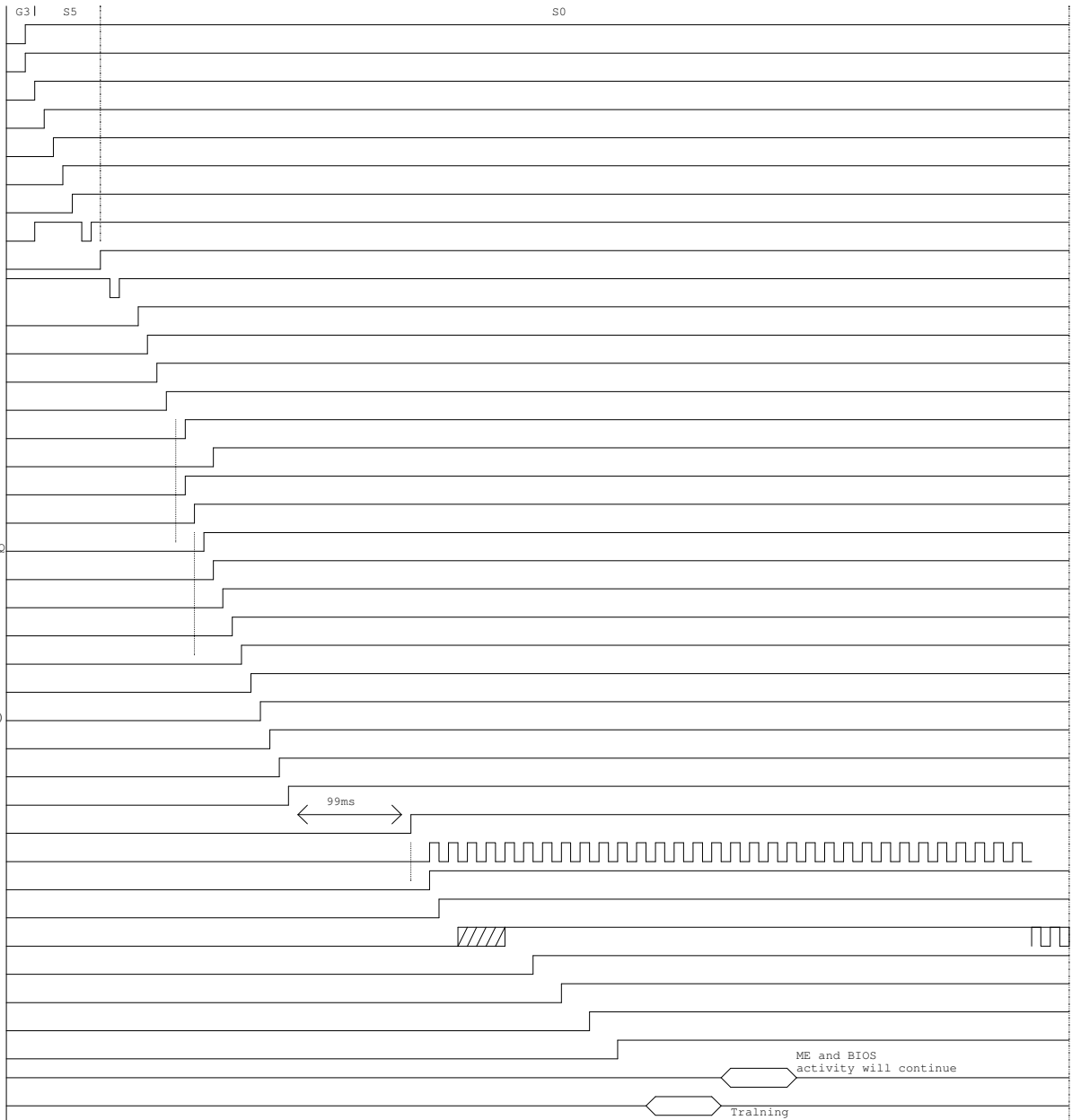
GPU

RAM

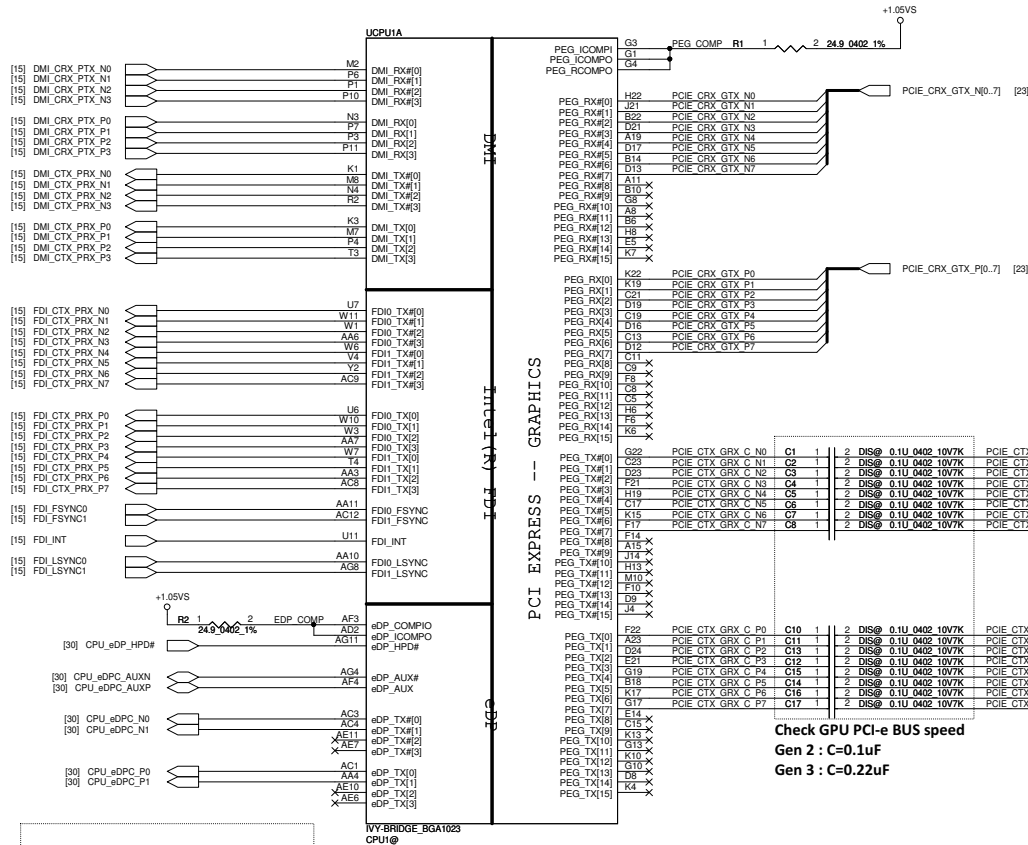
CPU



RTC  
RTCRST  
EC\_111 pin  
EC\_ON  
MAINPWON  
+5VALW  
+3VALW/VCCDSW  
ON/OFF#  
EC\_RSMRST#  
PBTN\_OUT#  
SLP\_S5#  
SLP\_S4#  
SYSON  
SYSON  
M\_PWR\_ON  
PCH\_APWROK  
SLP\_S3#  
SUSP#  
+1.5V\_CPU\_VDDQ  
+1.8VS  
+5VS  
+3VS  
+1.5VS  
+0.75VS  
+V1.05VS (VCCP)  
+VCCSA  
SA\_PGOOD  
VR\_ON  
PCH\_POK  
PCH\_CLKOUT  
DRAMPWROK  
H\_CUPFWRGD  
CPU\_VID  
CPU\_CORE  
VGATE  
SYS\_PWROK  
BUF\_PLT\_RST#  
SPI  
DMI



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PEG\_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 mohms  
PEG\_ICOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 14.5 mohms

PEG Static Lane Reversal - CFG2 is for the i6x

CFG2

★ 1: Normal Operation; Lane # definition matches socket pin map definition

0: Lane Reversed

Check GPU PCI-e BUS speed

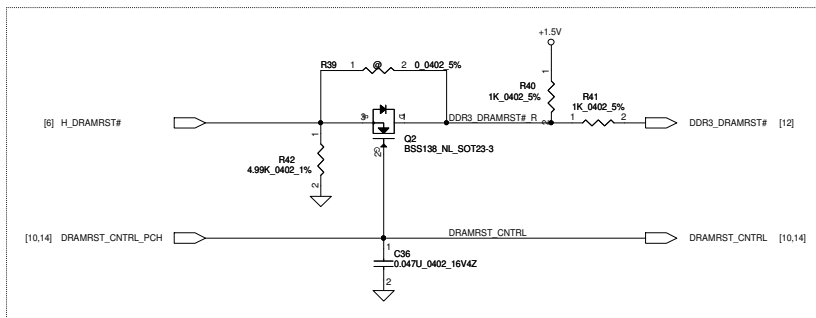
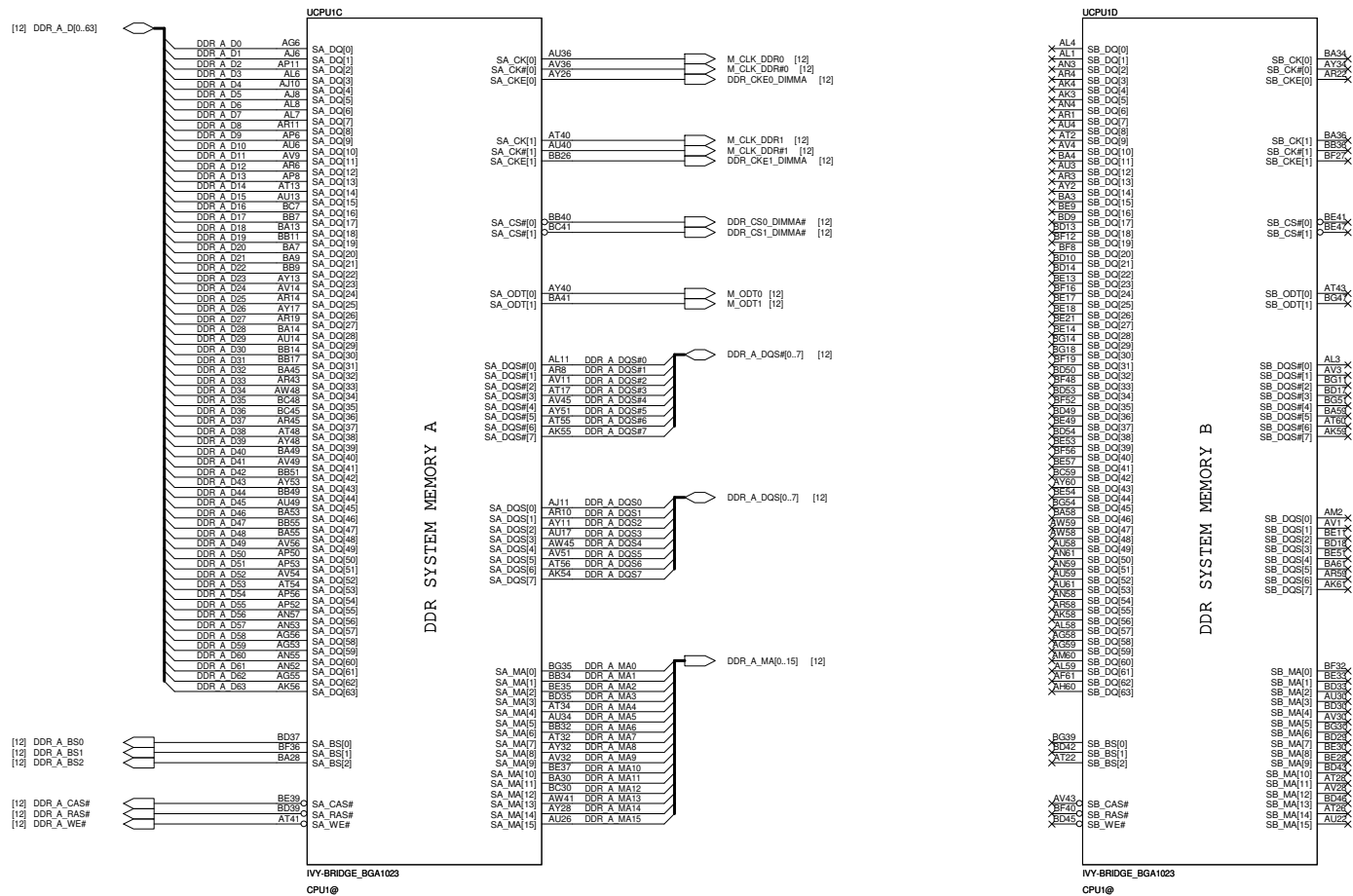
Gen 2 : C=0.1uF

Gen 3 : C=0.22uF

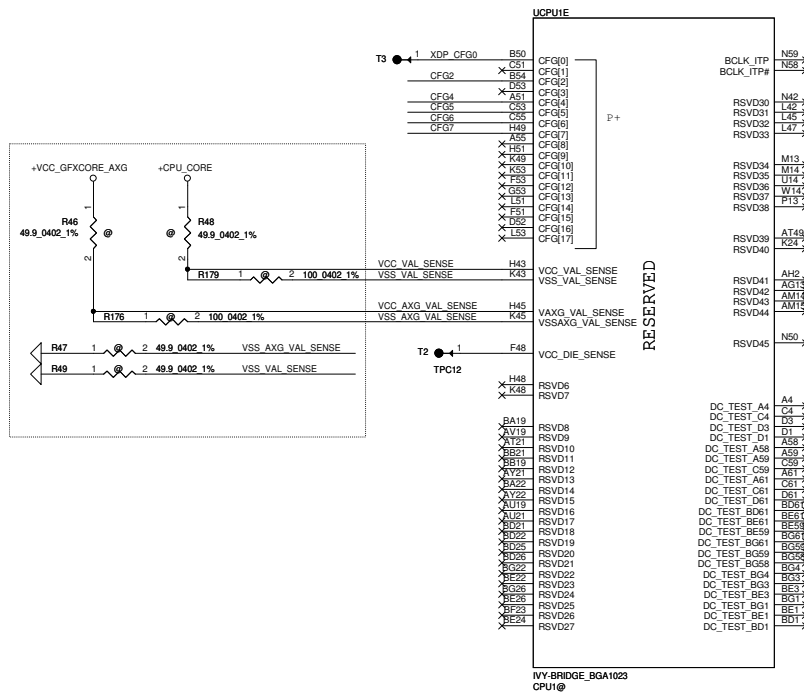
eDP\_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

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						LA-9611P		
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### CFG Straps for Processor

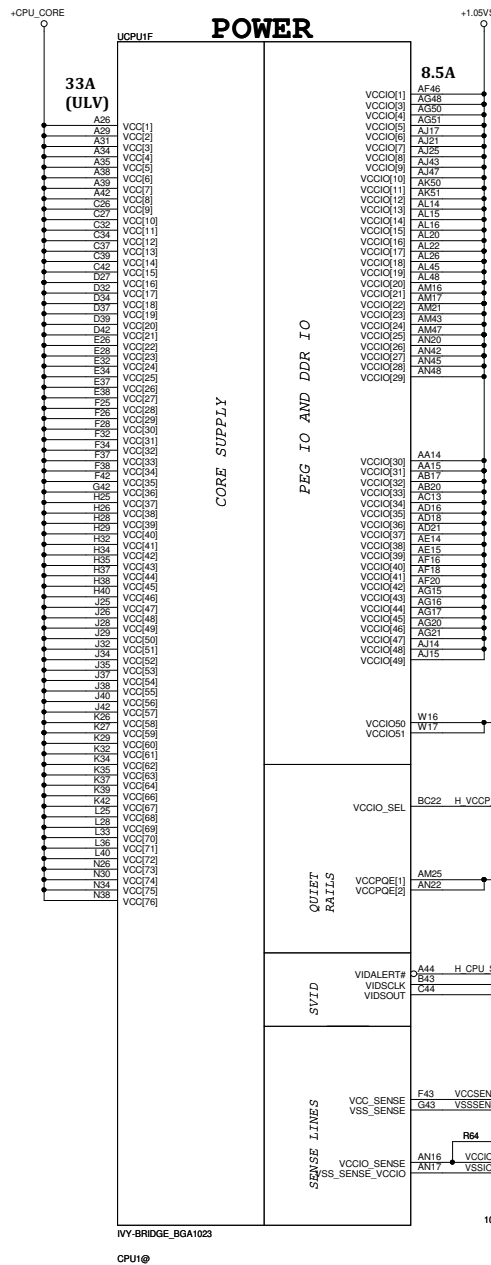
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	* 1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port * 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

PCIe Port Bifurcation Straps	
CFG[6:5]	- 00 = 1 x8, 2 x4 PCI Express* - 01 = reserved * - 10 = 2 x8 PCI Express* - 11 = 1 x16 PCI Express*

PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training





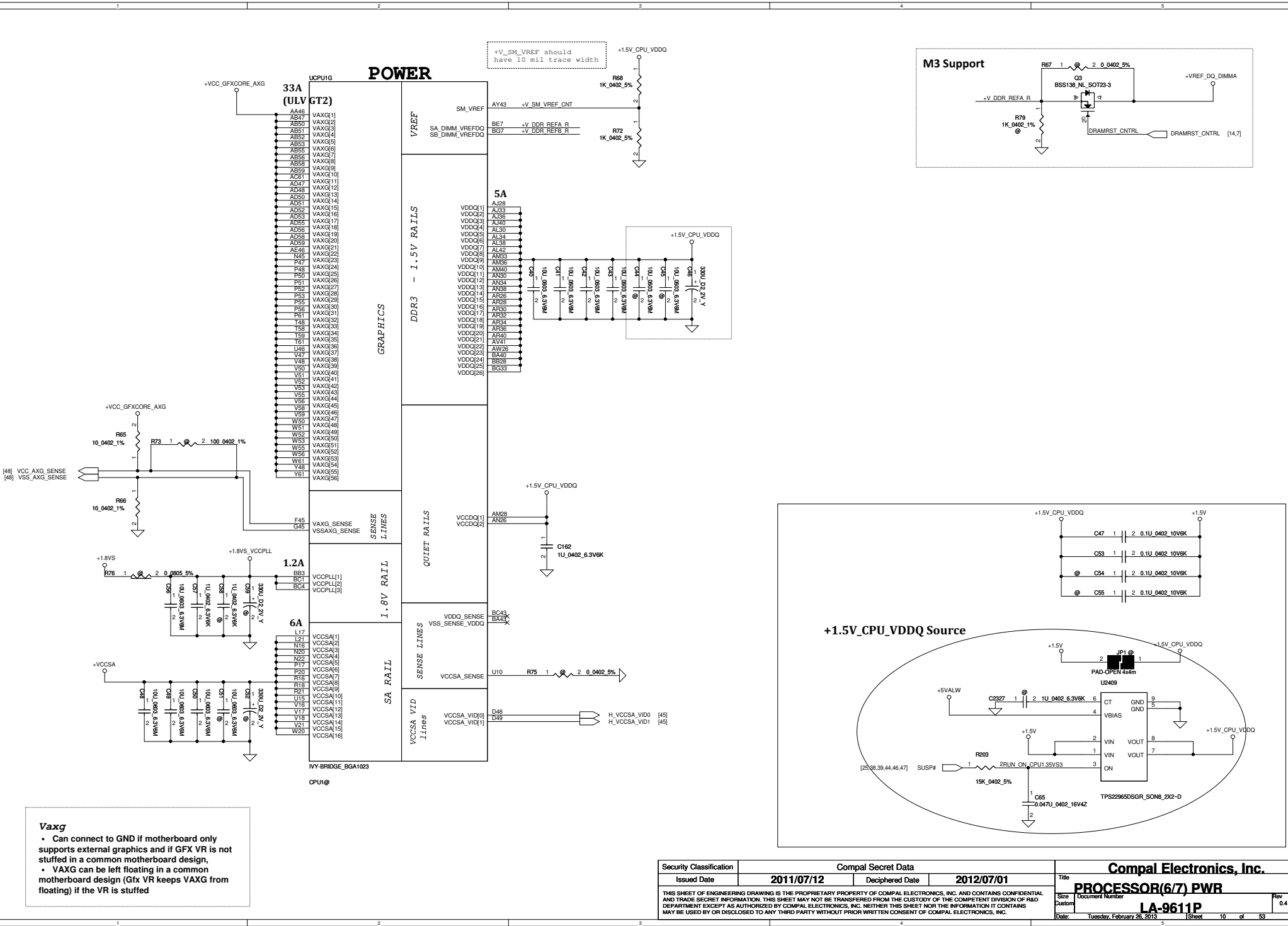
Chief-River platforms  
VCCIO\_SEL = pulled high

Place the PU  
resistors close to VR

Trace Impedance = 27 ~ 33 ohm  
Trace Length Match < 25 mils

Place the PU  
resistors close to CPU

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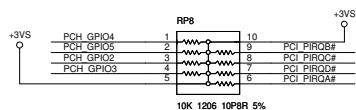








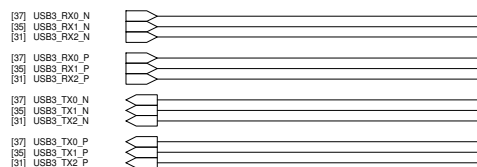
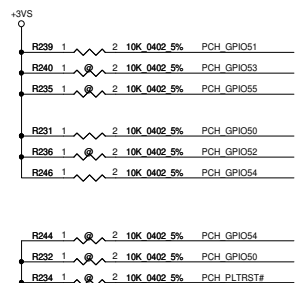




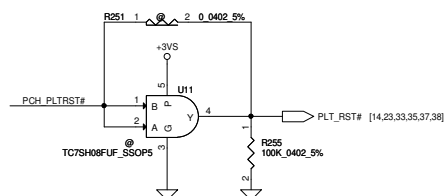
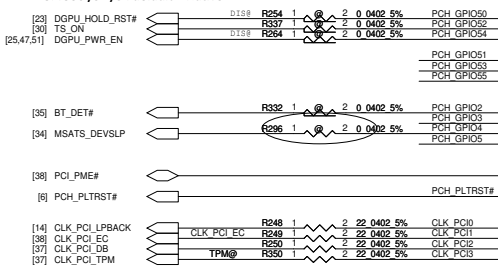
GNT0#, GNT1#/GPIO51, GNT2#/GPIO53, GNT3#/GPIO55  
PCI Grants: The PCH supports up to 4 masters on the PCI bus.

GNT[3:1]# pins can instead be used as GPIO.  
Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3\_3 power rail.

NOTES:  
1. GNT[3:1]#/GPIO[55,53,51] are sampled as a functional strap. See Section 2.27 for details.



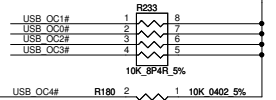
GPIO50 /52 /54 default = Native



USB 3.0 (I/O Board)  
USB 3.0 (MB)  
USB 3.0 (Docking)  
CMOS Camera (LVDS)

Touch panel  
(Test Point for BIOS Debug)  
Mini Card(WLAN/BT)  
FingerPrint

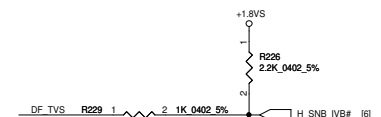
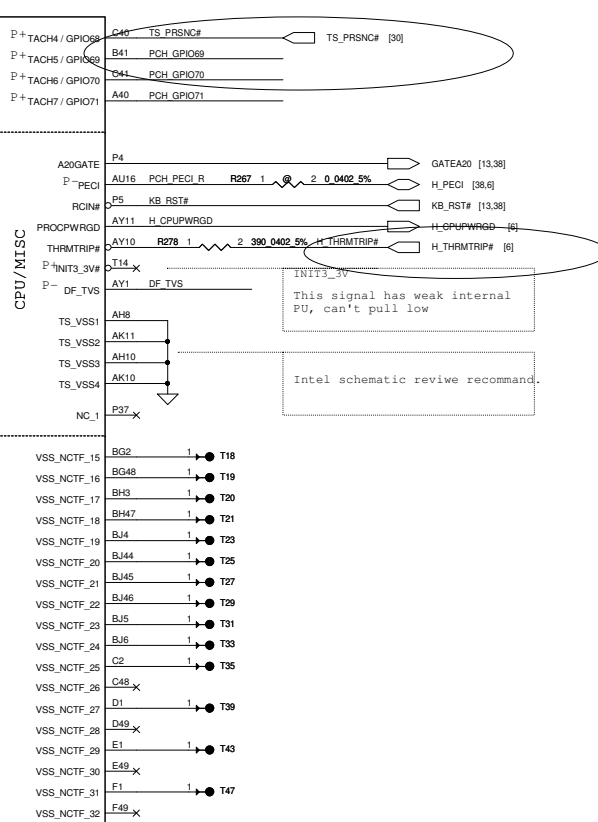
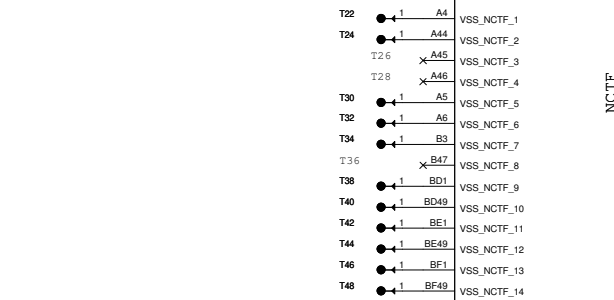
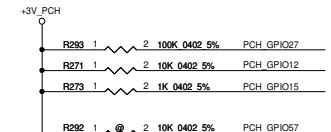
OC[0..3] use for EHCI 1  
OC[4..7] use for EHCI 2



Boot BIOS Strap bit1 BBS1		
GPIO51 GPIO19	Boot BIOS	Destination
Bit11 Bit10		
0 1		Reserved
1 0		PCI
1 1	*	SPI (Default)
0 0		LPC

A16 swap override Strap/Top-Block Swap Override jumper	
Low=A16 swap override/Top-Block Swap Override enabled	
High=Default *	

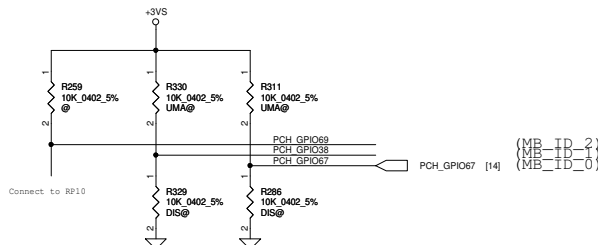
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PCH (5/9) PCI, USB, NVRAM				LA-9611P	
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DMI Termination Voltage	
NV_CLE	Set to Vcc when HIGH
	Set to Vss when LOW

CLOSE TO THE BRANCHING POINT

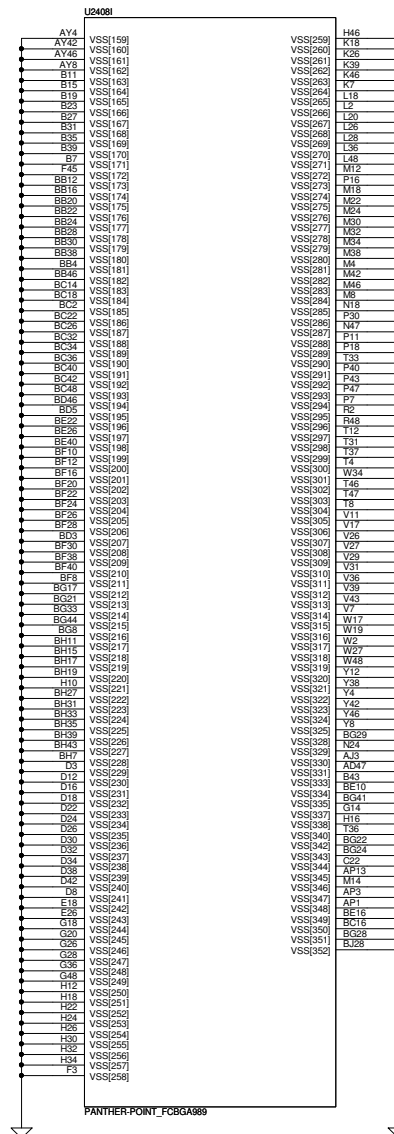
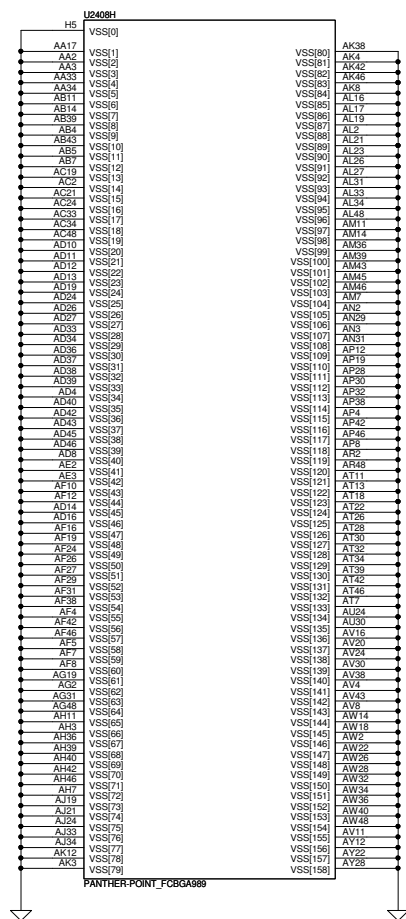
PCH_GPIO69	PCH_GPIO38	PCH_GPIO67	Function
0	0	0	Optimus
0	0	1	Reserved
0	1	0	DIS
0	1	1	UMA



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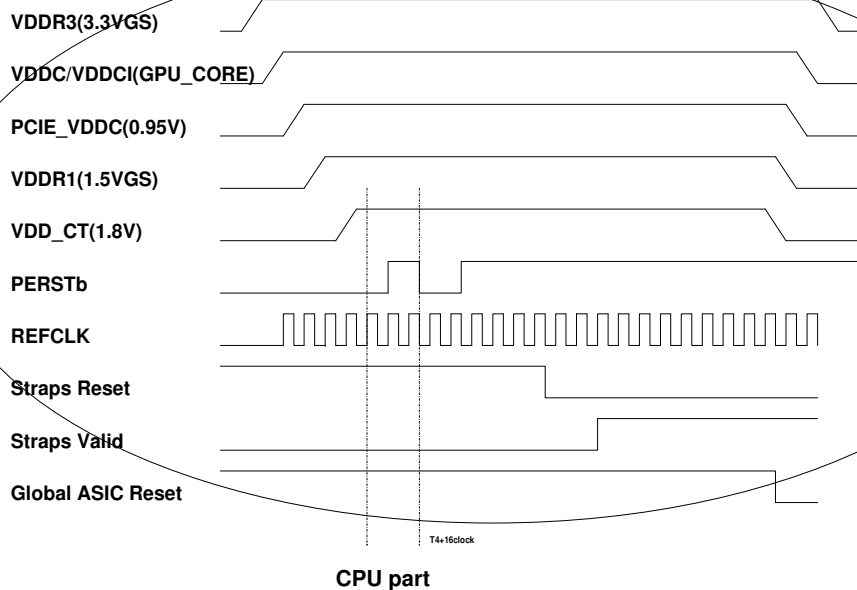




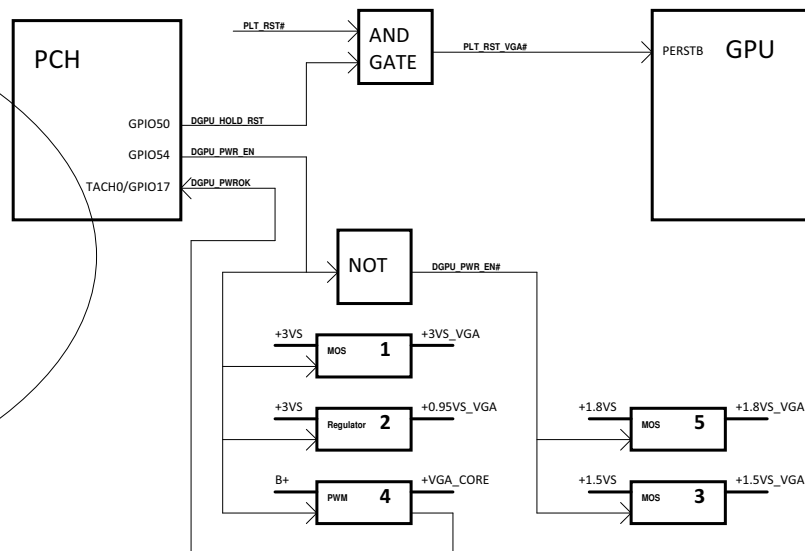
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## Power-Up/Down Sequence

1. All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/ $\mu$ s.
2. The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD\_CT have ramped up.
3. VDDC and VDD\_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD\_CT starts to ramp up (or vice versa).
4. For power down, reversing the ramp-up sequence is recommended.



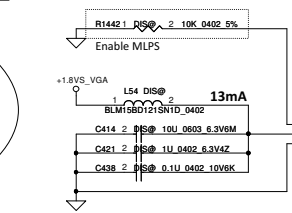
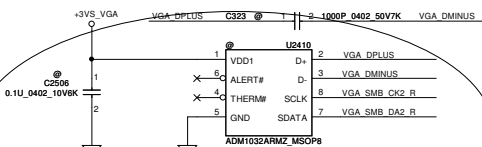
CPU part



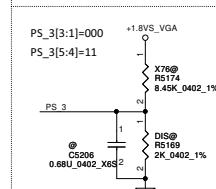
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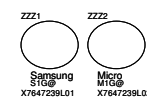


Cap (nF) C5206	Bitd [5:4]	Compal PN
680nF	00	SE00000YJ80
82nF	01	SE076823K80
10nF	10	SE074103KN
NC	11	



Memory ID	Memory Type	Configuration	Size
1	gDDR3-2133	Samsung K4W2G1646E-BC1A	2Gb X4 (256GBX4)
	SA000068U00 - 5 IC D3 128MX16 K4W2G1646E-BC1A FBGA 96P		
2	gDDR3-2000	Micro MT41J128M16JT-093G	2Gb X4 (256GBX4)
	SA000067500 - 5 IC D3 128M16 MT41J128M16JT-093G;K FBGA		

```
EX:
PS_3=11001 (PU=NC, PD=4.75K, C=NC) for Samsung 1GB
PS_3=11010 (PU=8.45K ,PD=2K, C=NC) for Micro 1GB
```



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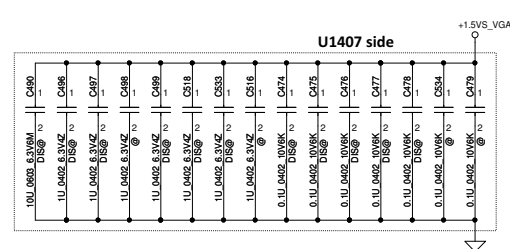
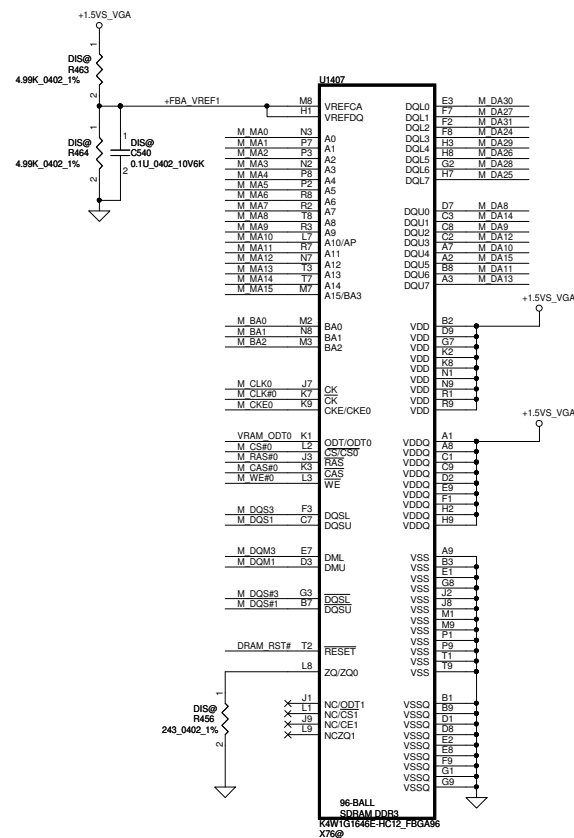
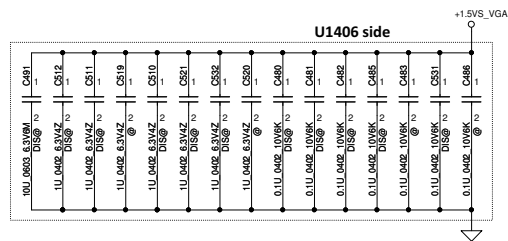
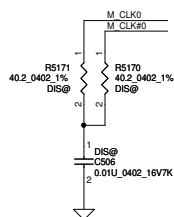
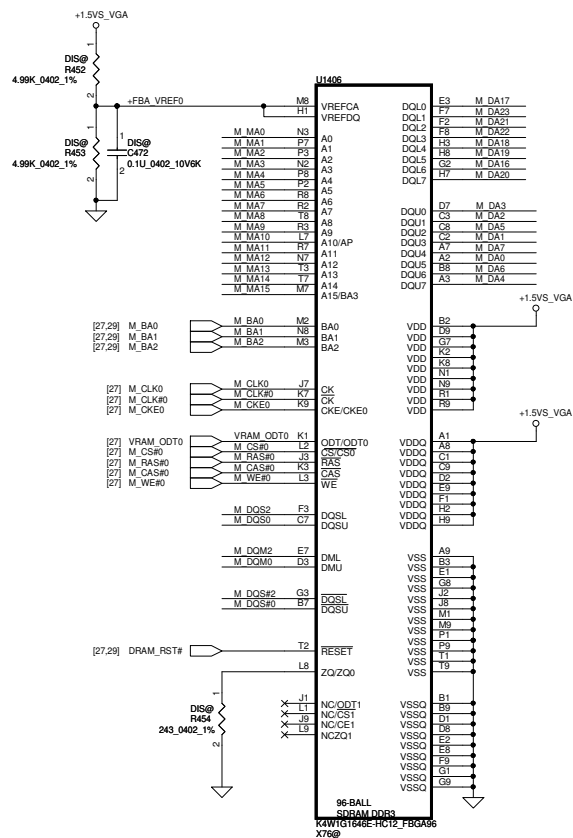






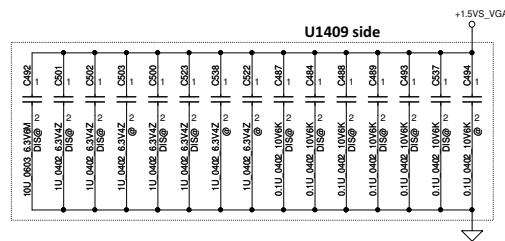
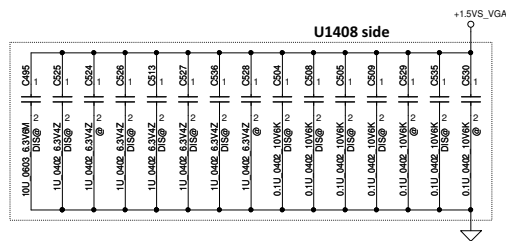


[27..29]	M_DA[63..0]	◀	M_DA[63..0]
[27..29]	M_MA[15..0]	◀	M_MA[15..0]
[27..29]	M_DQM[7..0]	◀	M_DQM[7..0]
[27..29]	M_DQS[7..0]	◀	M_DQS[7..0]
[27..29]	M_DQS#[7..0]	◀	M_DQS#[7..0]

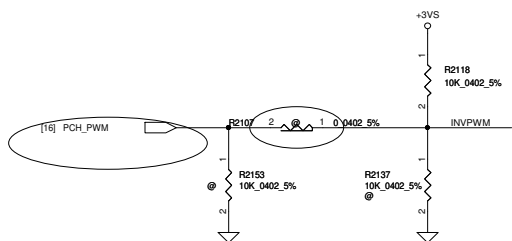
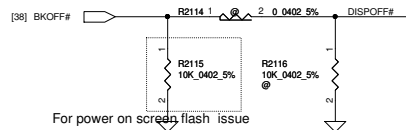


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				Customer	LA-9611P
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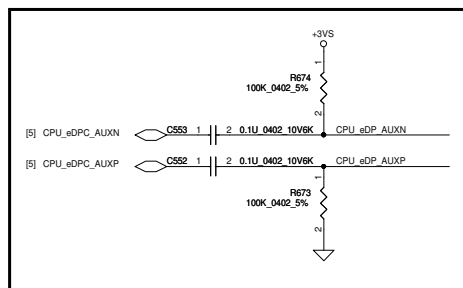
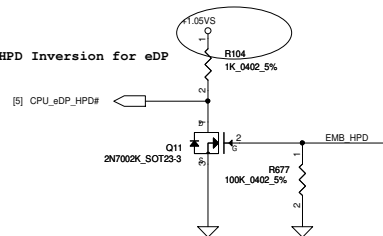
**WWW.AliSaler.Com**



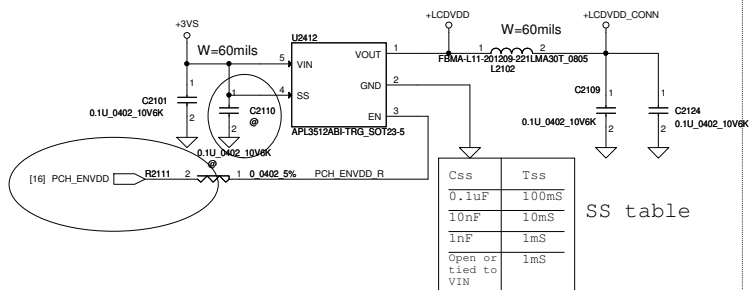
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	MARS VRAM A Upper	
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				LA-9611P		
Date: Tuesday, February 26, 2013				Sheet	29 of 53	



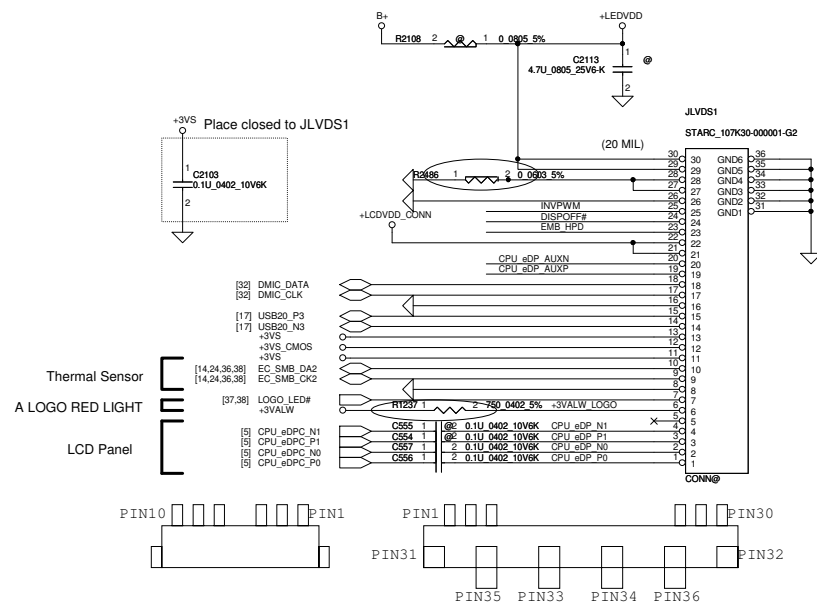
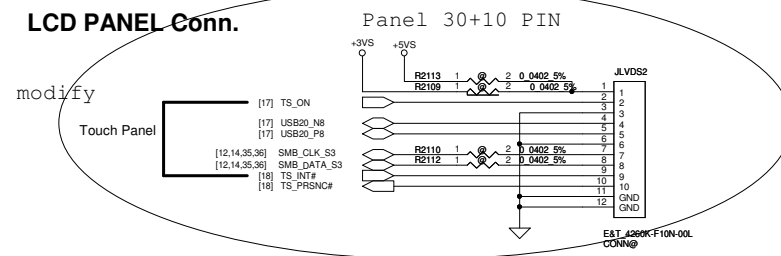
#### HPD Inversion for eDP



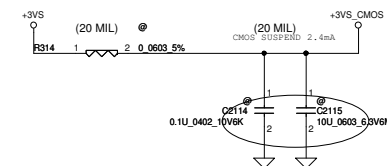
#### LCD POWER CIRCUIT



#### LCD PANEL Conn.

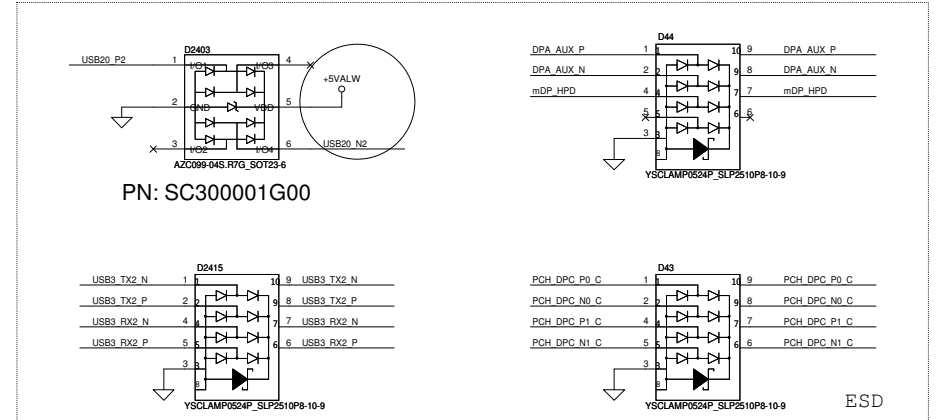
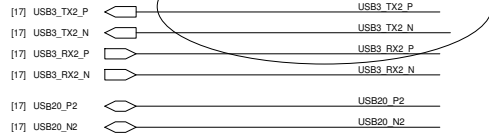


#### CMOS Camera Conn

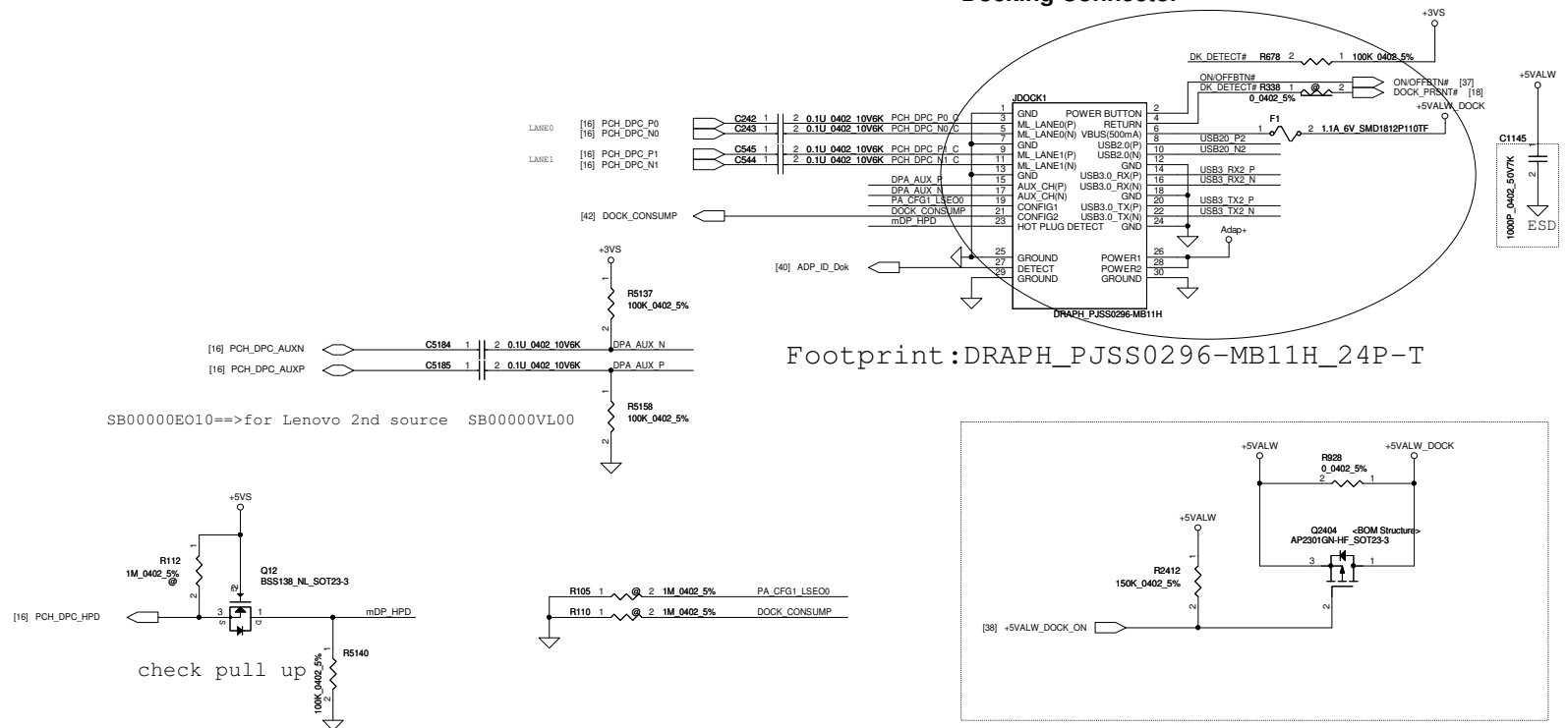


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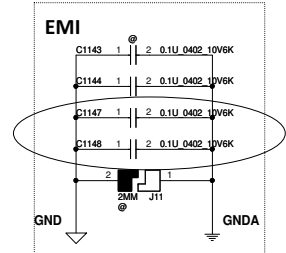
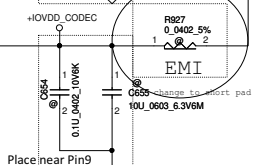
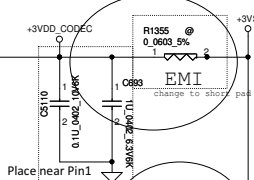
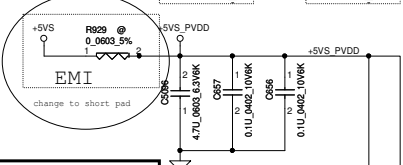
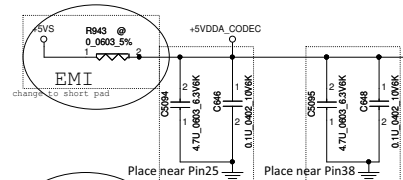
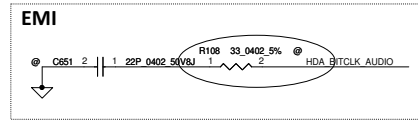
## Docking (USB3.0)



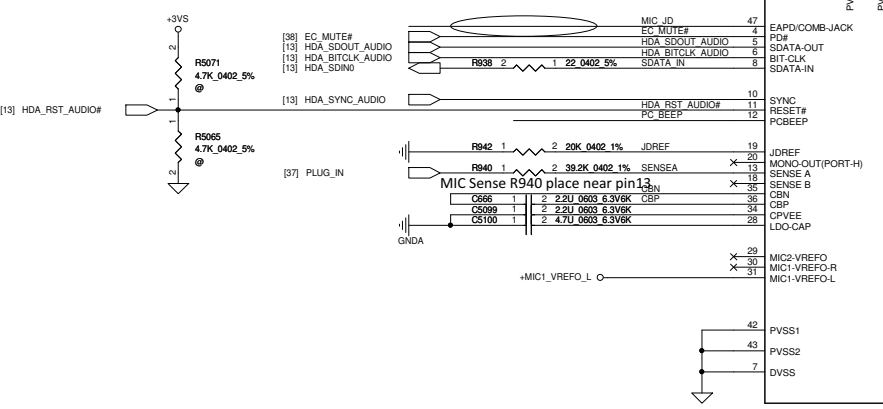
## Docking (Display Port)



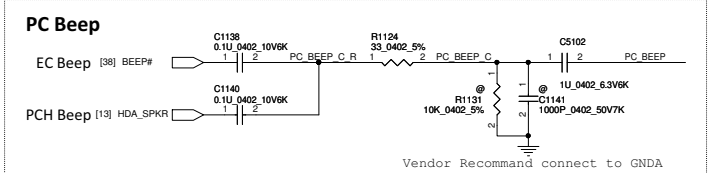
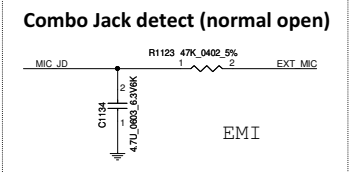
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Issued Date	2011/07/12	Deciphered Date	2012/07/01		Doc	0.4
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Compal Electronics, Inc.						
Docking						
LA-9611P						
Date: Tuesday, February 26, 2013						
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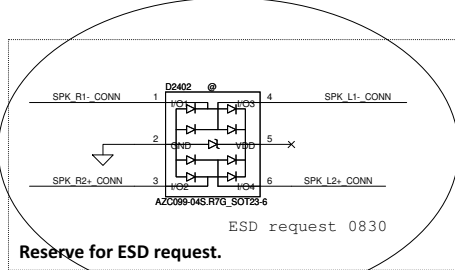
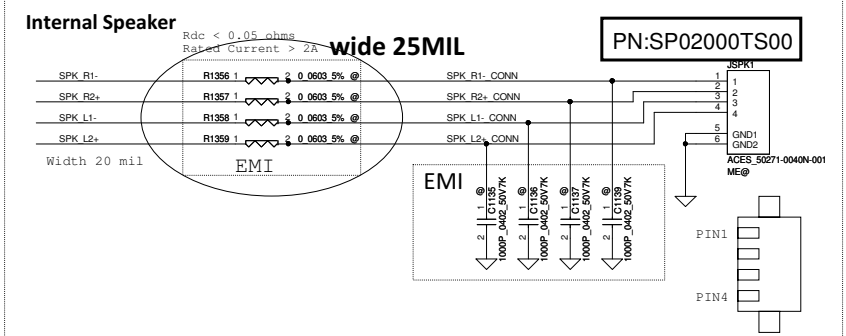
Power down (PD#) power stage for save power  
0V: Power down power stage  
3.3V: Power up power stage



Pin Assignment	Location	Function
SPK-OUT (Pin40/41/44/45)	Internal	Int Speaker
Capless HP-OUT (Pin32/33)	External	Headphone out
MIC1 (Pin21/22)	External	Mic in

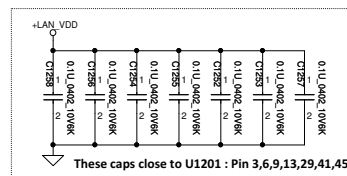


ALC3202 VC3  
SA000058310



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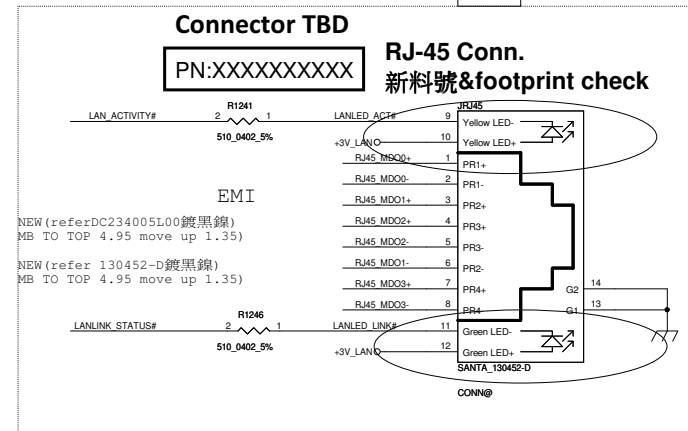
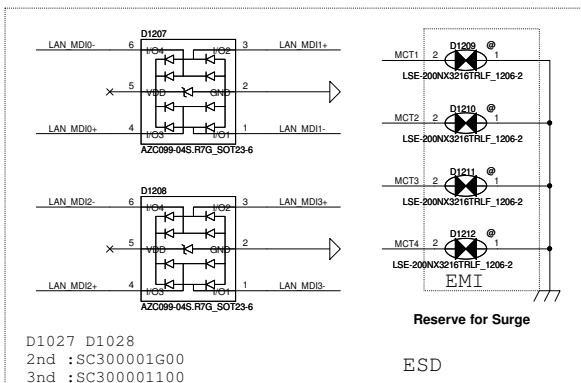
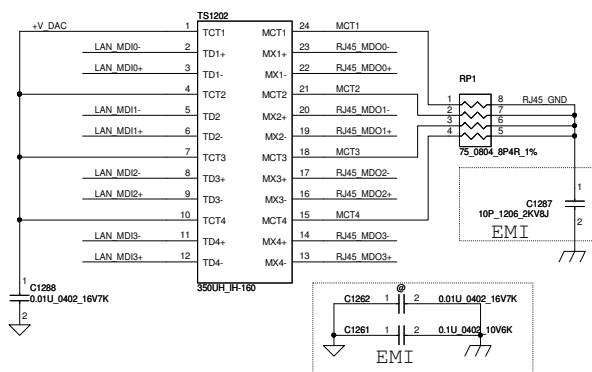
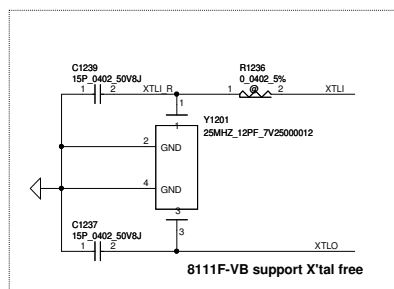
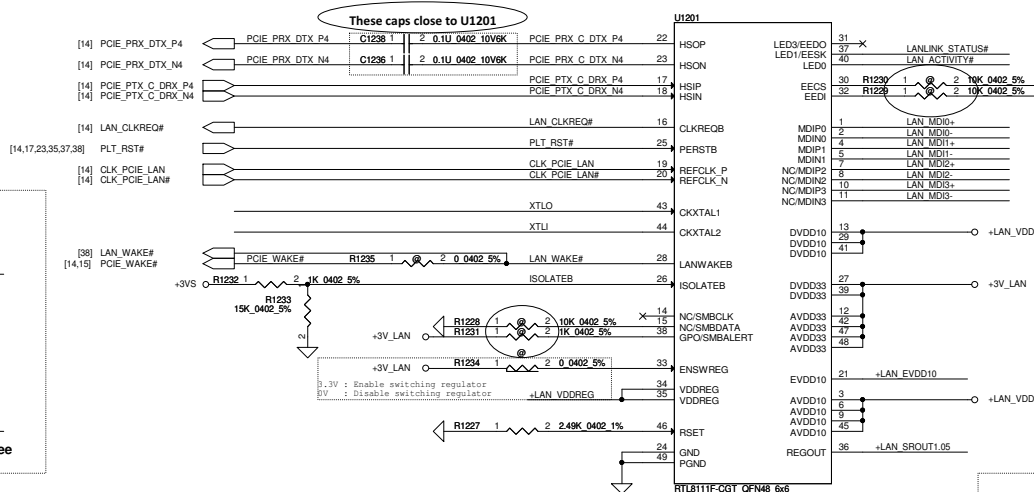
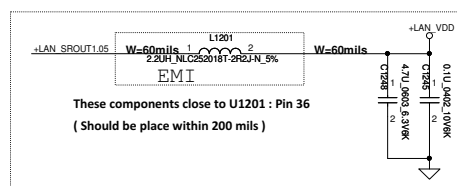
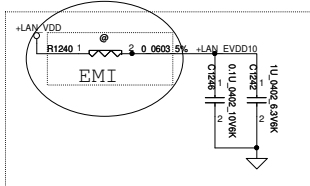
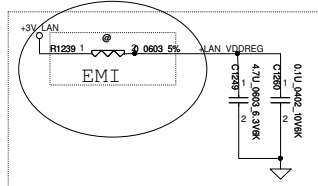
+3V LAN Rising time (10%~90%) >1mS and <100mS

+3V LAN

W=60mils

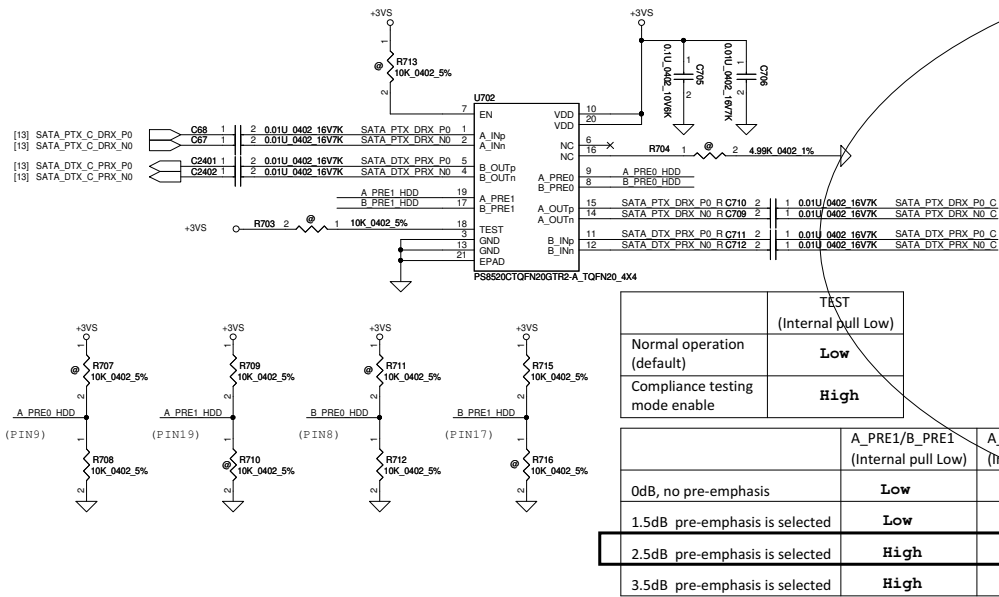
J1203 @ JUMP\_43X39

370mA

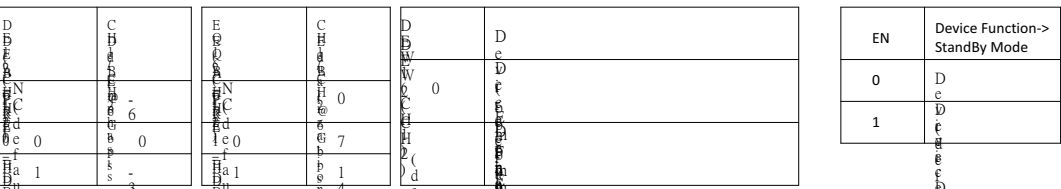
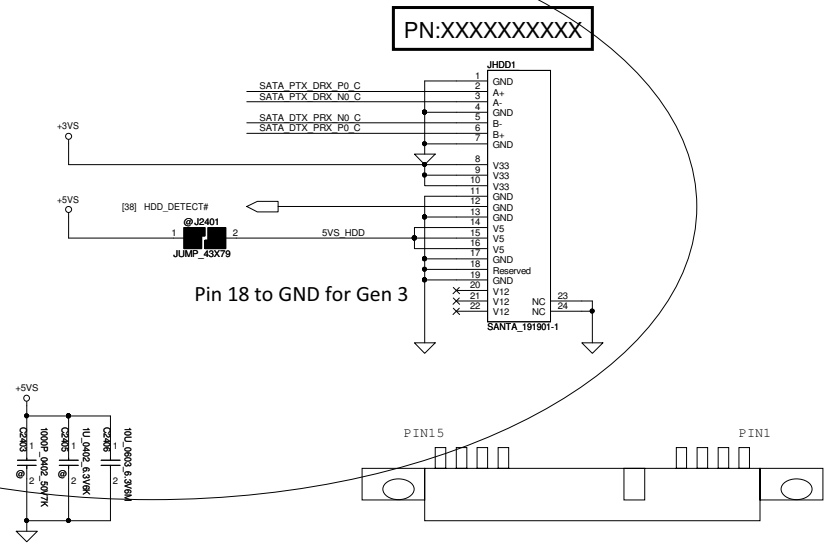


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Date				Wednesday, February 27, 2013	Sheet	33 of 63

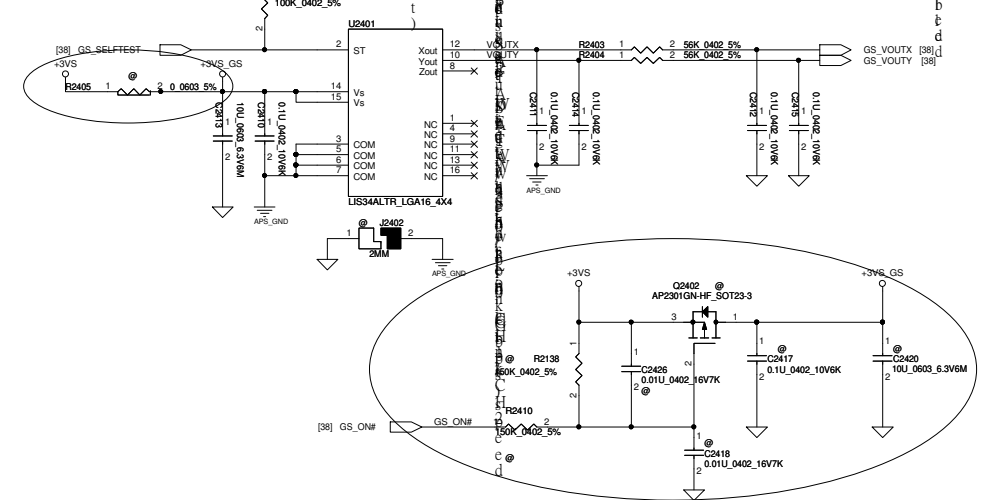
SATA HDD BTB CONN.



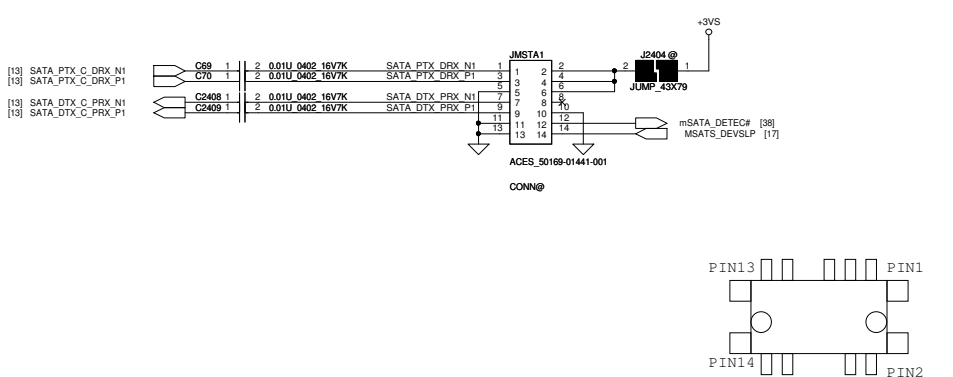
SATA HDD CONN.



APS G-Sensor

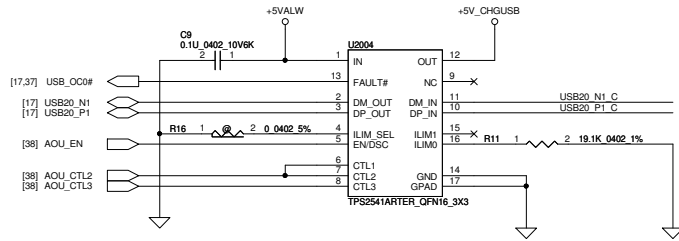


mSATA CONN.

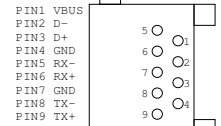
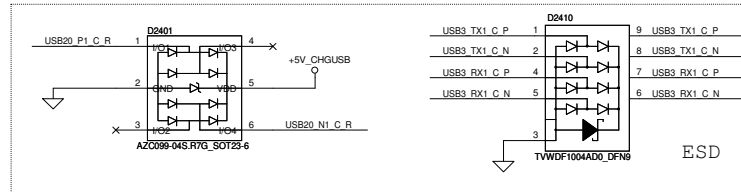
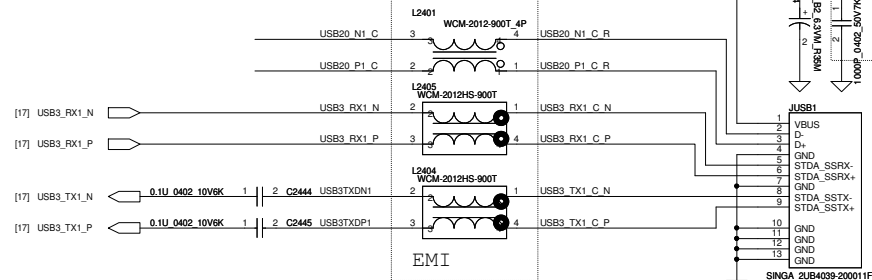


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## USB 3.0 Charger & Conn.

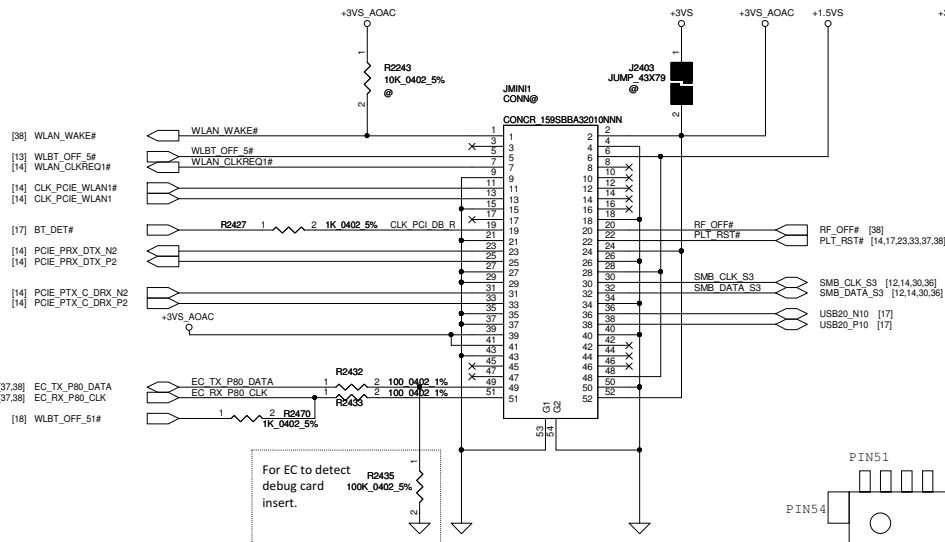


Superworld's common mode choke(SM070001V00) has quality issue for USB 3.0



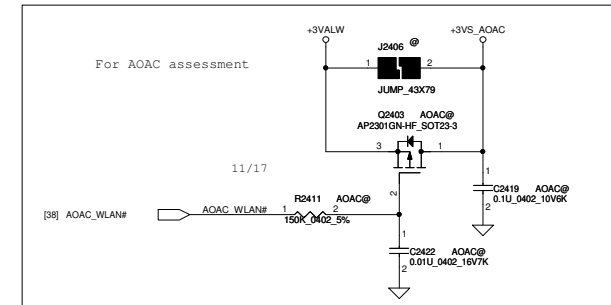
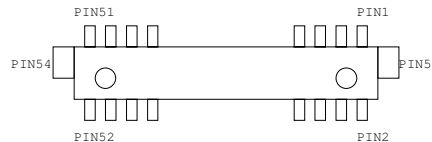
## Mini-Express Card for WLAN/WiMAX(Half)

### Mini-Express Card(WLAN/WiMAX)



For EC to detect debug card insert.

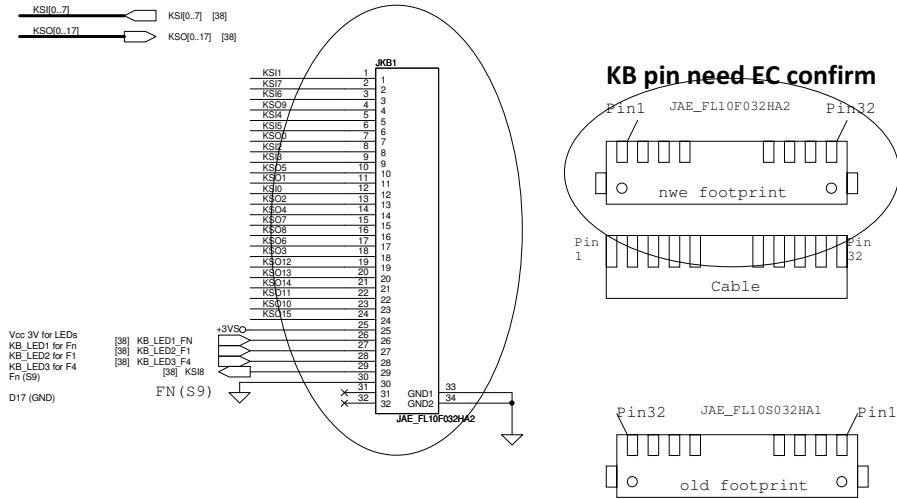
NEW(apply compal PN)  
159SBA32010NNN



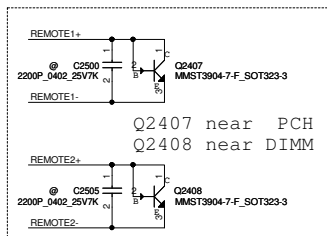
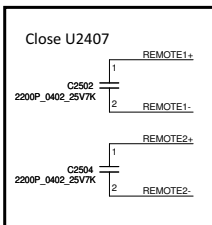
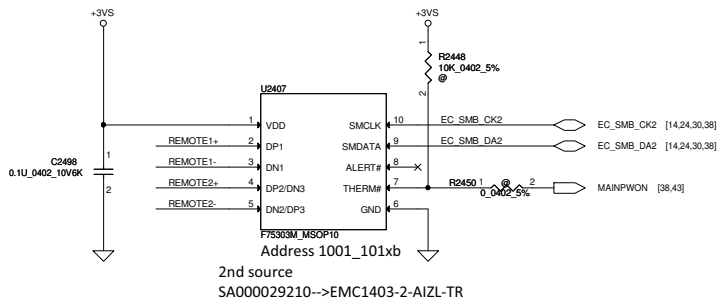
Need check WLAN/BT module OFF pin

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## INT\_KBD Conn.

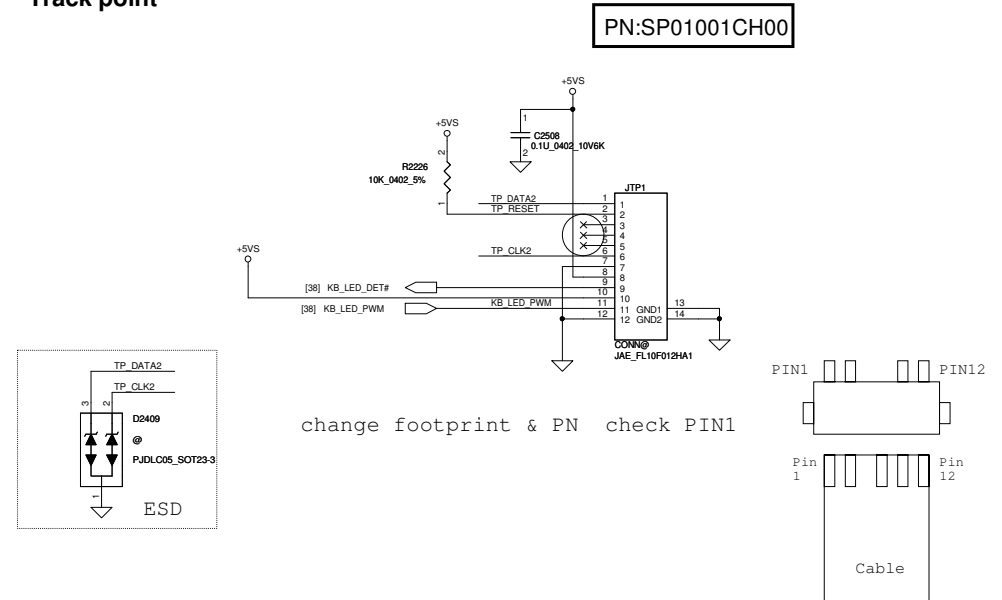


## Fintek thermal sensor placed near CPU Core

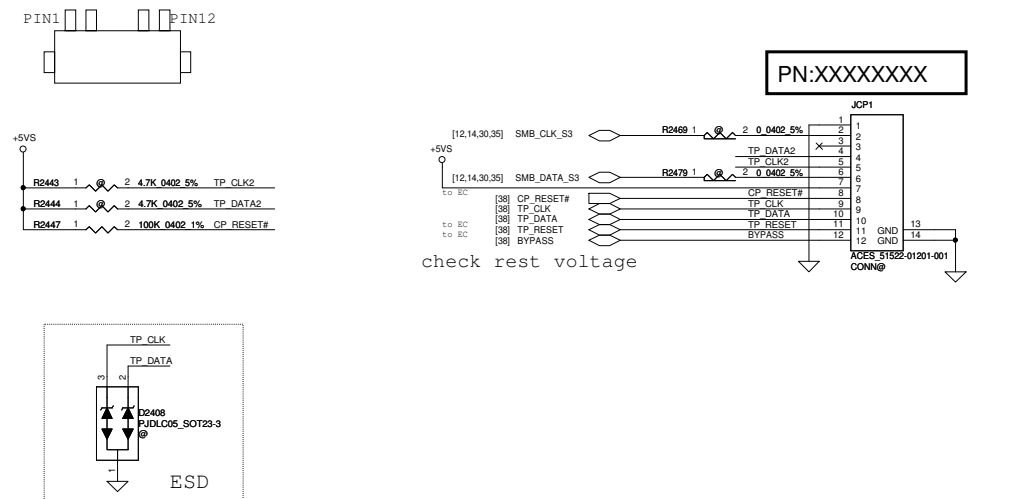


REMOTE1,2 (+/-):  
Trace width/space:10/10 mil  
Trace length:<8"

## Track point

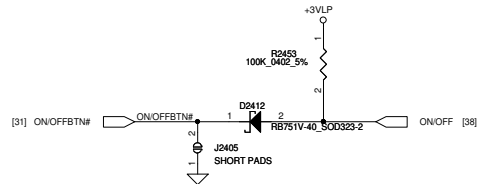


## Click pad

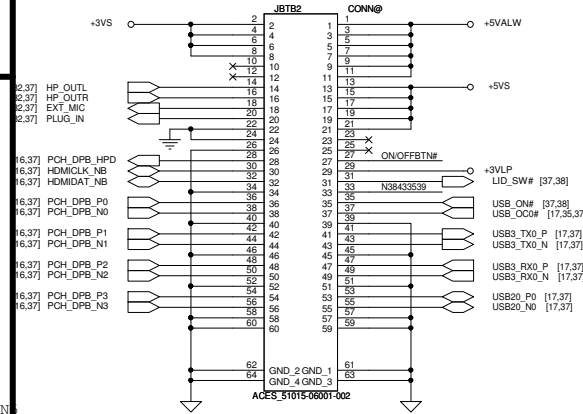


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				Rev	0.4
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## Power Button



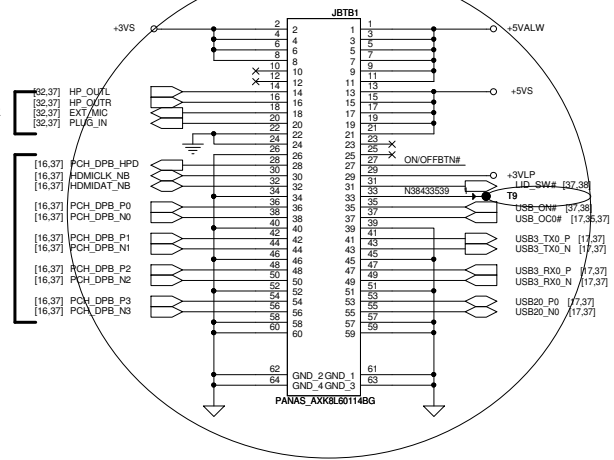
## I/O Board CONN.



Audio combo Jack

HDMI

Connector: 0.3A / pin



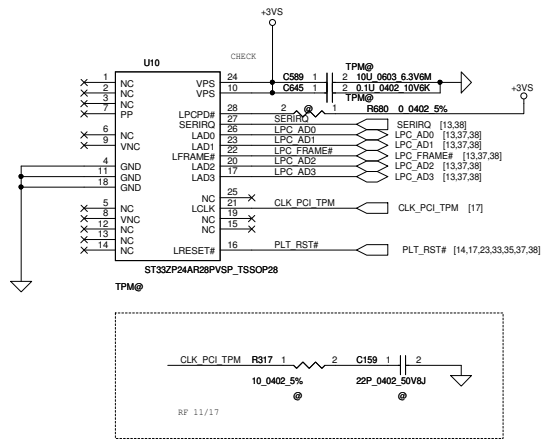
Power Button  
Lid Switch & LED

to EC

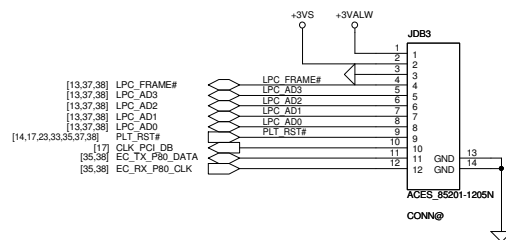
USB3.0

ESD request 0827

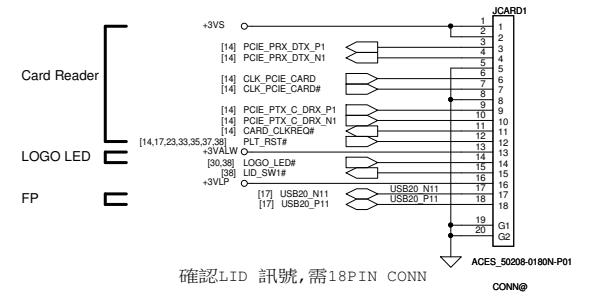
## TPM



## Debug Conn.



## Card Reader CONN.



確認LID 訊號, 需18PIN CONN

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Can't internal pull up

GPIO44  
GPIO45  
GPIO46  
GPIO47  
GPIO4A  
GPIO4B  
GPIO4E  
GPIO4F  
GPIO50  
GPIO5B

RF EMI

R2225 1 2 47K 0402 5% KSO1  
R2227 1 2 47K 0402 5% KSO2  
R2231 1 2 2.2K 0402 5% EC SMB CK1  
R2232 1 2 2.2K 0402 5% EC SMB DA1

R2454 1 2 10K 0402 5% KS18  
R2228 1 2 2.2K 0402 5% EC SMB CK1  
R2230 1 2 2.2K 0402 5% EC SMB DA1

R2452 1 2 10K 0402 5% EC FAN PWM  
R2451 1 2 10K 0402 5% EC TACH  
R2236 1 2 2.2K 0402 5% EC SMB CK2  
R2237 1 2 2.2K 0402 5% EC SMB DA2  
C2220 @ 1 2 100P 0402 50V/J EC SMB CK2  
C2221 @ 1 2 100P 0402 50V/J EC SMB DA2  
R2239 1 2 10K 0402 5% PCH PWROK

EC RTCK1  
R2229 1 2 10M 0402 5% SUSCLK R  
Y2202  
32768KHZ\_12SPF\_CM3153780ZFT  
C2218 1P 0402 50V/J  
C2219 1P 0402 50V/J

**BOTTOM SIDE**  
SN111005800  
by ME drawing  
[43] PWR\_RESET PWR\_RESET  
SW4  
SKRBAAE010\_4P  
GND

SD034120280 S RES 1/16W 12K +-1% 0402  
SD034150280 S RES 1/16W 15K +-1% 0402  
SD034200280 S RES 1/16W 20K +-1% 0402  
SD034270280 S RES 1/16W 27K +-1% 0402  
SD034330280 S RES 1/16W 33K +-1% 0402

EC 要求須改為1%

Vcc	3.3V +/- 5%				
R2210	100K +/- 1%				
Board ID	R2213	V <sub>AD_BID</sub> min	V <sub>AD_BID</sub> typ	V <sub>AD_BID</sub> max	Phase
0	0K +/- 5%	0 V	0 V	0 V	SDV
1	12K +/- 5%	0.347 V	0.354 V	0.360 V	FVT
2	15K +/- 5%	0.423 V	0.430 V	0.438 V	SIT
3	20K +/- 5%	0.541 V	0.550 V	0.559 V	SVT
4	27K +/- 5%	0.691 V	0.702 V	0.713 V	
5	33K +/- 5%	0.807 V	0.819 V	0.831 V	

LCD for thermal  
LID SW# R2203 1 2 100K 0402 5%  
LID SW# R2208 1 2 100K 0402 5%  
Turbo V R2218 1 2 10K 0402 5%  
NTC V R2219 1 2 10K 0402 5%  
BATT\_TEMP R2240 1 2 10K 0402 5%  
Turbo V R2217 1 2 47K 0402 5%  
NTC V R2206 1 2 10K 0402 5%  
ADP\_65W R2207 1 2 10K 0402 5%  
ADP\_90W R2214 1 2 10K 0402 5%  
EC\_MUTE# R2202 1 2 10K 0402 5%  
HDD\_DETECT# R2204 1 2 100K 0402 5%  
mSATA\_DETECT# R2242 1 2 10K 0402 5%  
HDD\_DETECT# R2246 1 2 100K 0402 5%  
mSATA\_DETECT# R2244 1 2 10K 0402 5%  
USB\_ON# R2209 1 2 10K 0402 5%  
TP\_CLK R2211 1 2 4.7K 0402 5%  
TP\_DATA R2212 1 2 4.7K 0402 5%  
TP\_CLK R2216 1 2 4.7K 0402 5%  
TP\_DATA R2241 1 2 4.7K 0402 5%

for 5 button

add resistor

KB\_LED1 R2234 2 1 100 0402 1%  
KB\_LED2 R2235 2 1 150 0402 1%  
KB\_LED3 R2238 2 1 100 0402 1%

EC\_PME#  
LAN\_WAKE# [33]  
EC\_PME#  
PC1\_PME# [17]  
2N7002K\_SOT23-3

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	2012/07/01	
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[illegible][illegible]

### +3VALW TO +3VALW(PCH AUX Power)

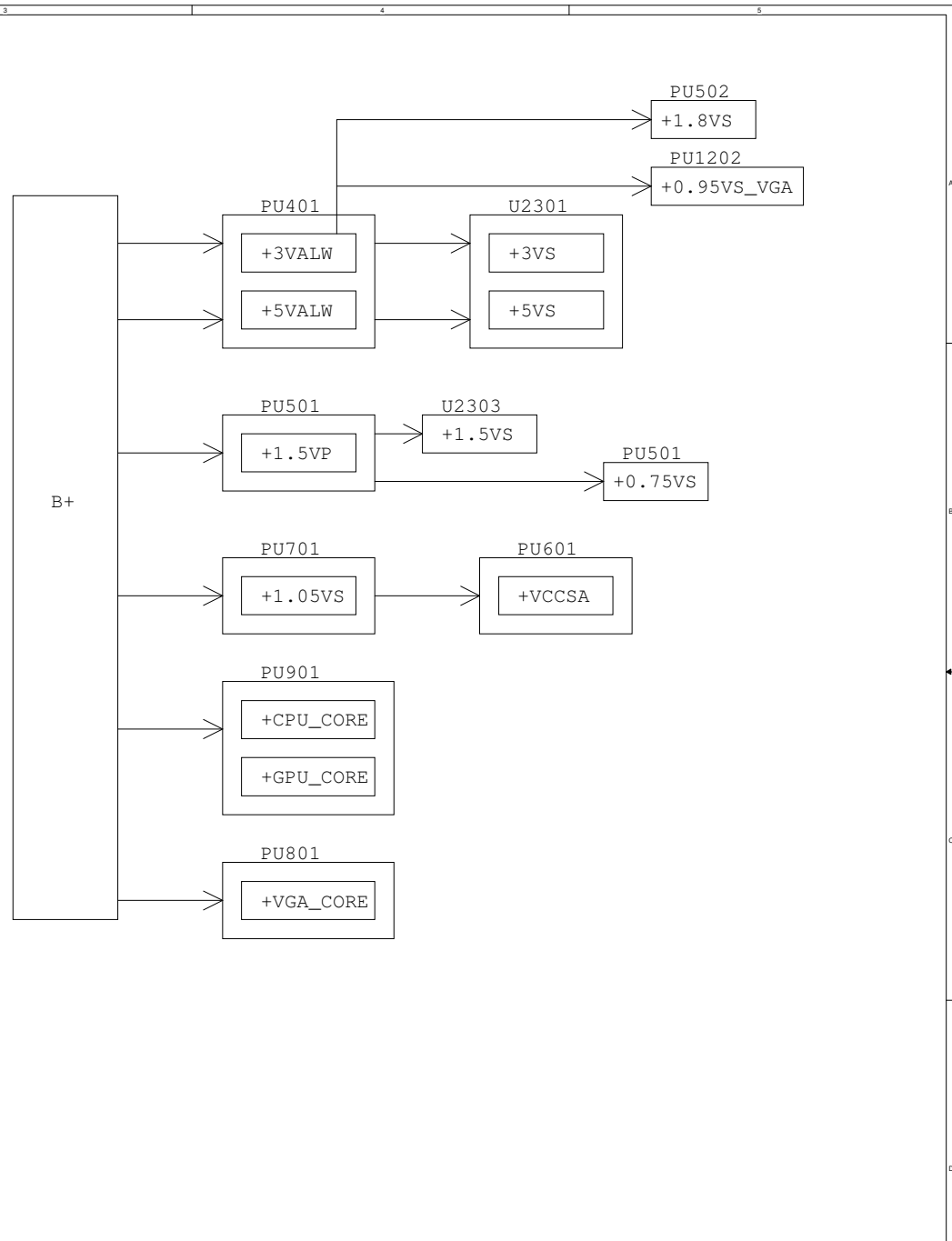
Short J2301 for PCH VCCSUS3.3

### For Intel S3 Power Reduction

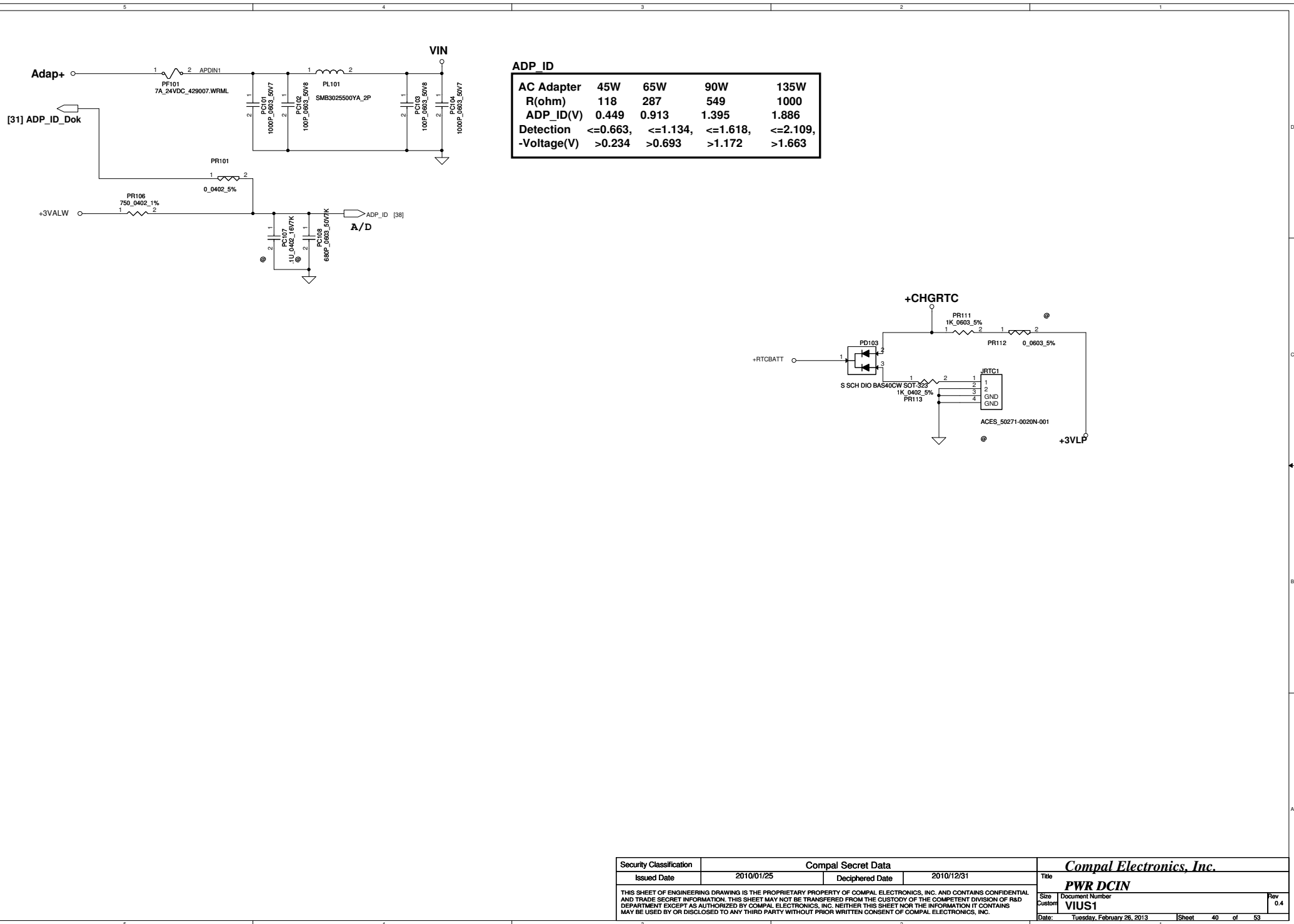
The diagrams show the following components and connections:

- Diagram 1 (+0.75VS):** Resistor R2314 (22\_0603\_5%) connected to MOSFET Q2307 (2N7002K\_SOT23-3).
- Diagram 2 (+1.05VS):** Resistor R2315 (470\_0603\_5%) connected to MOSFET Q2308 (2N7002K\_SOT23-3).
- Diagram 3 (+1.8VS):** Resistor R2316 (470\_0603\_5%) connected to MOSFET Q2309 (2N7002K\_SOT23-3).
- Diagram 4 (-5VS):** Resistor R2317 (470\_0603\_5%) connected to MOSFET Q2310 (2N7002K\_SOT23-3).
- Diagram 5 (-3VS):** Resistor R2319 (470\_0603\_5%) connected to MOSFET Q2312 (2N7002K\_SOT23-3).

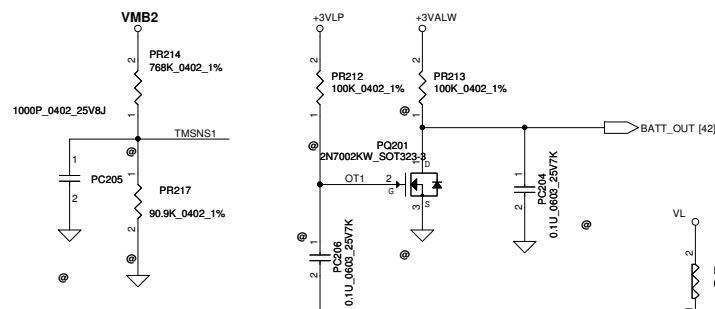
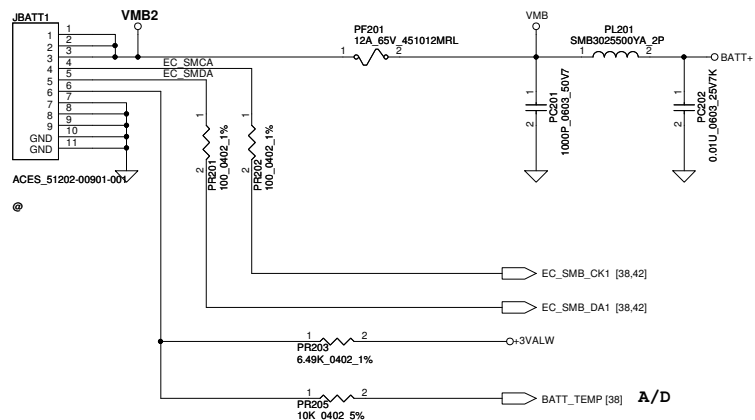
The MOSFETs are labeled with '2 SUSP' and 'Q2307' through 'Q2312'. The transistors are labeled with '2N7002K\_SOT23-3'.



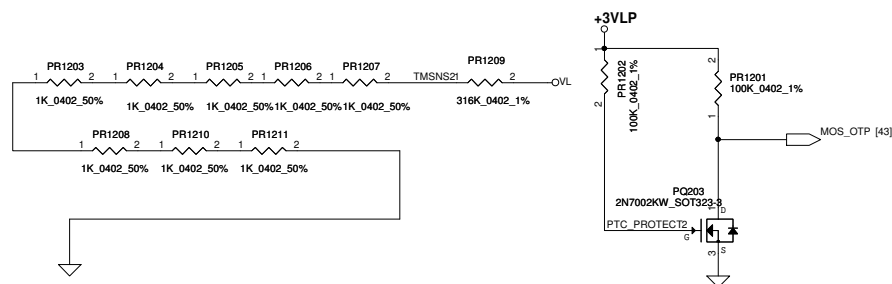
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Issued Date	2011/07/12	Deciphered Date	2012/07/01	Title	PC Interface	
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## Posestor



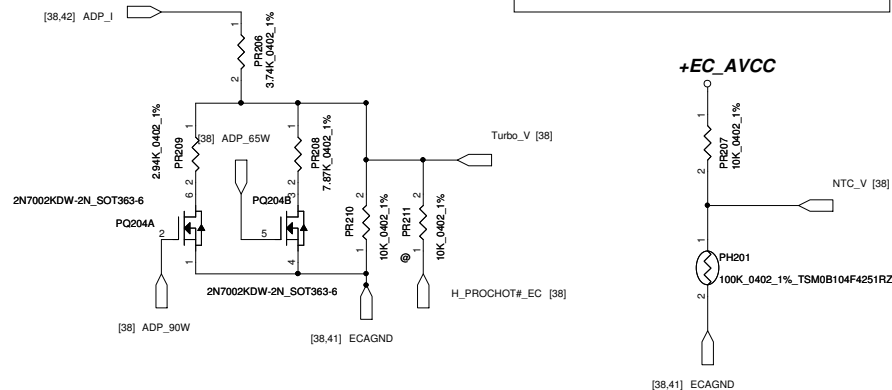
## Resistance between Turbo\_V and ECAGND:

45 W: 10K (Default)  
 65 W: 4.4K (ADP\_65W to High, ADP\_90W to Low)  
 90 W: 2.27K (ADP\_90W to High, ADP\_65W to Low)

## Trigger Power:

45 W → 55 W → ADP\_I:1.65  
 65 W → 74 W → ADP\_I:2.22  
 90 W → 106 W → ADP\_I:3.18

**PH201 under CPU bottom side :**  
 CPU thermal protection at 100 degree C



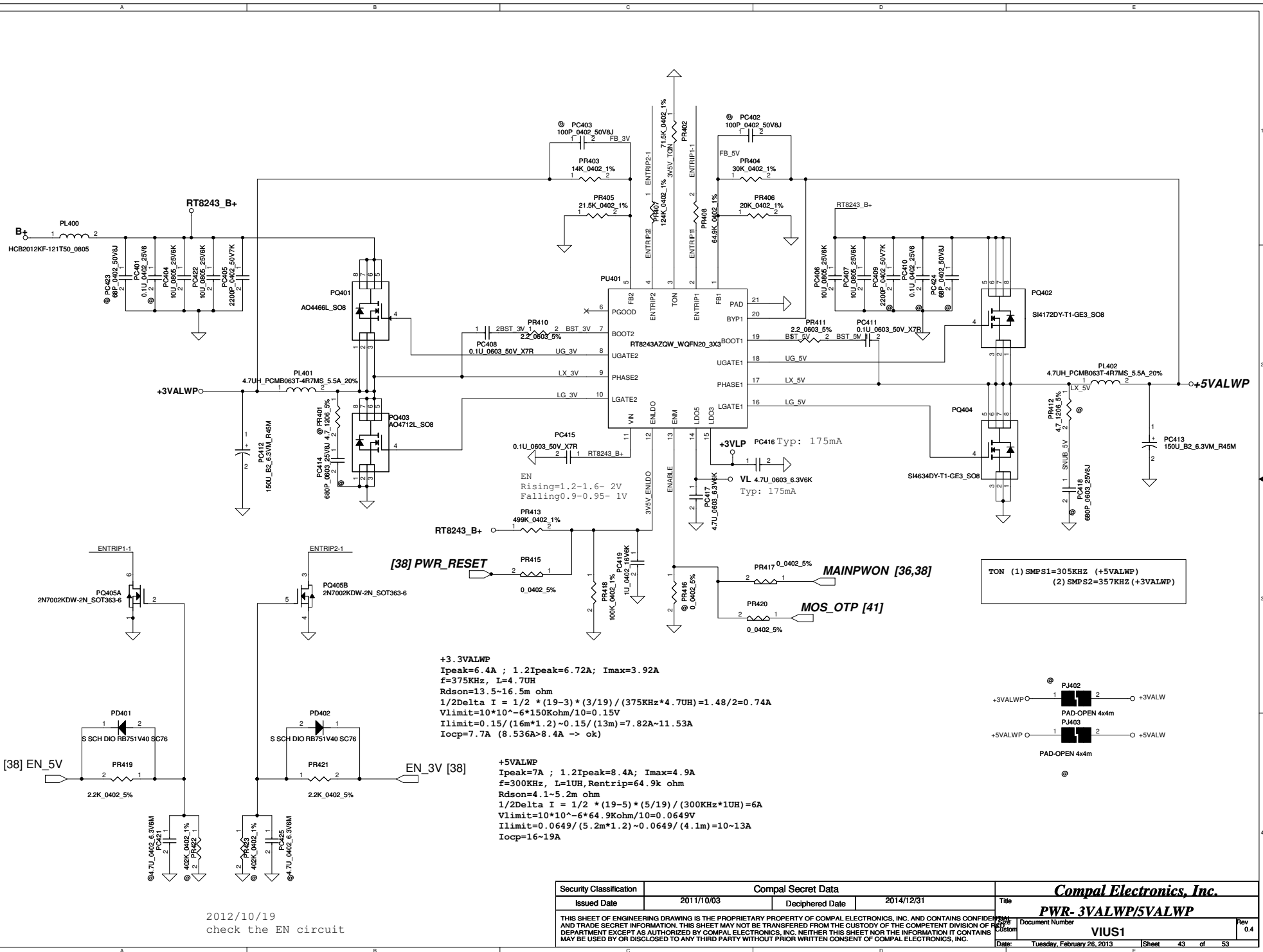
PH201:	Temp.	Rman.	Rnor.	Rmin. (Kohm)
	93	7.3419	7.0792	6.8253

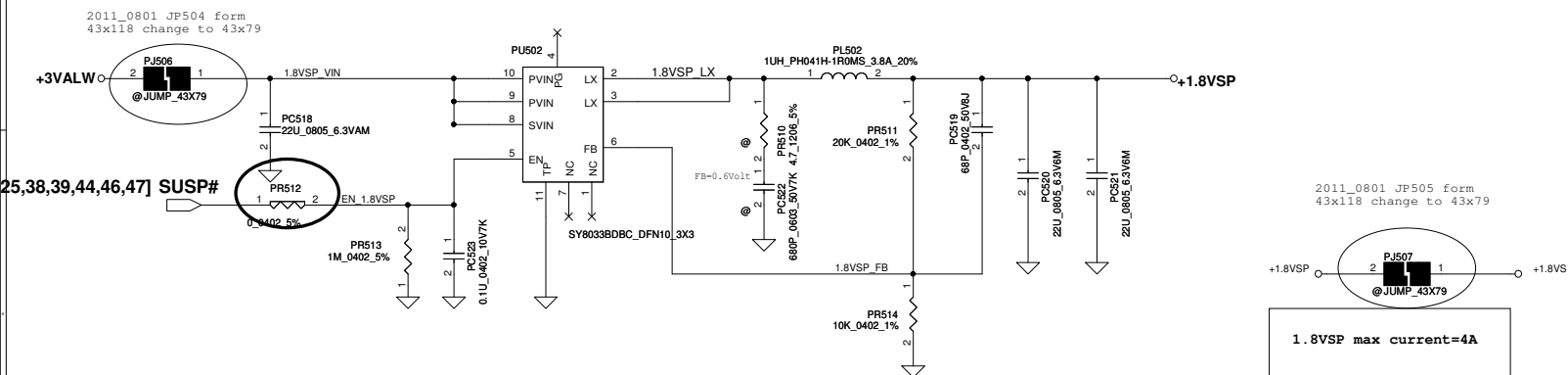
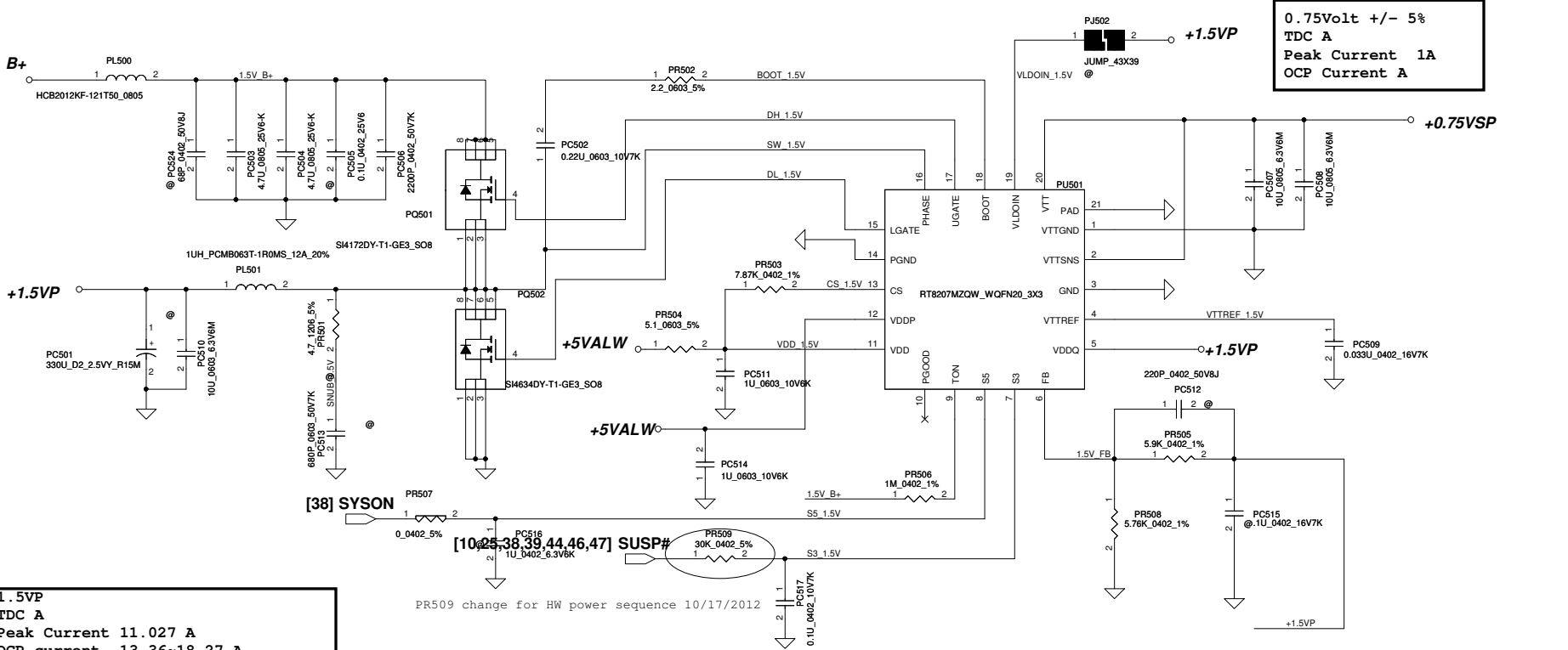
MOS\_OTP:  
 Default:High  
 Active :Low

PTC\_PROTECT:  
 Default:Low  
 Active :High

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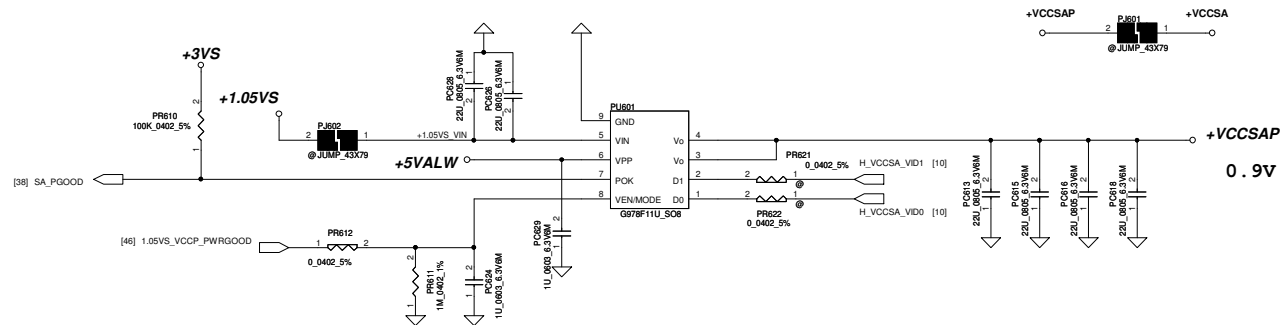
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
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VID [0]	VID[1]	VCCSA Vout
0	0	0.9V
0	1	0.85V
1	0	0.775V
1	1	0.75V

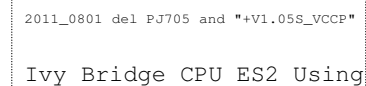
output voltage adjustable network

+VCC\_SAP  
TDC 2.9A  
Peak Current 4A  
OCP current 5.4A

The 1k PD on the VCCSA VIDs are empty.  
These should be stuffed to ensure that  
VCCSA VID is 00 prior to VCCIO stability.



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				Document Number
				VIUS1
				Rev
				0.4
				Date
				Wednesday, February 27, 2013
				Sheet
				45 of 53

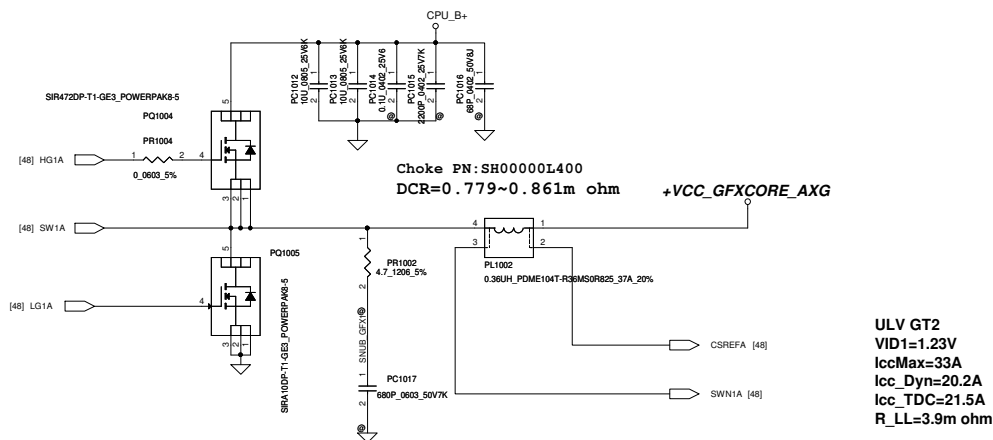
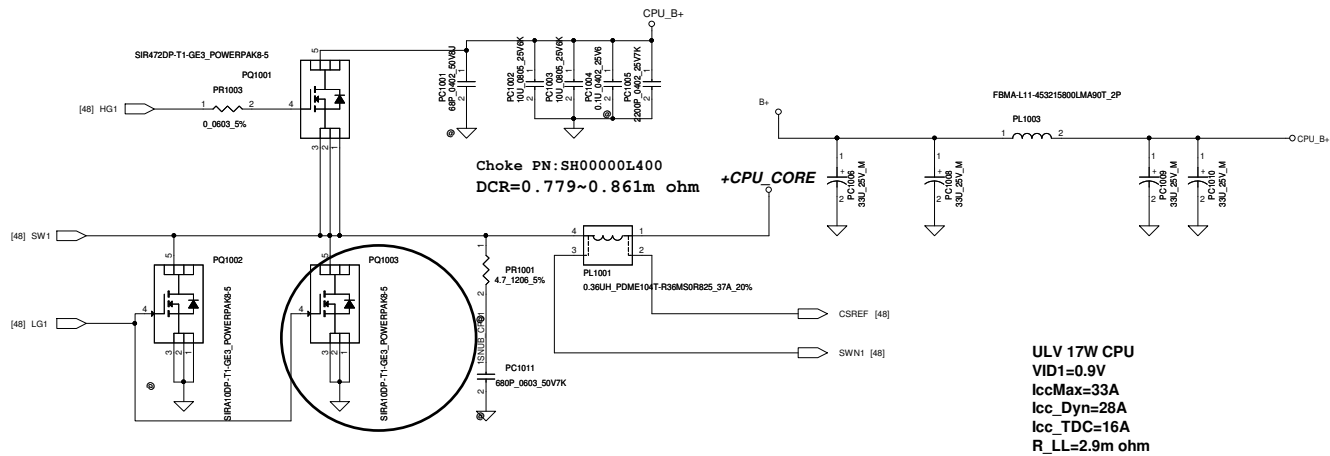


**WWW.AliSaler.Com**

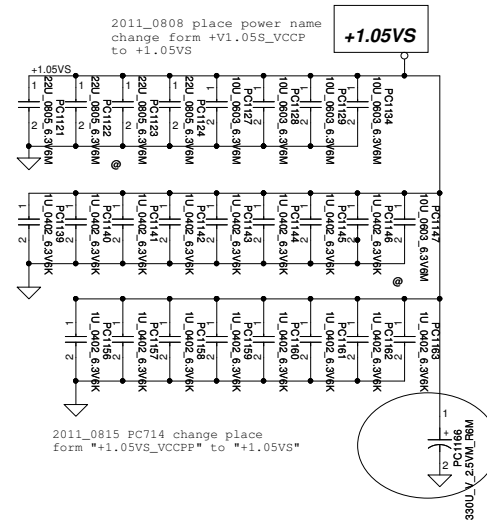
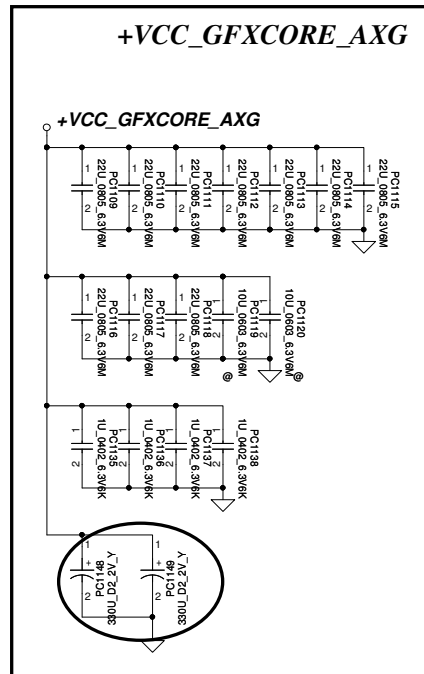
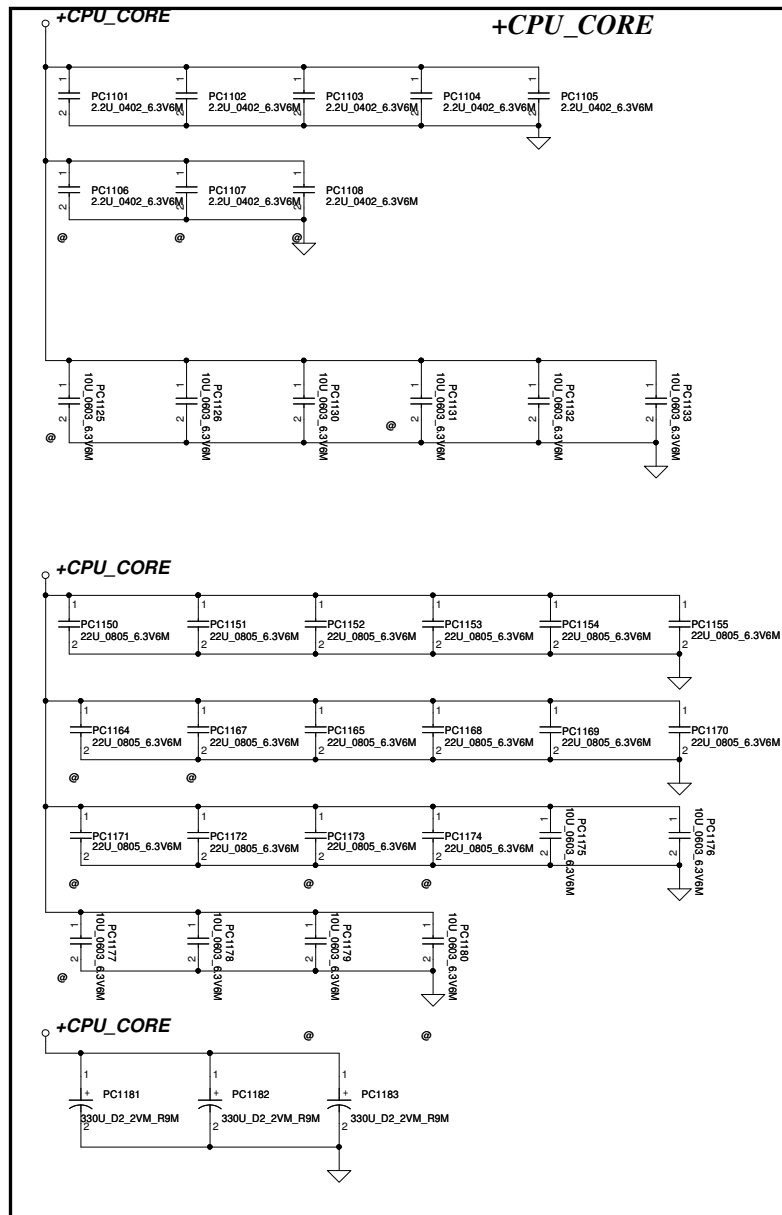






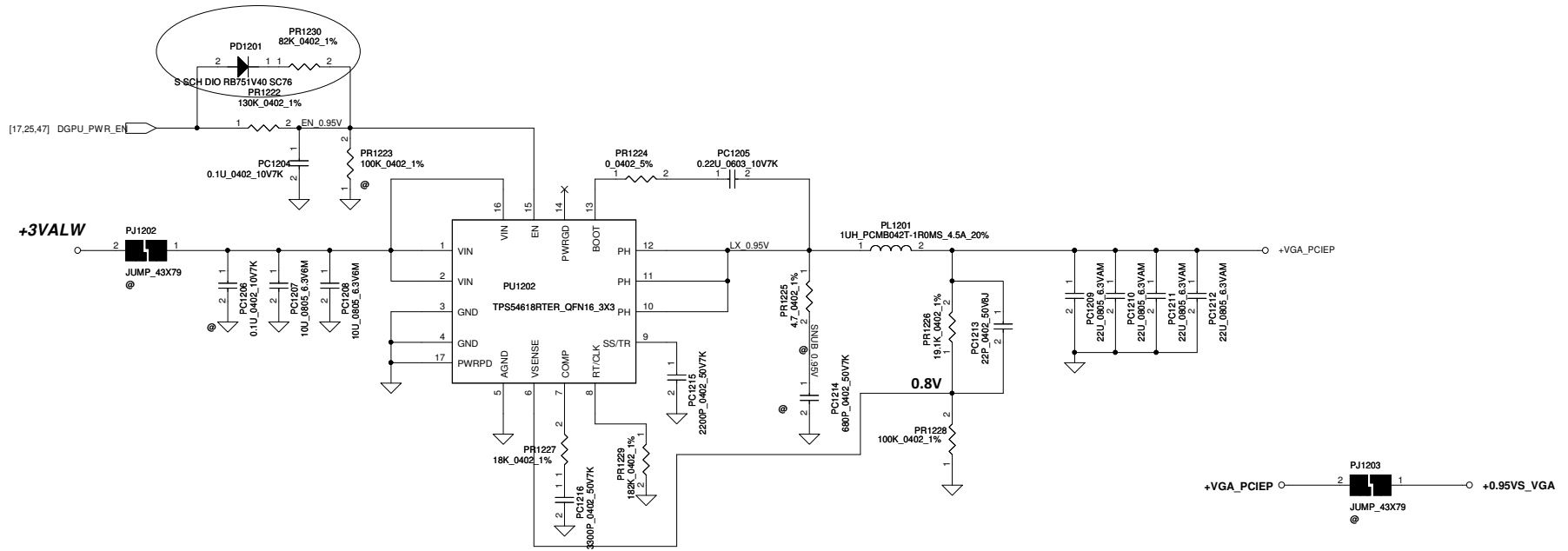


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PR1230,PD1201 add for HW power sequence required 10/31/2012



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## Version change list (P.I.R. List)

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for PWR

Item	Reason for change	PG#	Modify List	Date	Phase
1				2012/06/05	
2				2012/06/08	
3				2012/06/08	
4				2012/06/08	
5					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

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Version Change List (P.I.R. List)

Phase	Date	No.	BOM	Sch	Layout	Description	function
	2011/09/13	No1		V	V	Add C2325,C2326,C2327,C2328,C2329,R2319,R2324,Q2312	Add SBA function (+3VM) power

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				Rev	0.4
Date: Tuesday, February 26, 2013				Sheet	53 of 53